400073

National Semiconductor

Memory Databook

MEMORY
DATABOOK

1994 Edition

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Introduction

National Semiconductor's Non-Volatile Memory Databook is a representation of the **NEW Memory Products Division (MPD)**; a division that offers innovative system solutions to you, our customers.

National's memory products have come about through years of participation in the non-volatile memory market, which is why National is a world leader in this arena. As a matter of fact, in 1980 we brought to market the first low density EEPROMs: ¼ Kbit and 1 Kbit NMOS devices. We now offer three families of EEPROMs: MICROWIRE™ products in densities from ¼ Kbit to 4 Kbit; IIC™ products in densities from 2 Kbit to 16 Kbit; and a 4 Kbit Serial Peripheral Interface (SPI™) EEPROM. We were also the first company to manufacture CMOS EPROMs, which are currently available in all densities from 16 Kbit to 4 Mbit. Our portfolio is now growing to include 1 Mbit and 4 Mbit NOR FLASH, and 16 Mbit NAND FLASH.

In addition to the products listed above, we have brought to market memory devices designed to benefit our customers by meeting the needs of specific markets and systems. Some examples of that would be our Low Voltage EPROMs (3V ± 0.3V); our Processor Oriented EPROMs (POP™), which were designed to improve system performance 25%; and our "Burst" mode EPROM (in design)—a wordwide 1 Mbit EPROM with four data word bursts capable of operating in 33 MHz and 40 MHz systems with no wait states. Each of these products bring to you system solutions that provide the end user customer increased satisfaction.

The Memory Products Division of National Semiconductor is committed to excellence in design, manufacturing reliability, and service to our customers through the continued development of new technologies, products, solutions!

I sincerely hope that you will continue to look to National for all your non-volatile memory needs.

For additional information, please contact our Customer Response Center at 800-272-9959.

Thanks once again for your support!

Dr. Bami Bastani
VP and General Manager
Memory Products Division

National Semiconductor

Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The data sheet is printed for reference information only.

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Section 1

FLASH

Section 1 Contents

National Semiconductor

FLASH Memory Selection Guide

General Description

National Semiconductor's family of FLASH memory products cover applications for both code storage and data storage. The high density NM29N16 provides 16 Mbits of storage for data storage applications that require sequential access and high endurance. National's lower density NOR FLASH product line offers a reprogrammable solution for code storage.

Features

- High performance 0.7 μm CMOS
- Single or dual power supplies
- High endurance
  - 10k for NOR
  - 100k for NAND
- Embedded program/erase algorithm
- FLASH for all applications
  - Code storage (NOR)
  - File storage (NAND)

Available Product

NAND Flash	Packages	Speed
NM29N16	S, R	—
NOR Flash		
NM28F010	N, M, V, T, TR	100 ns, 120 ns, 150 ns

*The NM28F010 is advanced information only. Contact your local sales office for availability.

Ordering Information

NM 28 F 010 M 100

National Memory — NM

Power Supply Configuration — 28
- 28 = 5V V_{CC}, 12V V_{PP}
- 29 = 5V V_{CC}

FLASH Type — F
- F = NOR
- N = NAND

Size — 010
- 010 = 1 Mb
- 16 = 16 Mb

Packaging — M
- N = Plastic DIP
- M = SOP
- V = PLCC
- T = TSOP, Type I
- TR = Reversed TSOP, Type I
- S = TSOP, Type II
- R = Reversed TSOP, Type II

Access Time (speed) — 100
- 10 = 100 ns
- 12 = 120 ns
- 15 = 150 ns

National Semiconductor

ADVANCE INFORMATION

NM28F010
1-Mbit (131,072-Word x 8-Bit) CMOS FLASH

General Description

The NM28F010 is a 1,048,576-bit FLASH Electrically Erasable and Programmable non-volatile Memory device. The NM28F010 stores data reliably even after 10,000 program and erase cycles. The NM28F010 features single command control for read, chip erase, and programming operations to allow ease of use for on-board programming.

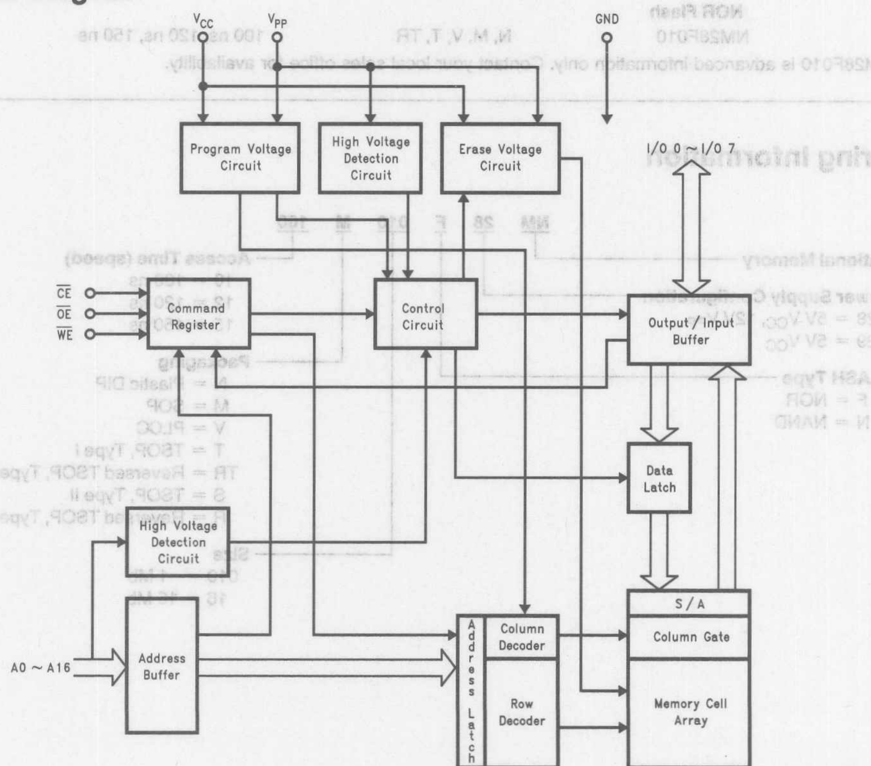
The NM28F010 is ideally suited for applications such as firmware storage, BIOS, engine control, and wireless communication—where EPROM has been used in the past.

The NM28F010 is available in either a 32-pin plastic DIP, SOP, PLCC, or forward and reverse bend TSOP packages to suit a variety of applications.

Features

- Power supply: V_{PP} = 12V ±0.6V
  V_{CC} = 5V ±0.25V
- Mode: Read/Reset
  Program (byte)
  Chip Erase
- Mode Control: command input
- Program: 10 µs typical per byte
  (loops = 10 µs x 25 max.)
- Erase: 1 sec typical per chip
  (loops = 10 ms x 1,000 max.)
- W/E Cycles: 10,000 cycles minimum target
- Access Time: 100 ns/120 ns
- Power Dissipation: Operating = 30 mA
  Standby = 100 µA
- Packages available: 32-pin DIP, SOP, TSOP, TRSOP, PLCC
- Pin compatible with NM27C010 EPROM

Functional Diagram



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National Semiconductor

NM29N16
16 MBit (2M x 8 Bit) CMOS NAND FLASH E^2PROM

General Description

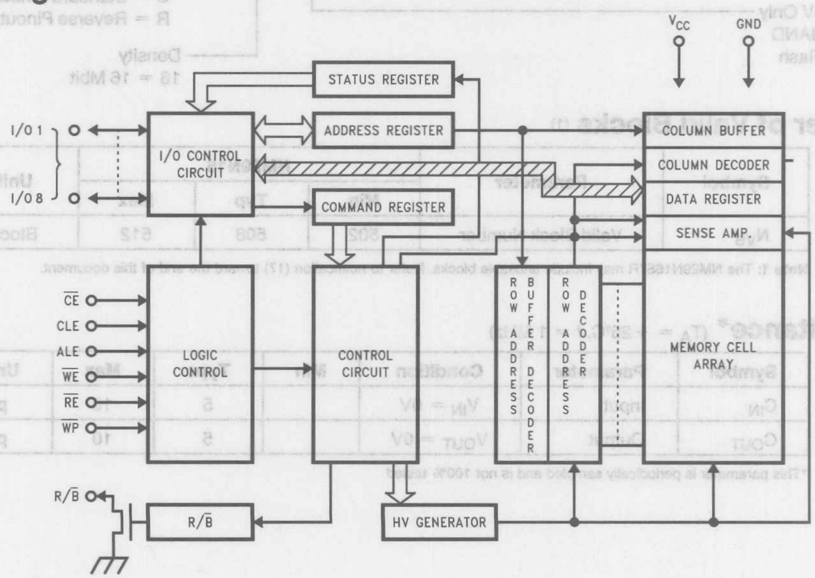
The NM29N16 is a 16 Mbit (2 Mbyte) NAND FLASH. The device is organized as an array of 512 blocks, each consisting of 16 pages. Each page contains 264 bytes. All commands and data are sent through eight I/O pins. To read data, a page is first transferred out of the array to an on-chip buffer. Sending successive read pulses ($\overline{RE}$ low) reads out successive bytes of data. The erase operation is implemented in either a single block (4 kbytes) or on multiple blocks at the same time. Programming the device requires sending address and data information to the on-board buffer and then issuing the program command. Typical program time for 264 bytes is less than 300 μs. The erase and program operations are internally timed.

The NM29N16 incorporates a number of features that make it ideal for portable applications requiring high density storage. These features include single 5V operation, high read/write endurance (10^6 cycle), and low current operation (15 mA during reads). The device comes in a TSOP Type II package which meets the requirements of PCMCIA cards. The NM29N16 is suited for numerrious applications such as Solid State Drives (SSD), Audio Recording, and Image Storage for digital cameras.

Features

- Single 5V ±5% power supply
- Write/Erase endurance of 100,000 cycles
- Fast Erase/Program Times
  - — Average Program Time of 300 μs/264 bytes
  - — Typical Block Erase Time of 6 ms
- Organized as 512 blocks, each consisting of 16 pages of 264 bytes
  - — Read/Program in pages of 264 bytes
  - — Erase in Blocks of 4 kbytes
- High Performance Read Access times
  - — Initial 25 μs page transfer
  - — Sequential 80 ns access
- Low Operating Current
  - — Typical Read current of 15 mA (80 ns sequential read)
  - — Typical Program current of 40 mA
  - — Typical Erase current of 20 mA
  - — Standby current less than 100 μA (CMOS)
- Command Register for Mode Control:
  - — Read
  - — Auto Page Program
  - — Auto Block Erase
  - — Auto Multi-Block Erase
  - —Reset
  - —Suspend/Resume
  - —Status Read
- 400 mil TSOP Type II Package, Normal or Reverse Pinout

Block Diagram



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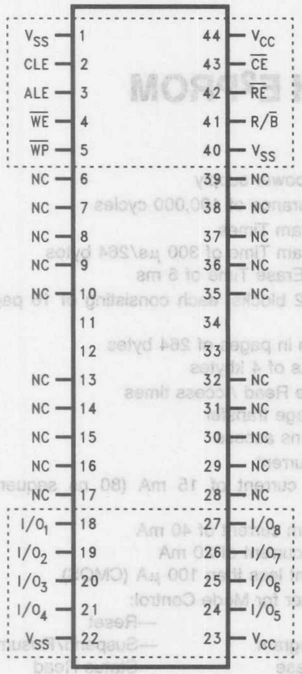
Pin Connection (Top View)

NM29N16S



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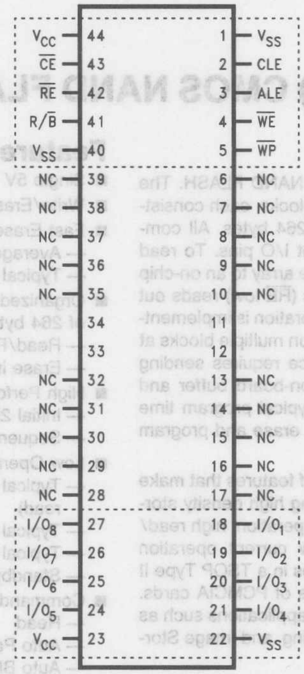
NM29N16R



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Pin Assignment

I/O_{1-8}	I/O Port
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{WP}$	Write Protect
$R/\overline{B}$	Ready/Busy
V_{CC}/V_{SS}	Power Supply/Ground

NM 29N 16 S

- NM — National Memory
- 29N — 5V Only NAND Flash
- 16 — Density: 16 = 16 Mbit
- S — Package Type: S = Standard Pinout, TSOP Type II; R = Reverse Pinout, TSOP Type II

Number of Valid Blocks (1)

Symbol	Parameter	NM29N16			Units
		Min	Typ	Max	
N_{VB}	Valid Block Number	502	508	512	Blocks

Note 1: The NM29N16S/R may include unusable blocks. Refer to notification (17) toward the end of this document.

Capacitance* ($T_A = +25°C$, f = 1 MHz)

Symbol	Parameter	Condition	Min	Type	Max	Units
C_{IN}	Input	$V_{IN} = 0V$		5	10	pF
C_{OUT}	Output	$V_{OUT} = 0V$		5	10	pF

*This parameter is periodically sampled and is not 100% tested

Power Supply (V_{CC}) −0.6V to 7.0V

Input Voltage (V_{IN})	−0.6V to 7.0V
Input/Output Voltage ($V_{I/O}$)	−0.6V to V_{CC} ±0.5V (≤7V)
Power Dissipation (P_D)	0.5W
Soldering Temperature (T_{solder}) (10 seconds)	260°C
Storage Temperature (T_{stg})	−55°C to 150°C
Operating Temperature (T_{opr})	0°C to 70°C

High Level Input Voltage (V_{IH})	2.2	V_{CC} + 0.5	V
Low Level Input Voltage (V_{IL})	−0.3*	0.8	V

* −2V (Pulse Width < 20 ns)

DC Operating Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}				±10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 0.4V to V_{CC}				±10	μA
I_{CC01}	Operating Current (Serial Read)	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA	t_{CYCLE} = 80 ns		15	30	mA
I_{CC02}	Operating Current (Serial Read)		t_{CYCLE} = 1 μs			5	mA
I_{CC03}	Operating Current (Command Input)	t_{CYCLE} = 80 ns			15	30	mA
I_{CC04}	Operating Current (Data Input)	t_{CYCLE} = 80 ns			50	70	mA
I_{CC05}	Operating Current (Address Input)	t_{CYCLE} = 80 ns			15	30	mA
I_{CC06}	Operating Current (Register Read)	t_{CYCLE} = 80 ns			15	30	mA
I_{CC07}	Programming Current				40	60	mA
I_{CC08}	Erasing Current				20	40	mA
I_{CCS1}	Standby Current	$\overline{CE}$ = V_{IH}				1	mA
I_{CCS2}	Standby Current	$\overline{CE}$ = V_{CC} − 0.2V				100	μA
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA		2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1 mA				0.4	V
$I_{OL}(R/\overline{B})$	Output Current of (R/$\overline{B}$) Pin	V_{OL} = 0.4V			10		mA

AC Test Conditions

Input Level	2.6V/0.4V
Input Comparison Level	2.2V/0.8V
Output Data Comparison Level	2.0V/0.8V
Output Load	1TTL & C_L (100 pF)
Transition Time	$t_T \leq 5$ ns

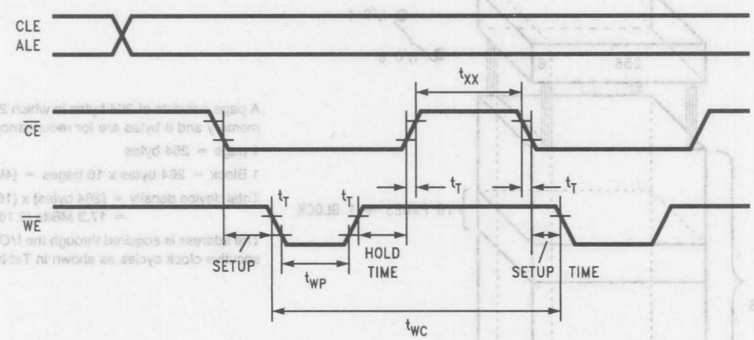
AC Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V +5%)

Symbol	Parameter	Min	Max	Unit	Notes
t_{CLS}	CLE Setup Time	20		ns	
t_{CLH}	CLE Hold Time	40		ns	
t_{CS}	$\overline{CE}$ Setup Time	20		ns	
t_{CH}	$\overline{CE}$ Hold Time	40		ns	
t_{WP}	Write Pulse Width	40		ns	
t_{ALS}	ALE Setup Time	20		ns	
t_{ALH}	ALE Hold Time	40		ns	
t_{DS}	Data Setup Time	30		ns	
t_{DH}	Data Hold Time	20		ns	
t_{WC}	Write Cycle Time	80		ns	(1)
t_{WH}	$\overline{WE}$ High Hold Time	20		ns	
t_{RR}	Ready to $\overline{RE}$ Falling Edge	20		ns	
t_{RC}	Read Cycle Time	80		ns	
t_{REA}	$\overline{RE}$ Access Time (Serial Data Access)		45	ns	
t_{CEH}	$\overline{CE}$ High Time at the Last Address in Serial Read Cycle	250		ns	(3)
t_{REAID}	$\overline{RE}$ Access Time (ID Read)		90	ns	
t_{RHZ}	$\overline{RE}$ High to Output High Impedance	5	20	ns	
t_{CHZ}	$\overline{CE}$ High to Output High Impedance		30	ns	
t_{REH}	$\overline{RE}$ High Hold Time	20		ns	
t_{IR}	Output High Impedance to $\overline{RE}$ Rising Edge	0		ns	
t_{RSTO}	$\overline{RE}$ Access Time (Status Read)	45		ns	
t_{CSTO}	$\overline{CE}$ Access Time (Status Read)	55		ns	
t_{RHW}	$\overline{RE}$ High to $\overline{WE}$ Low	0		ns	
t_{WHC}	$\overline{WE}$ High to $\overline{CE}$ Low	50		ns	
t_{WHR}	$\overline{WE}$ High to $\overline{RE}$ Low	50		ns	
t_{AR1}	ALE Low to $\overline{RE}$ Low (Address Register Read, ID Read)	200		ns	
t_{CR}	$\overline{CE}$ Low to $\overline{RE}$ Low (Address Register Read, ID Read)	200		ns	
t_R	Memory Cell Array to Starting Address		25	µs	
t_{WB}	$\overline{WE}$ High to Busy		200	ns	
t_{AR2}	ALE Low to $\overline{RE}$ low (Read Cycle)	150		ns	
t_{RB}	$\overline{RE}$ Last Clock Rising Edge to Busy (At Sequential Read)		200	ns	
t_{CRY}	$\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$ at Read Mode)		100+ tr(R/$\overline{B}$)	ns	(2)

AC Electrical Characteristics (T_A = 0°C to 70°C, V_{CC} = 5V ±5%) (Continued)

Note 1: In case that CLE, ALE, $\overline{CE}$ are input with clock, t_{WC} exceeds 80 ns

$$\frac{\text{set-up time}}{20\text{ ns}} + \frac{\text{hold time}}{40\text{ ns}} + \frac{t_{WP}}{40\text{ ns}} + \frac{t_{XX}}{} + \frac{4t_T}{20\text{ ns}}$$



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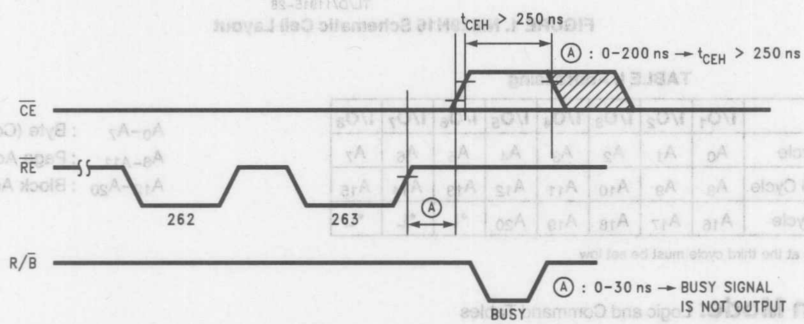
Note 2: $\overline{CE}$ high to Ready time depends on Pull up resister tied to R/$\overline{B}$ pin. (Refer to notification (11) toward the end of this document.)

Note 3: In the case that $\overline{CE}$ turns to a high level after accessing the last address (263) in read mode (1) or (2), $\overline{CE}$ high time must keep equal to or greater than 250 ns when the delay time of $\overline{CE}$ against $\overline{RE}$ is 0 to 200 ns as shown below.

In the second case, the device will not turn to a "Busy" state when the $\overline{CE}$ delay time is less than 30 ns.



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Programming and Erasing Characteristic (T_A = 0°C to 70°C, V_{CC} = 5V ±5%)

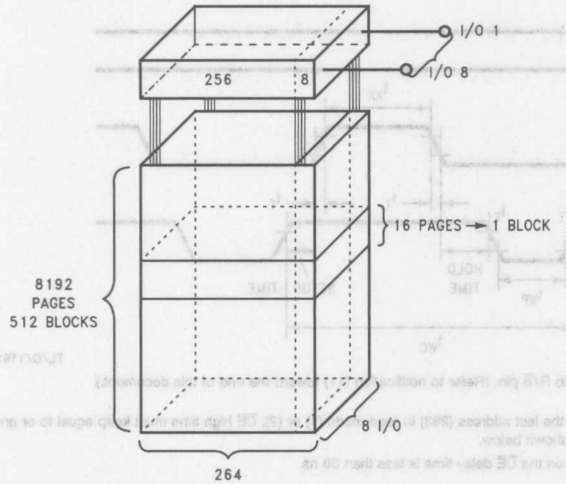
Symbol	Parameter	Min	Typ	Max	Unit	Notes
t_{PROG}	Average Programming Time		400	1000	μs	
N	Divided Number on Same Page			10	Cycles	(1)
t_{BERASE}	Block Erasing Time		6	100	ms	
$t_{MBERASE}$	Multi-Block Erasing Time		6–12	130	ms	
t_{SR}	Suspend Input to Ready			1	ms	

Note 1: Refer to the notification (16) toward the end of this document

1

Schematic Cell Layout and Address Assignment

Programming is done in page units of 264 Bytes while the erase operation is carried out in blocks of 4 kBytes.



A page consists of 264 bytes in which 256 bytes are for main memory and 8 bytes are for redundancy or other uses.

1 page = 264 bytes

1 Block = 264 bytes x 16 pages = (4k + 128) bytes

Total device density = (264 bytes) x (16 pages) x (512 block)
= 17.3 MBits (2.162 MBits)

The address is acquired through the I/O port using three consecutive clock cycles as shown in Table I.

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FIGURE 1. NM29N16 Schematic Cell Layout

TABLE I. Addressing

	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5	I/O_6	I/O_7	I/O_8
First Cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7
Second Cycle	A_8	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}
Third Cycle	A_{16}	A_{17}	A_{18}	A_{19}	A_{20}	*L	*L	*L

* I/O 6–8 at the third cycle must be set low

A_0–A_7 : Byte (Column) Address
A_8–A_{11} : Page Address in Block
A_{12}–A_{20} : Block Address

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read, Erase Suspend, and Reset are controlled by the twelve different command operations shown in Table III. The Address, Command Input and Data Input/Output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals as shown in Table II.

TABLE II. Logic Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command Input	H	L	L	↑	H	*
Data Input	L	L	L	↑	H	*
Address Input	L	H	L	↑	H	*
Address Output	L	H	L	H	↓	*
Serial Data Output	L	L	L	H	↓	*
During Programming (Busy)	*	*	*	*	*	H
During Erasing (Busy)	*	*	*	*	*	H
Program, Erase Inhibit	*	*	*	*	*	L

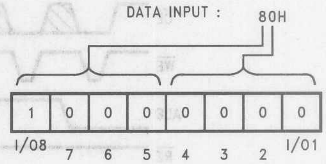
H: V_{IH}, L: V_{IL} *: V_{IH} or V_{IL}

Operation Mode: Logic and Command Tables (Continued)

TABLE III. Command Table (HEX Data)

	First Cycle	Second Cycle	Acceptable Command During Busy
Sequential Data Input	80		
Read Mode (1)	00		
Read Mode (2)	50		
Reset	FF		Yes
Auto Program	10		
Auto Block Erase	60	D0	
Auto Multi Block Erase	60...60	D0	
Suspend in Erasing	B0		Yes
Resume	D0		
Status Read	70		Yes
Register Read	E0		
ID Read	90		

Bit Assignment of HEX Data (Example)



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Once the device is set into Read mode by "00H" or "50H" command, additional Read commands are not needed for sequential page read operations. Table III shows the operation mode for Reads.

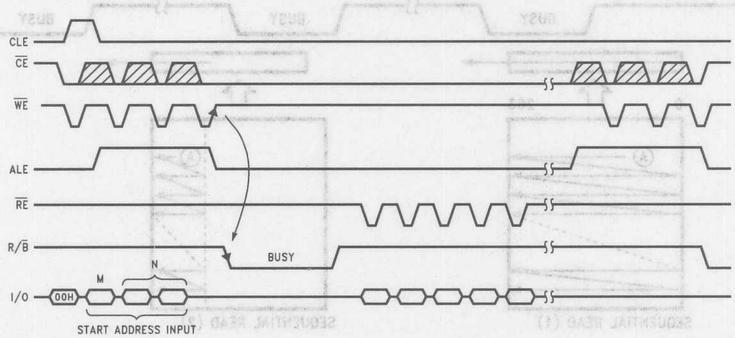
TABLE IV. Operation Mode for Reads

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O_1–I/O_8	Power
Read Mode	L	L	L	H	L	Data Output	Active
Output Deselect	L	L	L	H	H	High Impedance	Active
Standby	L	L	H	H	*	High Impedance	Standby

Device Operation

READ MODE (1)

The Read mode (1) is set by issuing a "00H" command to the command register. Refer to *Figure 2* below for timing details and block diagram.



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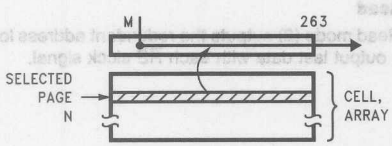


TL/D/11915–30

A data transfer operation from the cell array to the register starts at the rising edge of $\overline{WE}$ in the third cycle (after latching the address information). The device will be in a busy state during this transfer period.

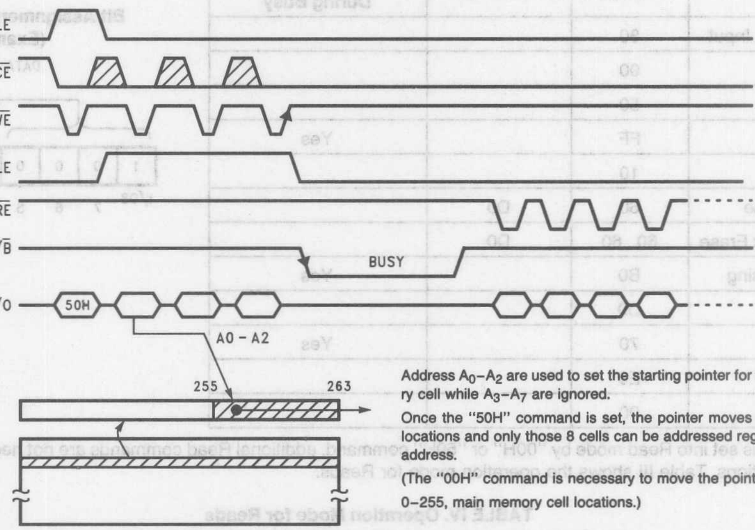
After the transfer period the device returns to a ready state. Serial data can be output synchronously with the $\overline{RE}$ clock from the designated starting pointer indicated during the address input cycle.

FIGURE 2. Read Mode (1) Operation

Device Operation (Continued)

READ MODE (2)

The Read mode (2) is the same timing as Read mode (1) but it is used to access information in the extra 8 byte redundancy area of the page. The starting pointer is therefore assigned between byte 256 and 263.



Address A_0–A_2 are used to set the starting pointer for the redundant memory cell while A_3–A_7 are ignored.

Once the "50H" command is set, the pointer moves to the redundant cell locations and only those 8 cells can be addressed regardless of the A_3–A_7 address.

(The "00H" command is necessary to move the pointer back to the 0–255, main memory cell locations.)

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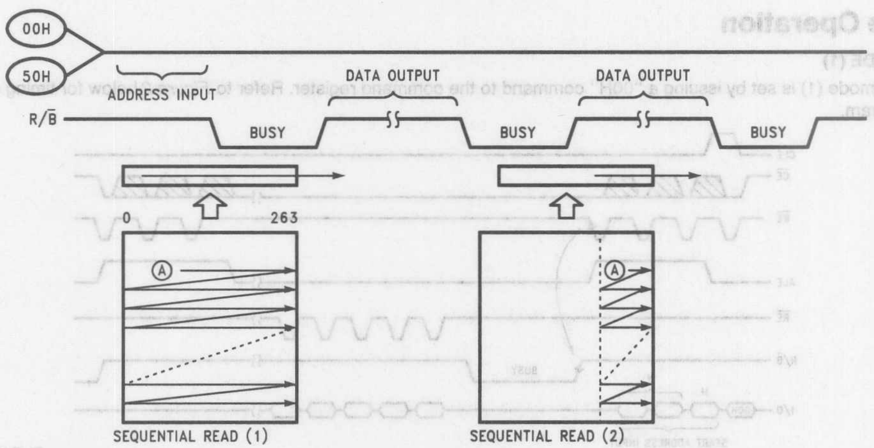
FIGURE 3. Read Mode (2) Operation

SEQUENTIAL READ (1) (2)

This mode allows sequential read without the additional address input



TL/D/11915–32

FIGURE 4. Sequential Read

Sequential Read mode (1) outputs the address 0 to 263 while Sequential Read mode (2) outputs the redundant address location only. When the pointer reaches the last address, the device continues to output last data with each $\overline{RE}$ clock signal.

Device Operation (Continued)

STATUS READ

The NM29N16S/R automatically implements the execution and verification of the program and erase operations. The status read function is used to monitor the Ready/Busy status of the device, determines the pass/fail result of a program or erase operation, and determines if the device is in a suspend or protect mode. The device status is output through the I/O port using the $\overline{RE}$ clock after a "70H" command input. The resulting information is outlined in Table V.

TABLE V. Status Output Table

	Status	Output	
I/O 1	Pass/Fail	Pass: "0"	Fail : "1"
I/O 2	Not Used	"0"	
I/O 3	Not Used	"0"	
I/O 4	Not Used	"0"	
I/O 5	Not Used	"0"	
I/O 6	Suspend	Suspended: "1"	Not suspended: "0"
I/O 7	Ready/Busy	Ready: "1"	Busy: "0"
I/O 8	Write Protect	Protect: "0"	Not Protect: "I"

The Pass/Fail status in I/O 1 is only valid when the device is in the Ready state. The device will always indicate a Pass status while in the Busy state at Read mode.

Application example with multiple devices is shown in *Figure 5* below.

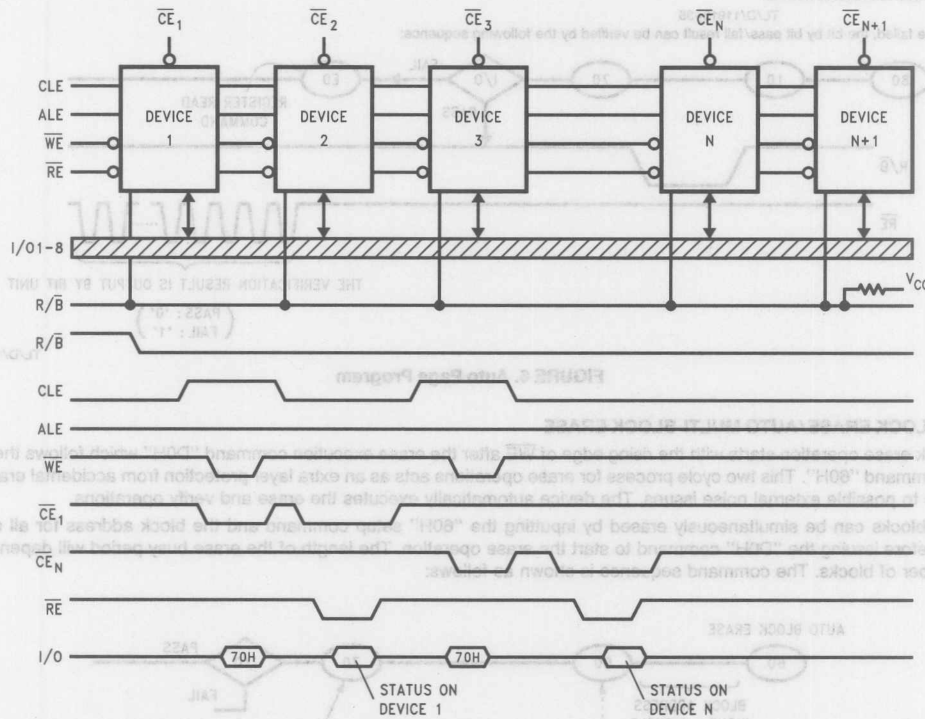


FIGURE 5. Status Read Timing Application Example

Note: If the R/$\overline{B}$ pin signals of multiple devices are common-wired as shown in the diagram, the status Read function can be used to determine the status of each individually selected device.

Device Operation (Continued)

AUTO PAGE PROGRAM

The NM29N16S/R implements the automatic page program operation by receiving a "10H" program command after the address and data have been input. The sequence of command, address and data input is shown below. (Refer to the detail timing chart).

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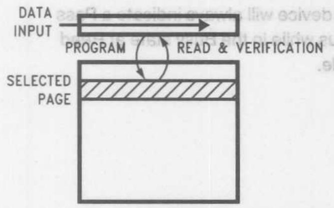

The data is transferred (programmed) from the register to the selected page at the rising edge of $\overline{WE}$ following the "10H" command input. The programmed data is transferred back to the register after programming to be automatically verified by the device. If the program does not succeed, the above program/verify operation is repeated by the device until success or the maximum loop number set in the device.

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If the device failed, the bit by bit pass/fail result can be verified by the following sequence:

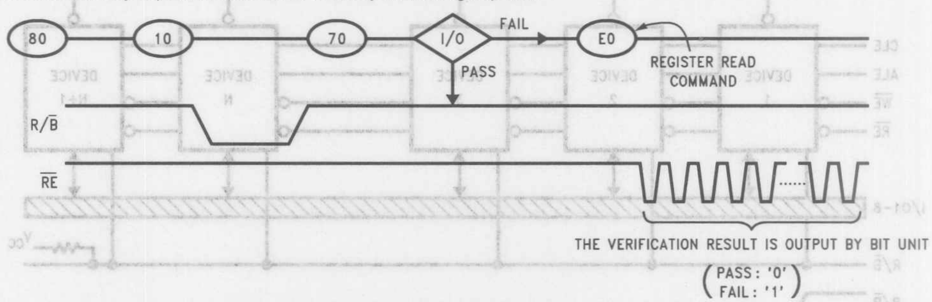

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FIGURE 6. Auto Page Program

AUTO BLOCK ERASE/AUTO MULTI-BLOCK ERASE

The block erase operation starts with the rising edge of $\overline{WE}$ after the erase execution command "D0H" which follows the erase setup command "60H". This two cycle process for erase operations acts as an extra layer protection from accidental erasure of data due to possible external noise issues. The device automatically executes the erase and verify operations.

Multiple blocks can be simultaneously erased by inputting the "60H" setup command and the block address for all desired blocks before issuing the "D0H" command to start the erase operation. The length of the erase busy period will depend upon the number of blocks. The command sequence is shown as follows:

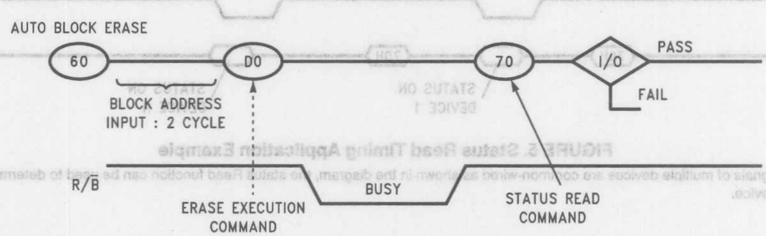

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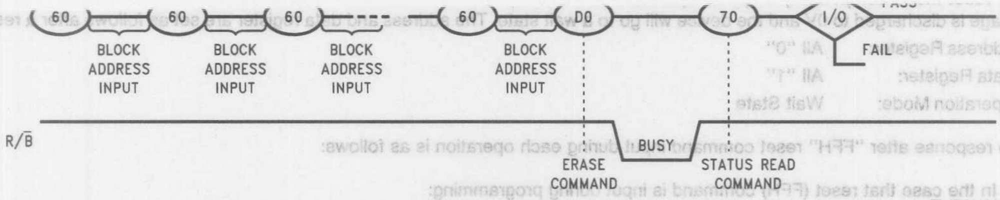
FIGURE 7. Auto Block Erase Operation



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Busy duration will be approximately (erase time + verify time) calculated as, $t_{MBERASE}$ = 6 ms + 15 μs × Erase block number

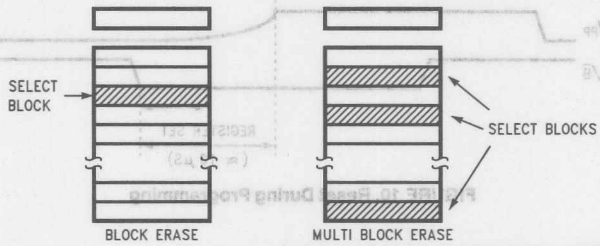

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FIGURE 8. Auto Block/Auto Multi Block Erase Operation

SUSPEND/RESUME ERASE OPERATION

Because a multi-block erase operation can keep the device in a busy state for an extended period of time, the NM29N16S/R has the ability to suspend the erase operation to allow program or read operations to be performed on the device. The block diagram and command sequence on this operation are shown as below. (Refer to the detail timing chart).

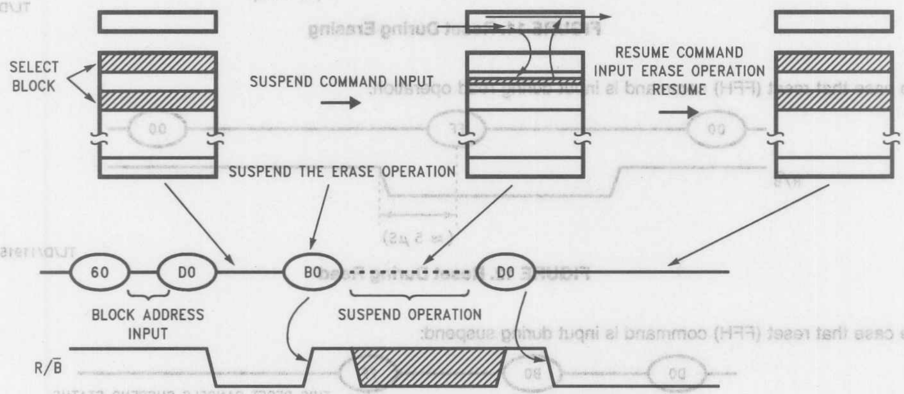

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FIGURE 9. Suspend/Resume Erase Operation

The B0...D0 suspend/resume cycle can be repeated up to 20 times during a multi-block erase operation. After the resume command input, the erase operation continues from the point at which it left off and does not have to restart.

1

Device Operation (Continued)

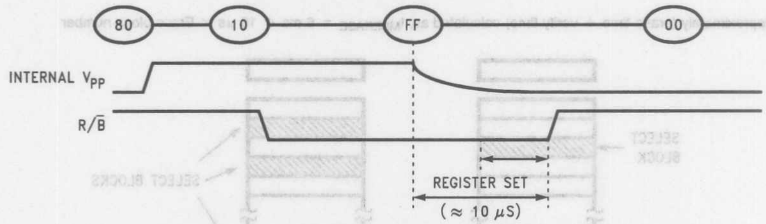
RESET

The reset mode compulsorily stops all operations. For example, in the case of a program or erase operation, the regulated voltage is discharged to 0V and the device will go to a wait state. The address and data register are set as follows after a reset:

- Address Register: All "0"
- Data Register: All "1"
- Operation Mode: Wait State

The response after "FFH" reset command input during each operation is as follows:

- In the case that reset (FFH) command is input during programming:



TL/D/11915-41

FIGURE 10. Reset During Programming

- In the case that reset (FFH) command is input during erasing:

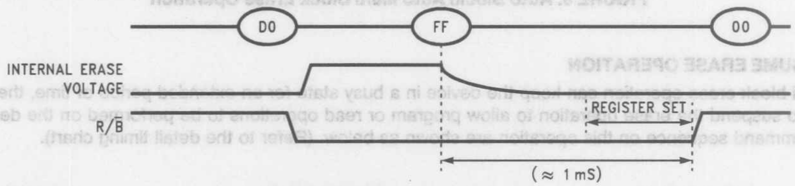


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FIGURE 11. Reset During Erasing

- In the case that reset (FFH) command is input during read operation:

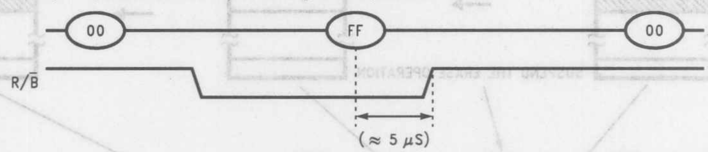

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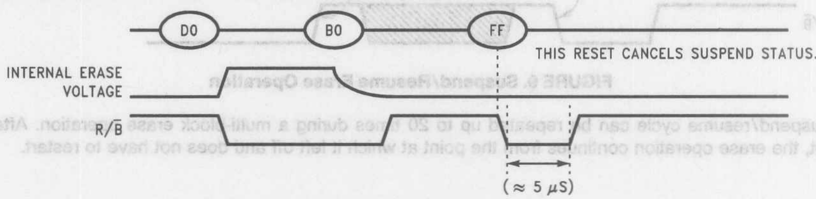
FIGURE 12. Reset During Read

- In the case that reset (FFH) command is input during suspend:



TL/D/11915-44

FIGURE 13. Reset During Suspend

Device Operation (Continued)

- In the case that the status read command (70H) is input after reset:

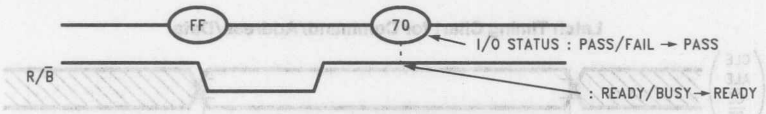


FIGURE 14. Read After Reset

- However the following operation is prohibited. If the following operation is executed, set up for address and data register can not be guaranteed.

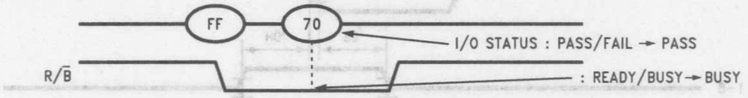


FIGURE 15. Prohibited Reset

- In the case that the reset command is input in succession:

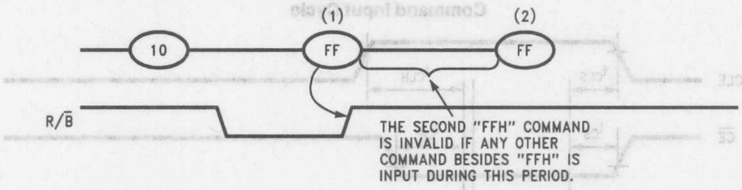


FIGURE 16. Consecutive Resets

ID READ

The NM29N16S/R contains an ID code to identify the device type and the manufacturer. The ID codes are read out using the following timing conditions:

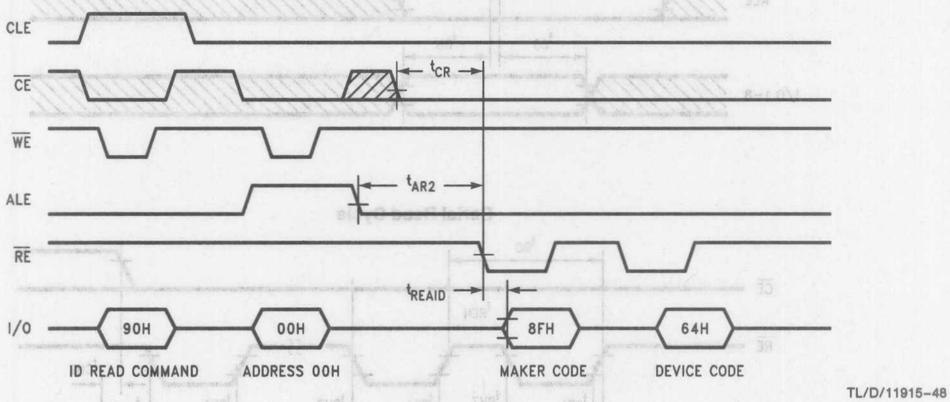


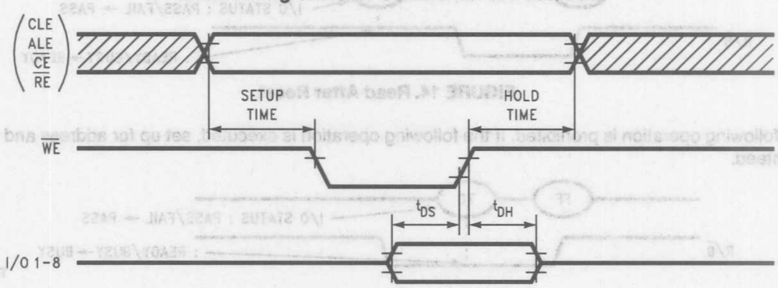
TABLE VI. Code Table

	I/O8	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	Hex Data
Maker Code	1	0	0	0	1	1	1	1	8FH
Device Code	0	1	1	0	0	1	0	0	64H

Refer to the timing specifications for the access time of t_{READ}, t_{CR}, t_{AR2}.

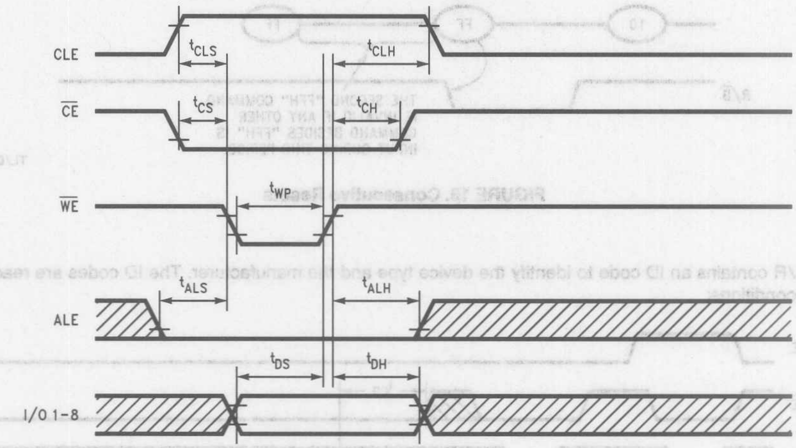
Timing Diagrams

Latch Timing Chart for Command/Address/Data



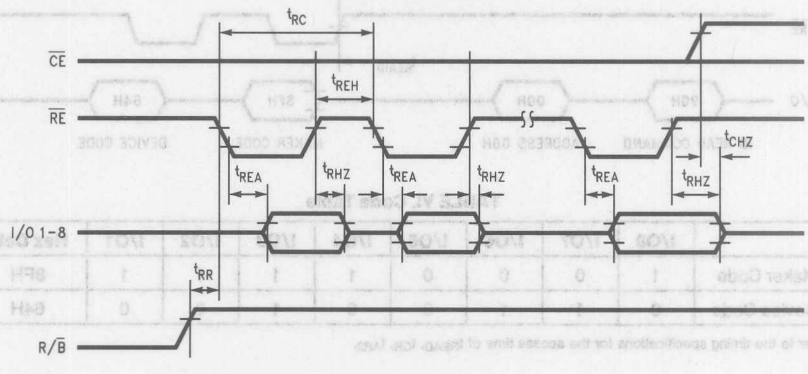
TL/D/11915-7

Command Input Cycle



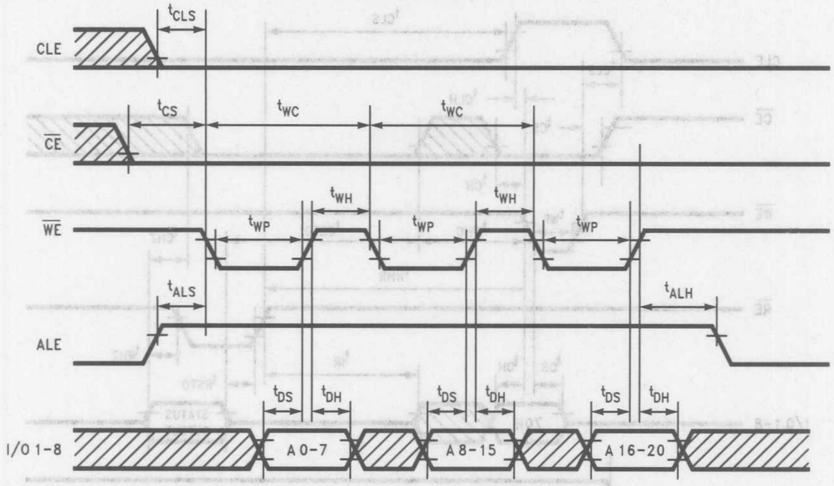
TL/D/11915-8

Serial Read Cycle



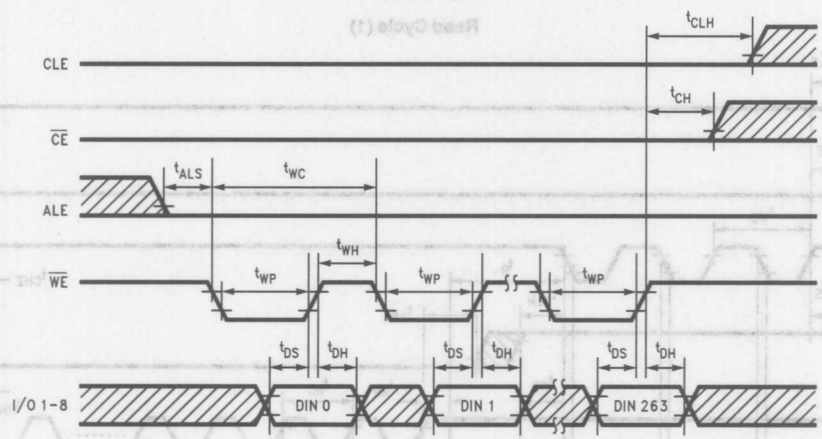
TL/D/11915-26

Address Input Cycle



TL/D/11915-9

Data Input Cycle

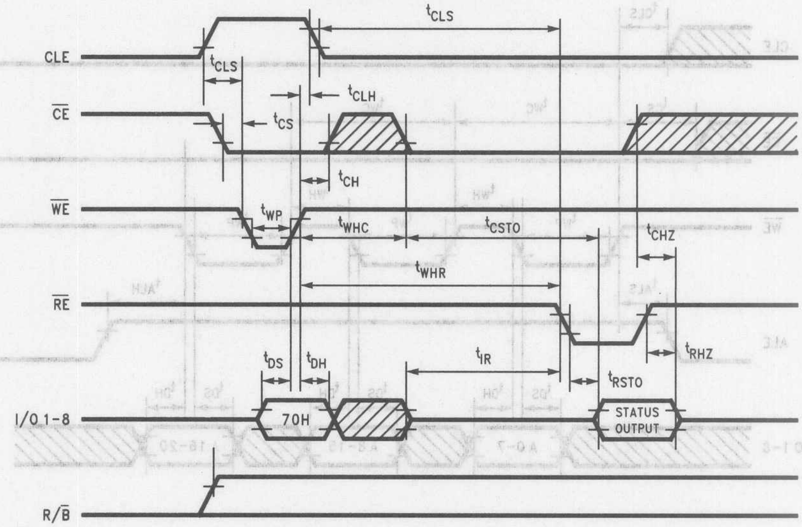


TL/D/11915-10

1

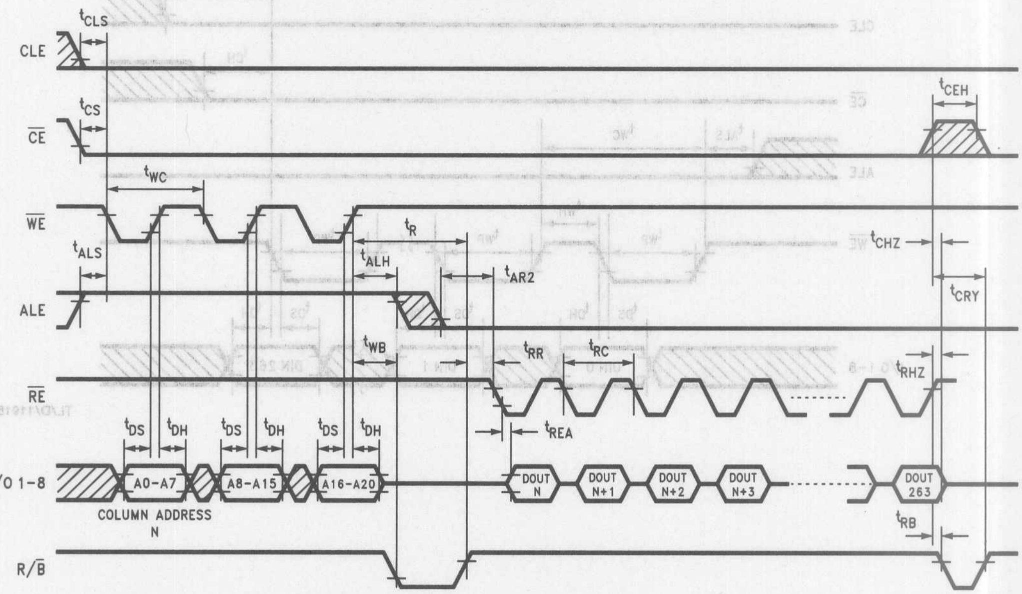
Timing Diagrams (Continued)

Status Read Cycle



TL/D/11915–11

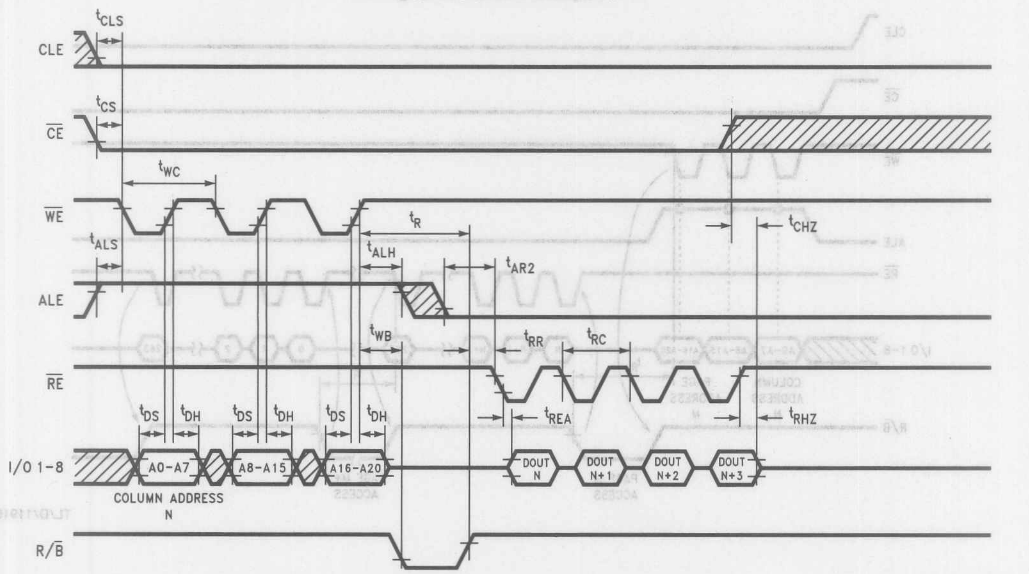
Read Cycle (1)



TL/D/11915–12

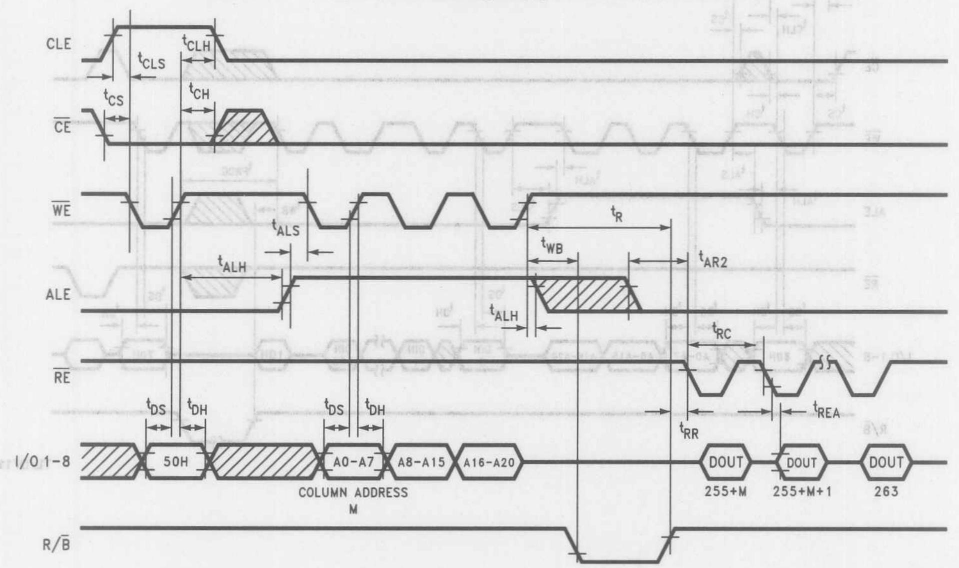
Timing Diagrams (Continued)

Read Cycle (1): Terminated by $\overline{CE}$



TL/D/11915-13

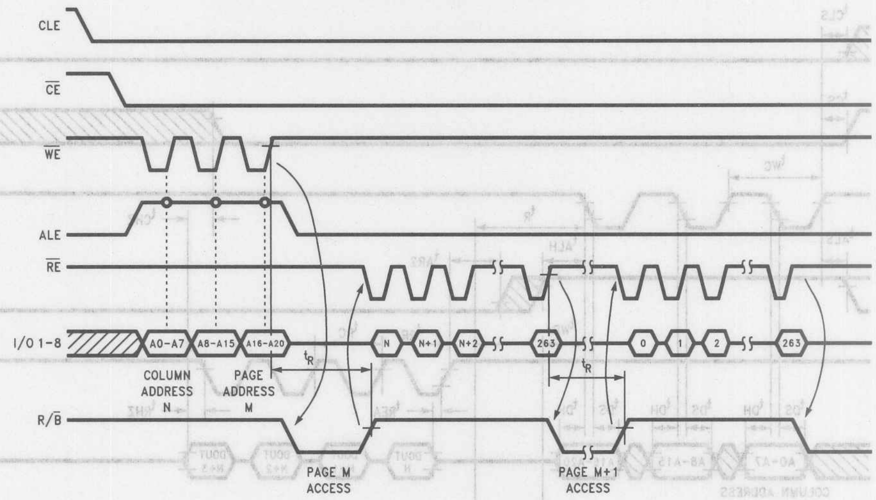
Read Cycle (2)



TL/D/11915-14

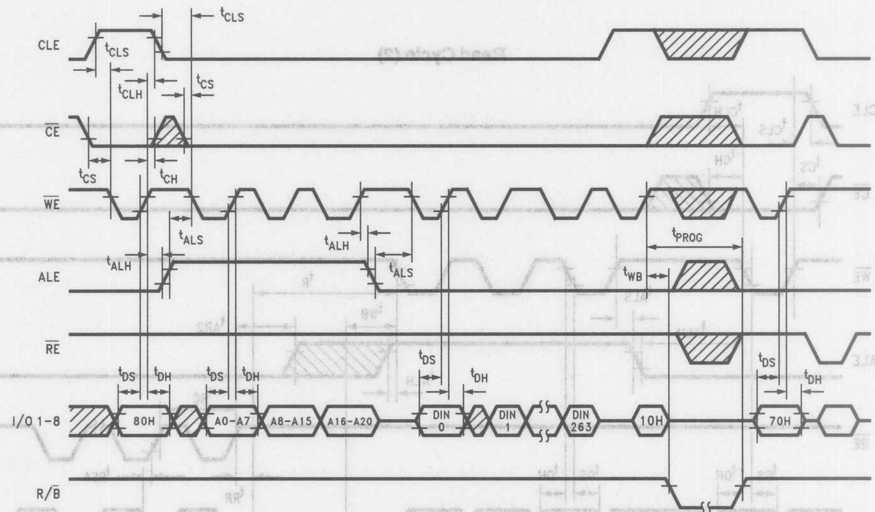
Timing Diagrams (Continued)

Sequential Read Timing



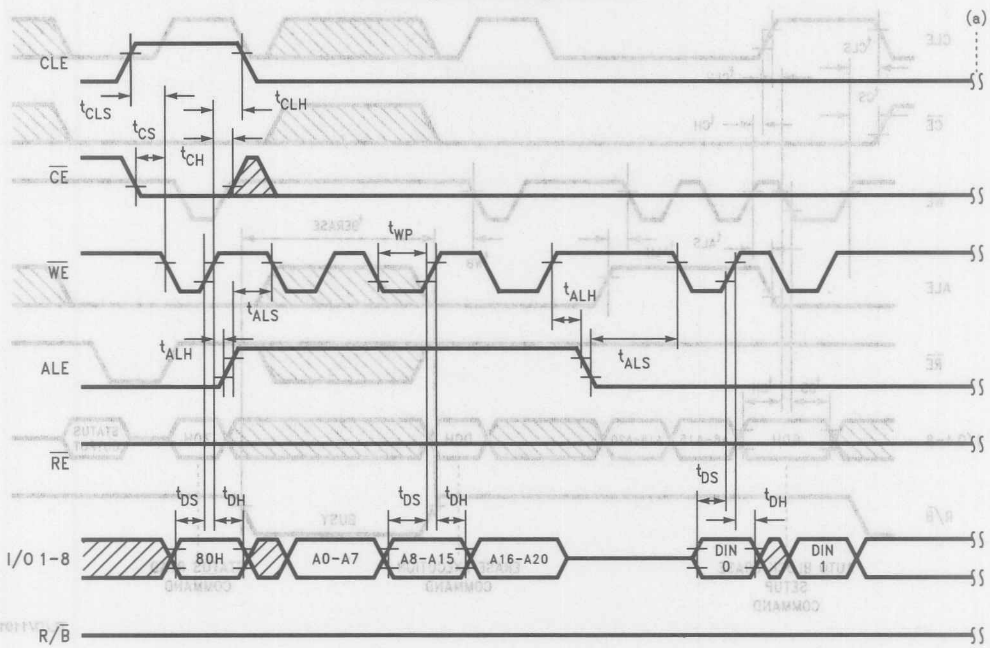
TL/D/11915-15

Auto Program Timing Chart

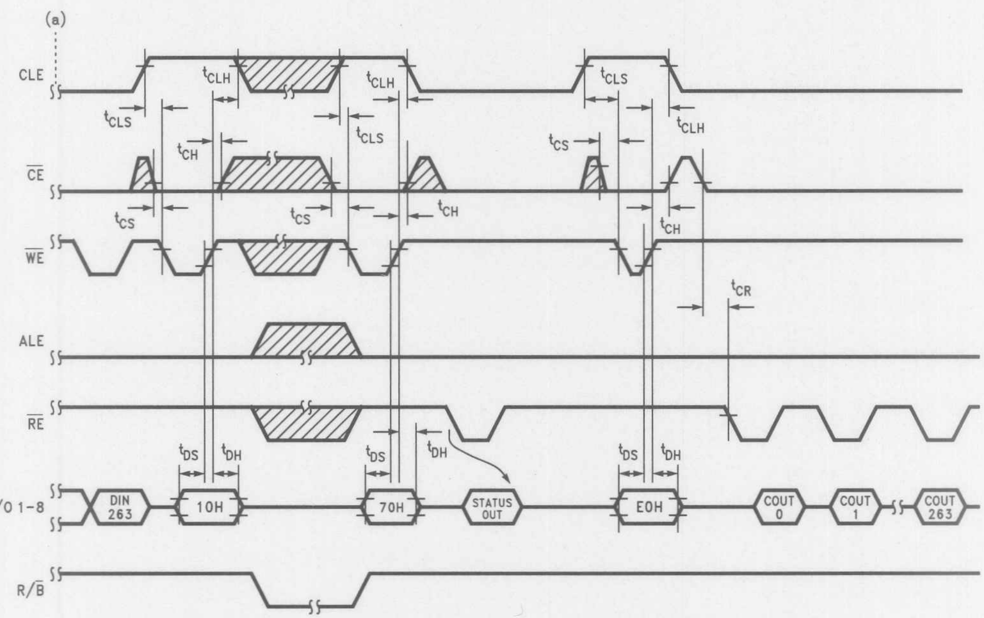


TL/D/11915-16

Auto Program and Register Read



TL/D/11915-17

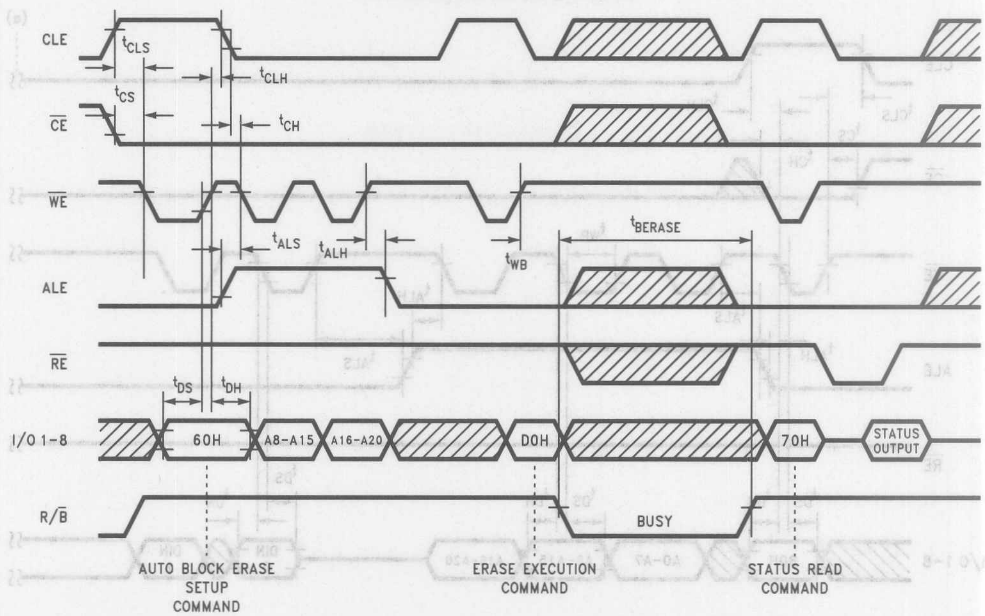


TL/D/11915-18

(a): Continued

Timing Diagrams (Continued)

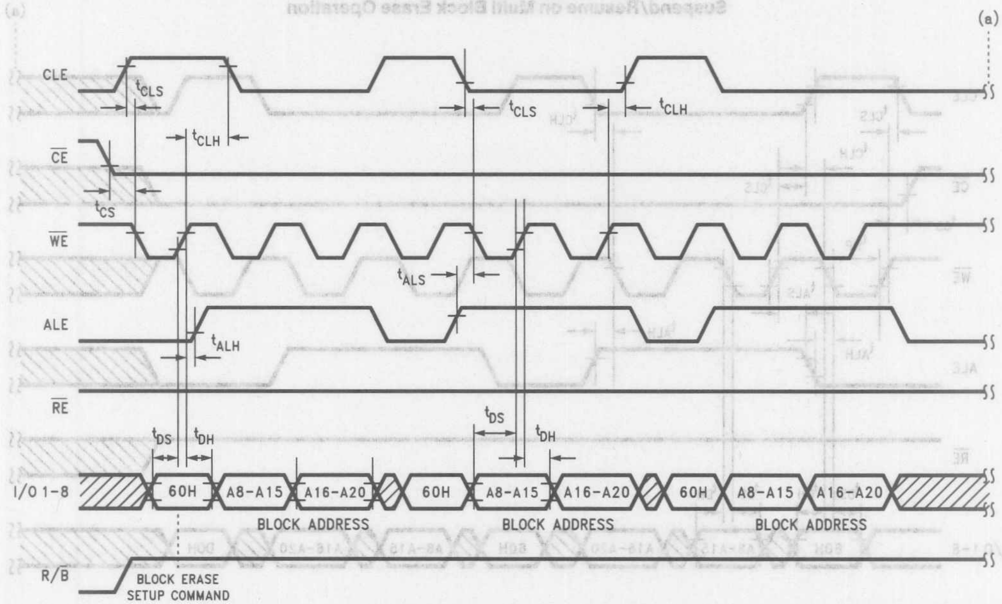
Auto Block Erase Timing



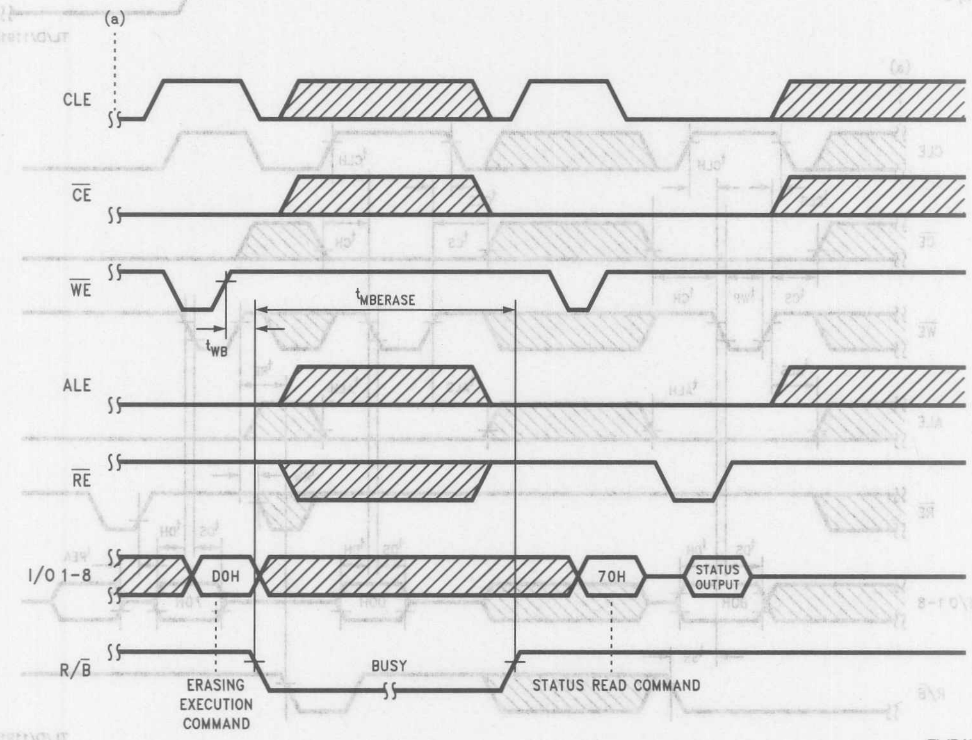
TL/D/11915-19

Timing Diagrams (Continued)

Auto Multi Block Erase Timing

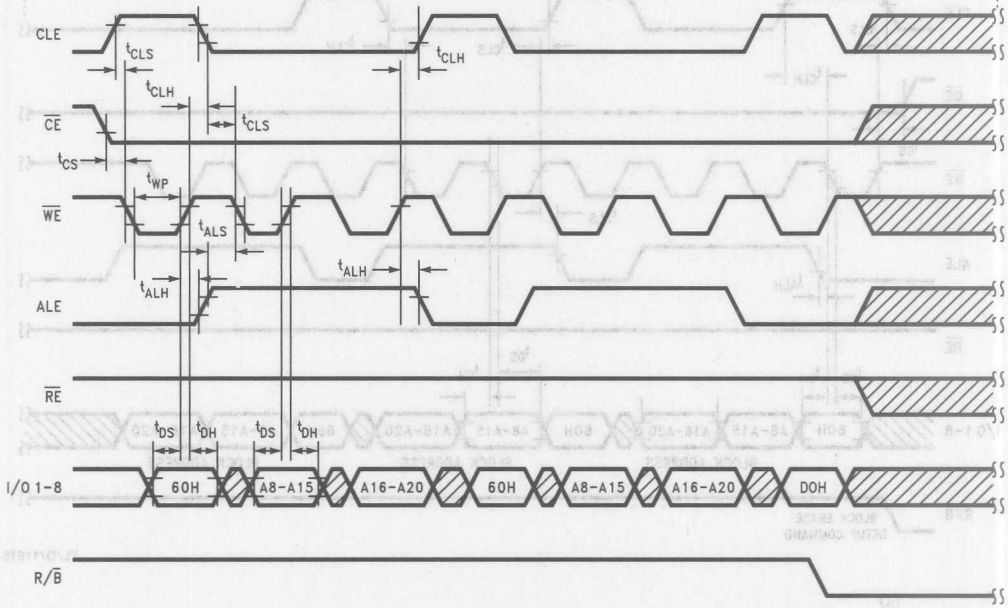


TL/D/11915-20

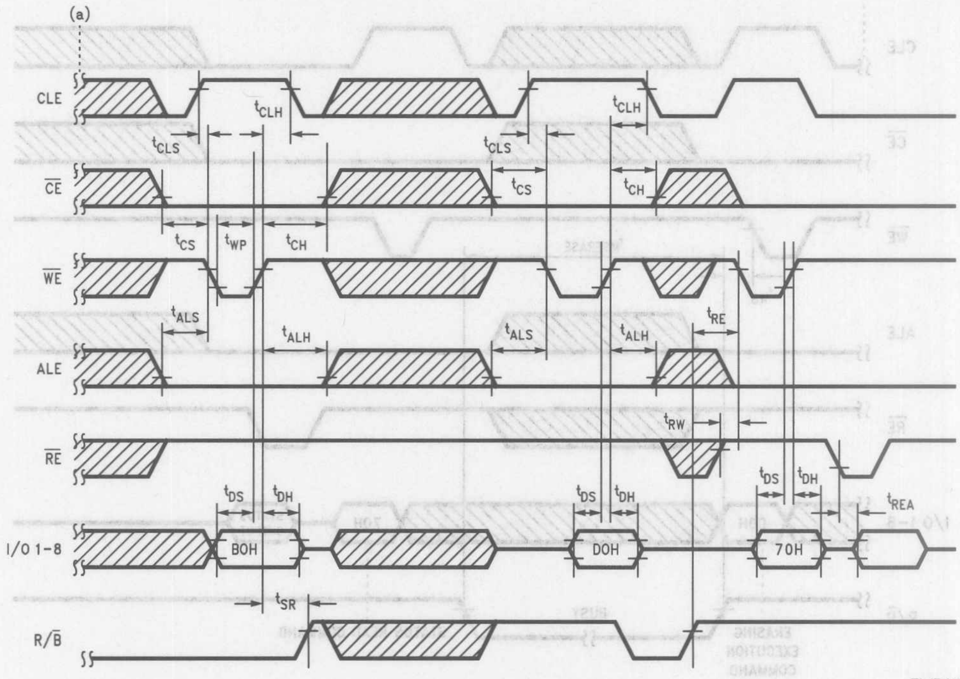


TL/D/11915-21

(a): Continued

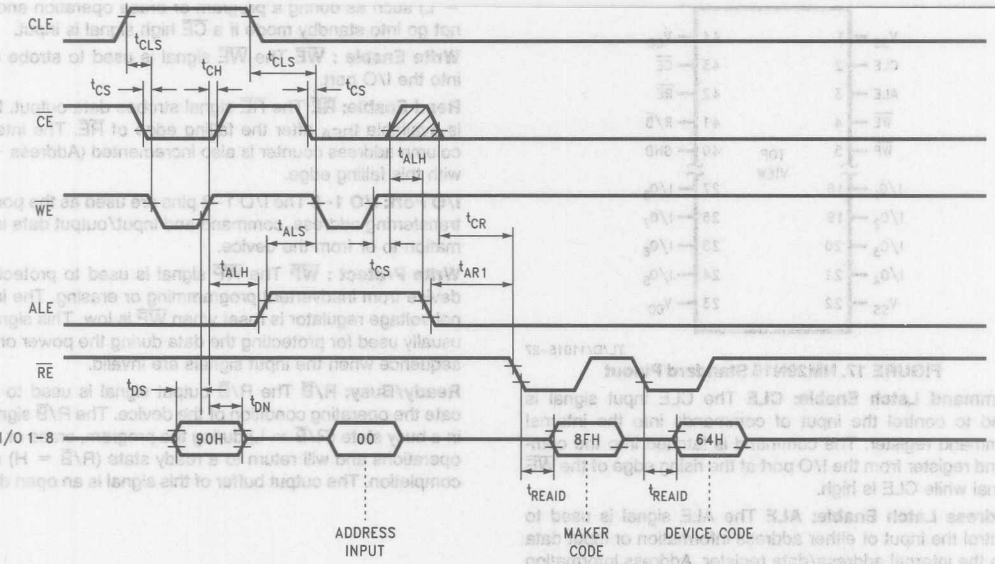


TL/D/11915-22



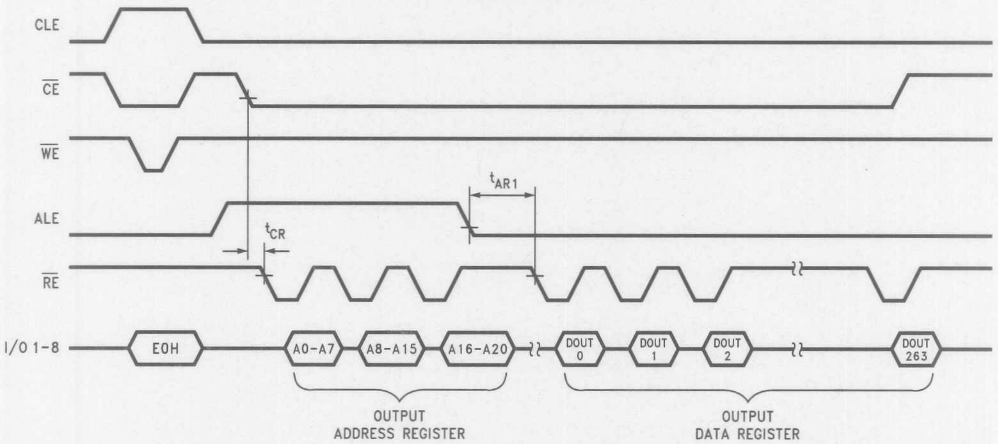
TL/D/11915-23

(a): Continued



TL/D/11915-24

Register Read Cycle

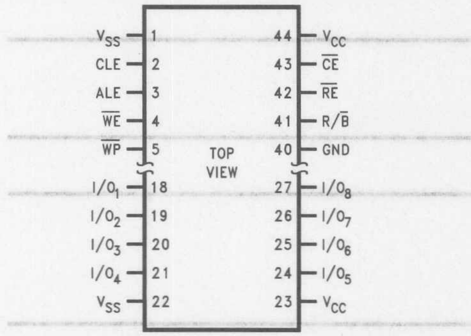


TL/D/11915-25

1

Pin Functions

The NM29N16 is a sequential access memory which utilizes time sharing input of address and data information. The device pinout is configured as shown in *Figure 17*.



TL/D/11915-27

FIGURE 17. NM29N16 Standard Pinout

Command Latch Enable: CLE The CLE input signal is used to control the input of commands into the internal command register. The command is latched into the command register from the I/O port at the rising edge of the $\overline{WE}$ signal while CLE is high.

Address Latch Enable: ALE The ALE signal is used to control the input of either address information or input data into the internal address/data register. Address information is latched at the rising edge of $\overline{WE}$ if ALE is high. Input data is latched if ALE is low.

Chip Enable : $\overline{CE}$ The device goes into a low power standby mode during a read operation when $\overline{CE}$ goes high. The $\overline{CE}$ signal is ignored when the device is in a busy state ($R/\overline{B}$ = L) such as during a program or erase operation and will not go into standby mode if a $\overline{CE}$ high signal is input.

Write Enable : $\overline{WE}$ The $\overline{WE}$ signal is used to strobe data into the I/O port.

Read Enable: $\overline{RE}$ The $\overline{RE}$ signal strobes data output. Data is available t_{REA} after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address + 1) with this falling edge.

I/O Port: I/O 1–8 The I/O 1–8 pins are used as the port for transferring address, command and input/output data information to or from the device.

Write Protect : $\overline{WP}$ The $\overline{WP}$ signal is used to protect the device from inadvertent programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is low. This signal is usually used for protecting the data during the power on/off sequence when the input signals are invalid.

Ready/Busy: $R/\overline{B}$ The $R/\overline{B}$ output signal is used to indicate the operating condition of the device. The $R/\overline{B}$ signal is in a busy state ($R/\overline{B}$ = L) during the program, erase or read operations and will return to a ready state ($R/\overline{B}$ = H) after completion. The output buffer of this signal is an open drain.

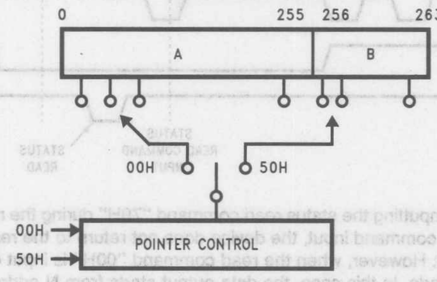
Supplementary Device Operation

(1) PROHIBITION OF UNSPECIFIED COMMANDS

The operation commands are listed in Table III. Data input as a command other than the specified commands in Table III is prohibited. Stored data may be corrupted if an unspecified command is entered during the command cycle.

(2) POINTER CONTROL FOR "00H", "50H"

The NM29N16S/R has two read modes to set the destination of the pointer in either the main memory area of a page or the redundancy area. The pointer can be designated at any location between 0 and 255 in read mode (1) and between 256 and 263 in read mode (2). *Figure 18* shows the block diagram of their operations.



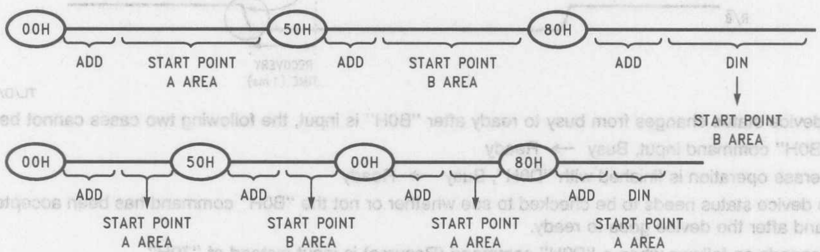
TL/D/11915–49

FIGURE 18. Pointer Control

The pointer is set to region "A" by the "00H" command and to region "B" by the "50H" command.

(Example)

The "00H" command needs to be input to set the pointer back to region "A" when the pointer exists in region "B".

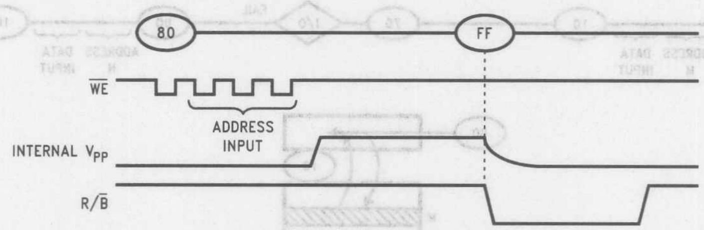


TL/D/11915–50

FIGURE 19. Example for Pointer Set

(3) ACCEPTABLE COMMANDS AFTER SERIAL INPUT COMMAND OF "80H"

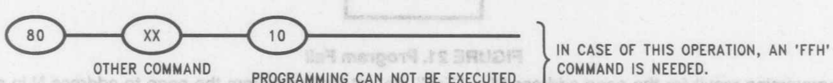
Once the serial input command ("80H") is input, do not input any command other than the program execution command ("10H") or the reset command ("FFH") during programming.



TL/D/11915–51

FIGURE 20. Reset After Serial Input

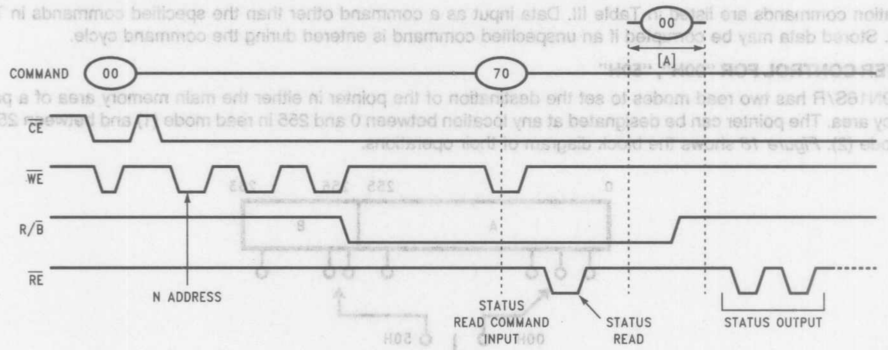
If a command other than "10H" or "FFH" is input, the program operation is not performed.



TL/D/11915–52

Supplementary Device Operation (Continued)

(4) STATUS READ DURING READ OPERATION

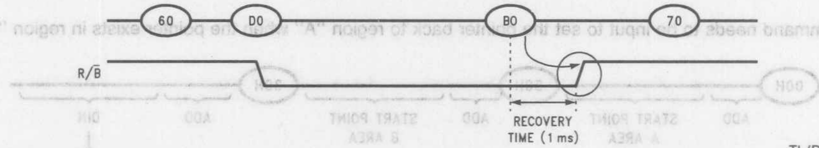


TL/D/11915–53

The device status can be read out by inputting the status read command "70H" during the read mode. Once the device is set to the status read mode after the "70H" command input, the device does not return to the read mode. Therefore, the status read during the read operation is prohibited. However, when the read command "00H" is input during [A], the status mode is reset, then the device returns to the read mode. In this case, the data output starts from N address without address input.

(5) SUSPEND COMMAND "B0H"

The following issues need to be observed when the device is interrupted by a "B0H" command during block erasing.



TL/D/11915–54

Although the device status changes from busy to ready after "B0H" is input, the following two cases cannot be recognized.

- — After a "B0H" command input, Busy → Ready
- — After an erase operation is finished with "D0H", Busy → Ready

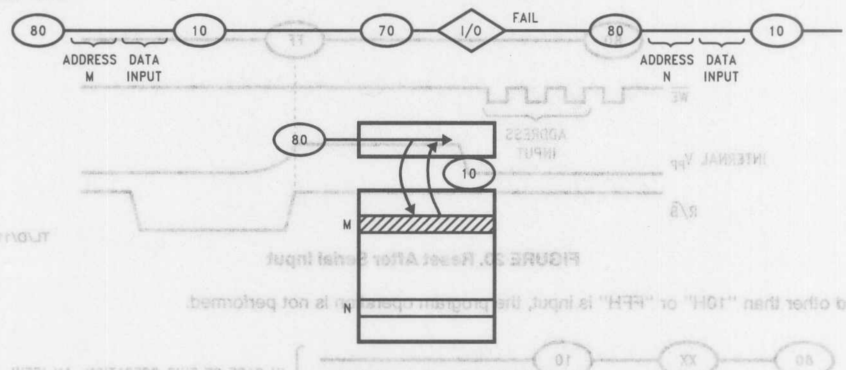
Therefore, the device status needs to be checked to see whether or not the "B0H" command has been accepted by issuing a "70H" command after the device goes to ready.

The device responds as follows when a "D0H" command (Resume) is input instead of "70H".

- — "B0H" has been accepted : Erase operation is executed. (The device is busy.)
- — "B0H" has not been accepted. (Erase operation has been completed) : "D0H" command cannot be accepted. (The device is in ready.)

Each case above is confirmed by monitoring the R/$\overline{B}$ signal.

(6) PROGRAM FAIL



TL/D/11915–55

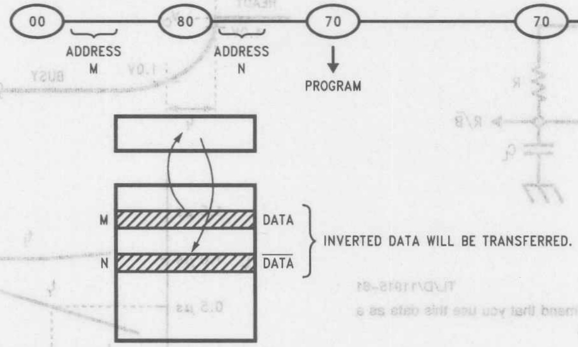
FIGURE 21. Program Fail

When the programming result for the page address M is "Fail", do not try to program the page to address N in another block. Because the previous input data is lost, the same sequence of "80H" command, address and data input is necessary.

Supplementary Device Operation (Continued)

(7) DATA TRANSFER

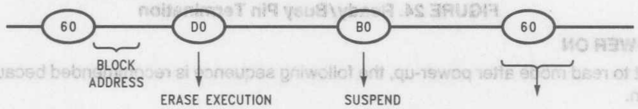
The data in page Address M cannot be automatically transferred to page address N. If the following sequence is executed, the data will be inverted (i.e., "1" data will become "0" and "0" will become "1").



TL/D/11915-56

FIGURE 22. Page to Page Transfer

(8) BLOCK ERASE AFTER SUSPEND COMMAND "B0H"

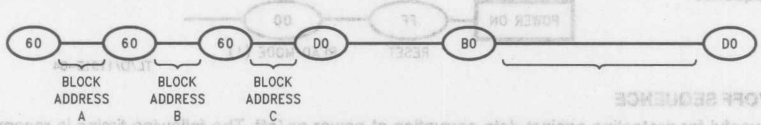


TL/D/11915-57

A block erase command is prohibited when the device has been suspended by inputting "B0H" during a block erase or multi-block erase operation. Only a program or read operation is allowed during this erase suspend interruption.

(9) INTERRUPTION OF AN ERASING BLOCK

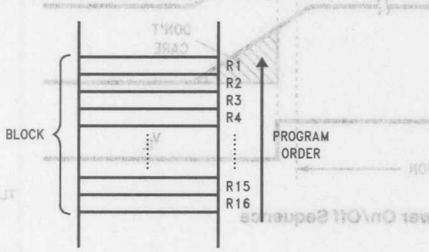
After a "B0H" command input, neither a program nor a read operation is allowed for the accessed block which is currently in an erase operation.



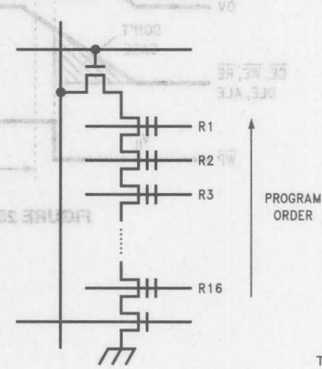
TL/D/11915-58

(10) ADDRESSING FOR PROGRAM OPERATION

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block (i.e., Row 16 must be programmed before row 15, etc.). Random page address input is prohibited. Programming must be executed in order from the NAND cell transistor closest to ground to the one closest to the bit line. Refer to the diagram below.



TL/D/11915-59



Correspondence of internal and external address

NAND address $\longrightarrow$ A_8–A_{11} $\begin{cases} 000\text{: R16} \\ \downarrow \\ 111\text{: R1} \end{cases}$

TL/D/11915-60

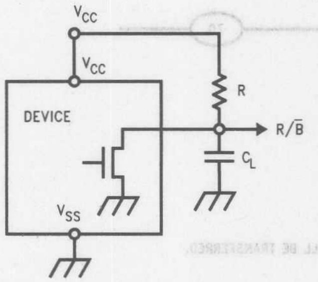
FIGURE 23. Page Program in Order within a Block

The order of the external address from A_8 to A_{11} corresponds to the device internal page address from R16 to R1.

Supplementary Device Operation (Continued)

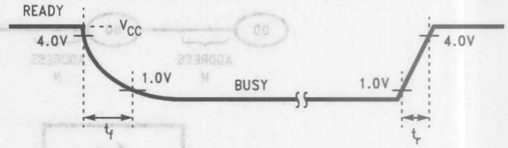
(11) R/B̄: TERMINATION FOR THE READY/BUSY PIN (R/B̄)

A pull-up resistor needs to be used for termination because the R/B̄ buffer consists of an open drain circuit.

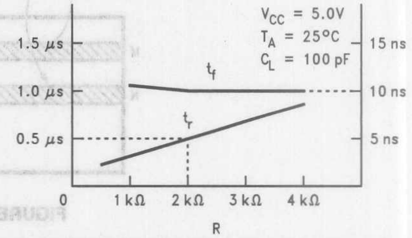


TL/D/11915-61

This data may vary by device. We recommend that you use this data as a reference when selecting a resistor value.



TL/D/11915-62



TL/D/11915-63

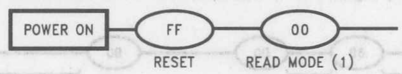
FIGURE 24. Ready/Busy Pin Termination

(12) STATUS AFTER POWER ON

Although the device is set to read mode after power-up, the following sequence is recommended because each input signal may not be stable at power on.

- Operation mode : Read mode (1)
- Address register : All "0"
- Data register : Indeterminacy
- High voltage generation circuit : Off state

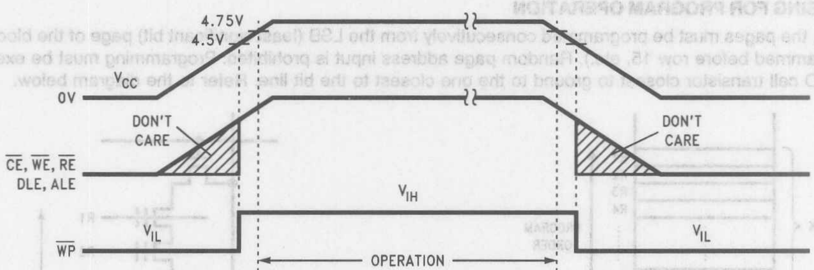
Recommended sequence



TL/D/11915-64

(13) POWER ON/OFF SEQUENCE

The W̄P̄ signal is useful for protecting against data corruption at power on/off. The following timing is recommended:



TL/D/11915-65

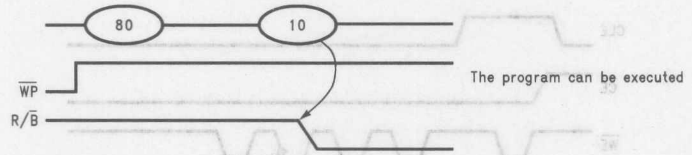
FIGURE 25. NM29N16 Power On/Off Sequence

Supplementary Device Operation (Continued)

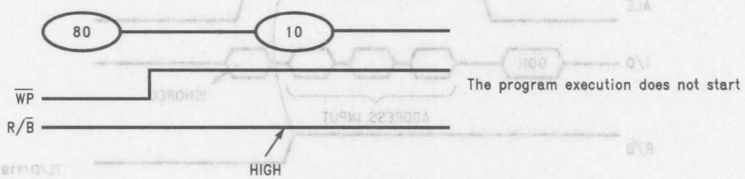
(14) NOTIFICATION FOR $\overline{WP}$ SIGNAL

The erase and program operations are reset when $\overline{WP}$ goes low. The following conditions must be recognized:

Program

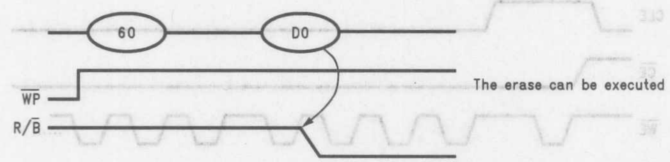


TL/D/11915-66

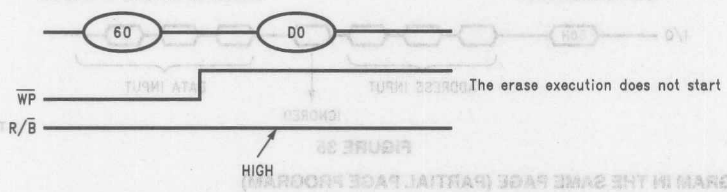


TL/D/11915-67

Erase

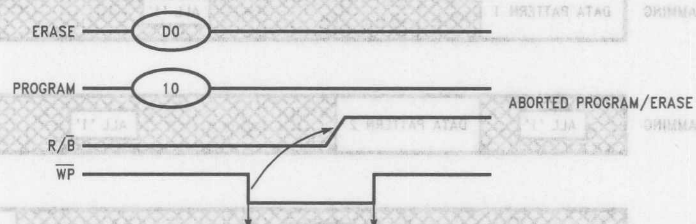


TL/D/11915-68



TL/D/11915-69

In the case that $\overline{WP}$ goes high during erase/program operation



TL/D/11915-70

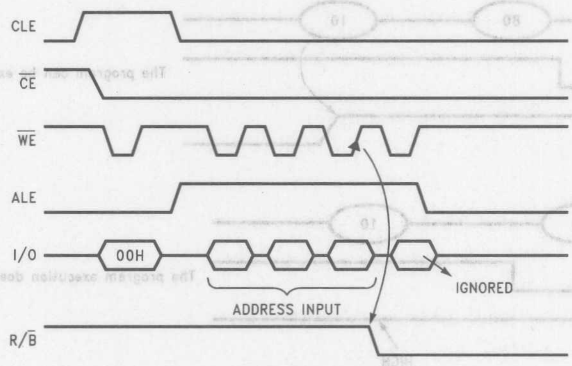
The previous operation is reset even when $\overline{WP}$ returns to high level and the device waits for the next command. The same loading sequence as after the reset command is needed to restart the operation.

Supplementary Device Operation (Continued)

(15) IN THE CASE THAT 4 ADDRESS CYCLES ARE INPUT

Although the device may acquire the fourth address, it is ignored inside the chip.

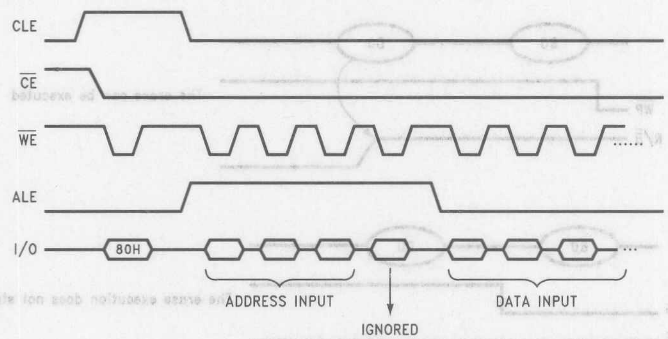
At Read operation:



TL/D/11915–71

FIGURE 34

At programming operation:

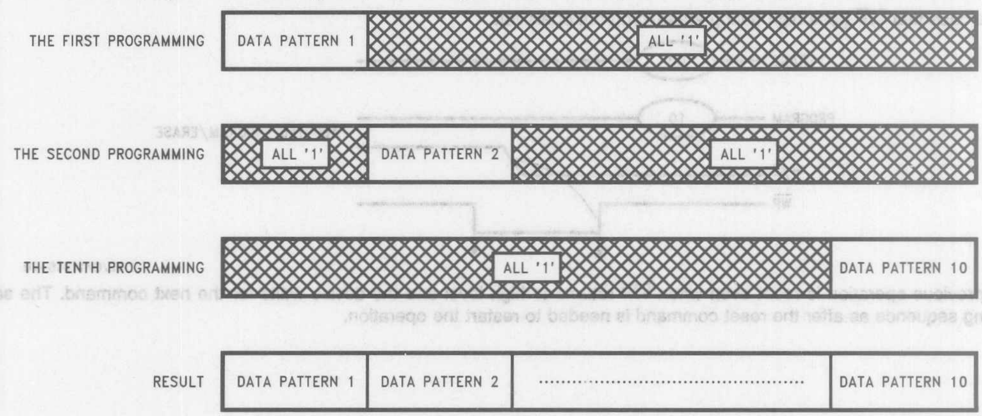


TL/D/11915–72

FIGURE 35

(16) DIVIDED PROGRAM IN THE SAME PAGE (PARTIAL PAGE PROGRAM)

The device allows a page to be divided typically into 10 segments and to program each page segment selectively as follows:



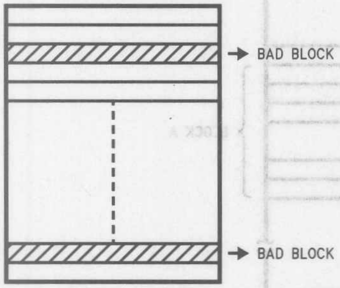
TL/D/11915–73

FIGURE 36

Note: The input data of unprogrammed or previously programmed page segments must be "1". (i.e., Mask all page bytes outside the segment to be programmed with "1" data.)

blocks must be identified by user software during initial op-eration. Do not try to access bad blocks. A bad block does not affect the performance of good blocks because it is isolated from the bit line by the select gate. The valid number of blocks is as follows:

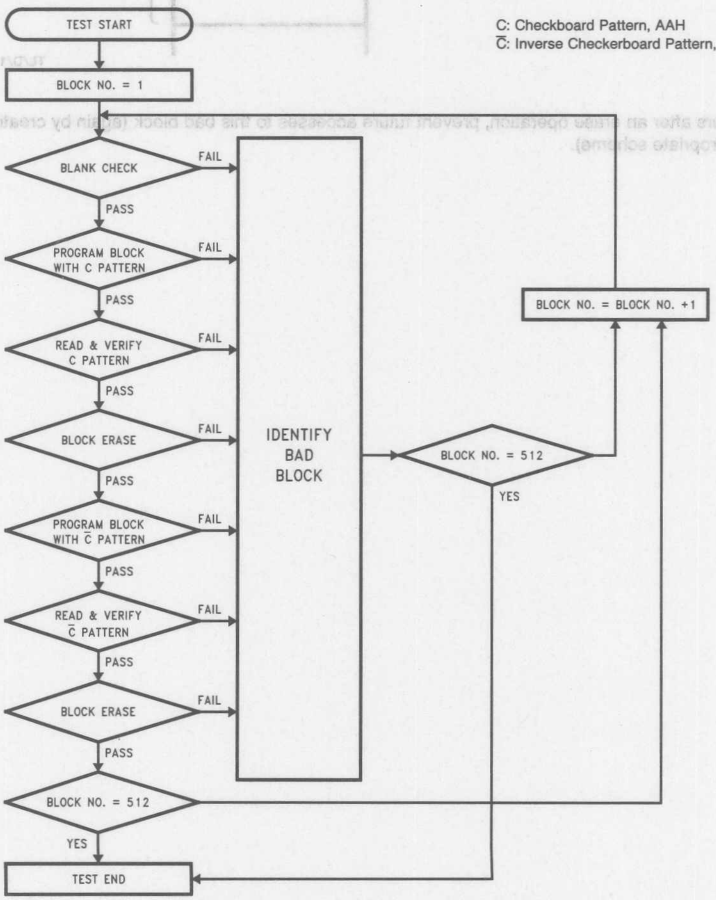
	Min	Typ	Max	Unit
Number of good blocks	502	508	512	Block



TL/D/11915-83

C: Checkboard Pattern, AAH

$\overline{C}$: Inverse Checkerboard Pattern, 55H



TL/D/11915-4

FIGURE 37. Identification of Bad Blocks

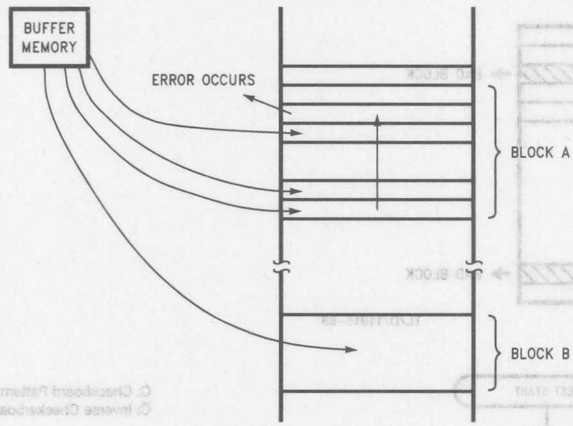
Supplementary Device Operation (Continued)

(18) ERROR IN PROGRAM OR ERASE OPERATION (FAIL AT STATUS READ)

The device may fail during a program or erase operation due to exceeding write/erase cycle limits, for example. The following system architecture will enable high system reliability if a failure occurs:

Program

When the error happens in Block A, try to reprogram the data into another Block B by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a "bad block" table or other appropriate scheme).



TL/D/11915-75

Erase

When the error oocurs after an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme).

Section 2

CMOS EEPROMs

2

Section 2 Contents

National Semiconductor

MICROWIRE™ CMOS EEPROM Selection Guide

General Description

National Semiconductor offers a family of CMOS EEPROMs which share the following features: MICROWIRE Serial Interface, floating gate M²CMOS™ technology, extended voltage (2.5V–5.5V) R/W range or 5V R/W only, Direct-write, and self-timed programming cycle with programming status on the data out pin. All of these devices are offered in compatible packages and pinouts.

There are also several features not shared by all family members, which separate the family into three groups. These features are **operating voltage range, write protection,** and **sequential register read.** Other differences are memory size, packaging, and operating temperature range. Although, for the purpose of this selection guide, the family will not be separated by these differences, as each individual device is available with all of these value added options.

Features

- 40 year data retention
- Extended voltage operation
- Endurance: 10^6 data changes
- Reliable CMOS floating gate technology
- Single voltage operation in all modes
- MICROWIRE compatible serial interface
- Directwrite, no erase cycles required
- Self-timed programming cycle
- Device status signal during programming mode
- Sequential Register Read*
- User configurable write protection*

*Features available on NM93CS only.

Available Product

	Packages	Temperature Ranges	4.5V–5.5V	2.0V–6.0V	1V–8V
NM93CS06	N, M8	C, E	Y	Y	
NM93CS46	N, M8	C, E	Y	Y	
NM93CS56	N, M8	C, E	Y	Y	
NM93CS66	N, M8	C, E	Y	Y	
NM93C06	N, M8	C, E	Y	Y	Y
NM93C13	N, M8	C	Y		
NM93C46	N, M8	C, E	Y	Y	Y
NM93C14	N, M8	C	Y		
NM93C56	N, M8	C, E	Y	Y	
NM93C66	N, M8	C, E	Y	Y	

*For Mil. Temp. Range Contact your Sales Office

**1V–8V is available for the NM93C06XLZ/NM93C46XLZ in the commercial temp. range only (0 to +70°C).

NM 93 C S 06 X L Z E M8

- NM — National Memory
- 93 — Microwire Interface
- C — CMOS
- S — Features
  - No Entry = Standard
  - S = User programmable write protection and sequential read
- 06 — Memory Size
  - 06/13 = 256 bit
  - 46/14 = 1024 bit
  - 56 = 2048 bit
  - 66 = 4096 bit
- X — X = 1.8V Read/Write
- L — Operating Voltage Range
  - L = 2.0V to 5.5V
  - No Entry = 4.5V to 5.5V
- Z — Zero Standby Current
  - Z = <1 μA Standby Current
- E — Operating Temperature Range
  - No Entry = 0°C to +70°C
  - E = −40°C to +85°C
  - M = −55°C to +125°C
- M8 — Package
  - N = Plastic DIP
  - J = Ceramic DIP
  - M = 14 Lead SO
  - M8 = 8 Lead SO

SPECIALTY Products CMOS EEPROM Selection Guide

General Description

National Semiconductor offers a full line of CMOS EEPROMs. Some share the MICROWIRE™ Serial Interface such as the NM93C06 and the NM93CS06; others share the I²C (2-wire) Interface such as the NM24C02 and the NM24C08. In addition to the above EEPROMs, we also offer some specialty EEPROMs.

These include the NM95C12, NM93C46A and the NM25C04 EEPROMs.

Features

- No erase necessary
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Reliable CMOS floating gate technology

The **NM95C12** is a 976-bit CMOS EEPROM with 8 programmable outputs that can be used as switches, i.e., DIP or analog. The 976 bits of memory are divided into 61 registers of 16 bits each with each register individually accessible. Registers 61–63 are dedicated for DIP switch functions. The NM95C12 contains 8 individually programmable outputs which can be used as switches.

The **NM25C04** is 4096 bits of CMOS EEPROM with an SPI-interface. The device is designed to seamlessly interface with the 68HCXX family of Motorola microcontrollers.

The **NM93C46A** is 1024 bits of CMOS EEPROM which can be organized as either 64 16-bit registers or as 128 8-bit registers. The NM93C46A shares the MICROWIRE Interface and the x8 and x16 configuration. The differentiating feature is in the pin configuration: The NM93C46A's Program/Erase status is output on the Data-Out (DO) pin. The device uses a low to high transition on the clock (SK) to clock all data into or out of the device, except device programming status which is independent of the clock.

Available Product

	Packages	Temperature Ranges	4.5V–5.5V	2.5V–5.5V
NM95C12	N, M	C, E	Y	
NM93C46A	N, M8	C, E	Y	Y
NM25C04	N, M	C, E		Y

National Semiconductor

NM93C06/C46/C56/C66 256-/1024-/2048-/4096-Bit Serial EEPROM (MICROWIRE™ Bus Interface)

General Description

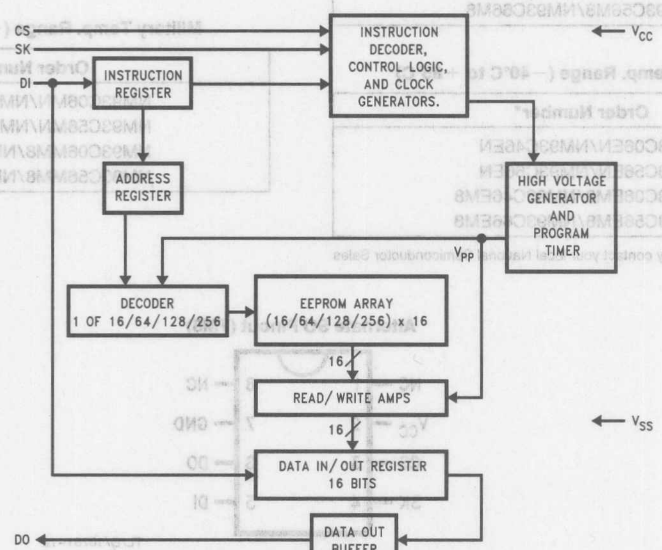
The NM93C06/C46/C56/C66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in an SO package for small space considerations.

The EEPROM Interfacing is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- Device status during programming mode
- Typical active current of 400 μA; Typical standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



TL/D/10751-1

2

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)

TL/D/10751–2

Top View

See NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number*
NM93C06N/NM93C46N NM93C56N/NM93C66N NM93C06M8/NM93C46M8 NM93C56M8/NM93C66M8

Alternate (Turned) SO Pinout

Order Number
NM93C06TM8/NM93C46TM8/NM93C56TM8 NM93C06TEM8/NM93C46TEM8/NM93C56TEM8

Extended Temp. Range (−40°C to +85°C)

Order Number*
NM93C06EN/NM93C46EN NM93C56EN/NM93C66EN NM93C06EM8/NM93C46EM8 NM93C56EM8/NM93C66EM8

Military Temp. Range (−55°C to +125°C)

Order Number*
NM93C06MN/NM93C46MN NM93C56MN/NM93C66MN NM93C06MM8/NM93C46MM8 NM93C56MM8/NM93C66MM8

*For 14-Pin SO availability contact your local National Semiconductor Sales Office.

Alternate SO Pinout (TM8)

TL/D/10751–12

See NS Package M08A

Office/Distributors for availability and specifications.			NM93C06E–NM93C66E	−40°C to +85°C
Ambient Storage Temperature	−65°C to +150°C		NM93C06M–NM93C66M	−55°C to +125°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V		Power Supply (V_{CC})	4.5V to 5.5V
Lead Temp. (Soldering, 10 sec.)	+300°C			
ESD Rating	2000V			

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified

Note: Throughout this table, "M" refers to temperature range (−55°C to +125°C), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	CS = V_{IH}, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		1 1 1	mA
I_{CCS}	Standby Current	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	CS = V_{IL}		50 50 100	μA μA μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	(Note 5)	0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M		250 300 500		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	(Note 2)	250 250 500		ns

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M		50 50 100		ns
t_{DH}	D0 Hold Time			70		ns
t_{DIS}	DI Setup Time	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M		100 200 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M			500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M			500 500 1000	ns
t_{SV}	CS to Status Valid	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M			500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C06-NM93C66 NM93C06E-NM93C66E NM93C06M–NM93C66M	CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 3)

T_A = 25°C f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (This is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/0.4 mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

The NM93C06/C46/C56/C66 devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

All Data in signals are clocked into the device on the low-to-high SK transition.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable WEN instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the selected register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

NOTE: The NSC CMOS EEPROMs do not require an 'ERASE' or 'ERASE ALL' operation prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C06 and NM93C46

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, at specified address.
WEN	1	00	11XXXX		Enable all programming modes.
ERASE	1	11	A5–A0		Erase selected register.
WRITE	1	01	A5–A0	D15–D0	Writes selected register.
ERAL	1	00	10XXXX		Erases all registers.
WRALL	1	00	01XXXX	D15–D0	Writes all registers.
WDS	1	00	00XXXX		Disables all programming modes.

Note: Address bits A5 and A4 become "Don't Care" for the NM93C06.

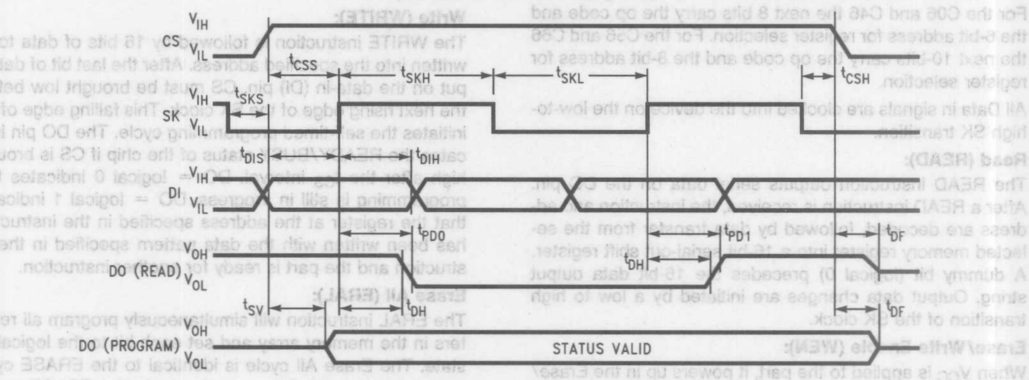
Instruction Set for the NM93C56 and NM93C66

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory, at specified address.
WEN	1	00	11XXXXXX		Enable all programming modes.
ERASE	1	11	A7–A0		Erase selected register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRITE	1	01	A7–A0	D15–D0	Writes selected register.
WRALL	1	00	01XXXXXX	D15–D0	Writes all registers.
WDS	1	00	00XXXXXX		Disables all programming modes.

Note: Address bit A7 becomes "Don't Care" for the NM93C56.

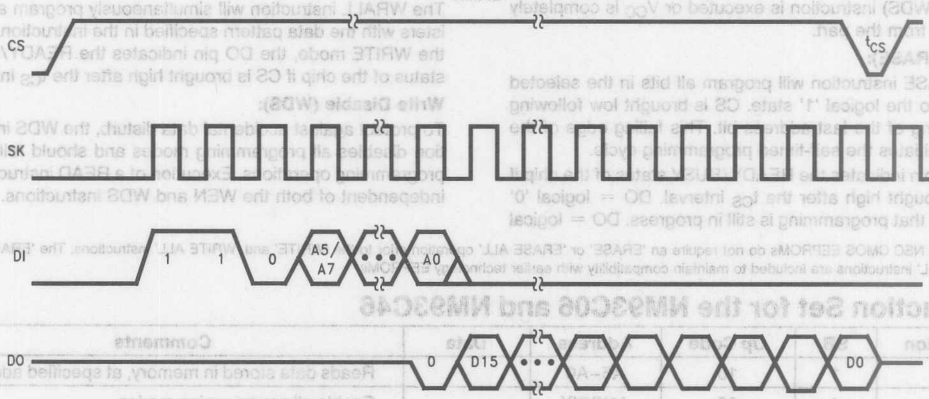
Timing Diagrams

Synchronous Data Timing



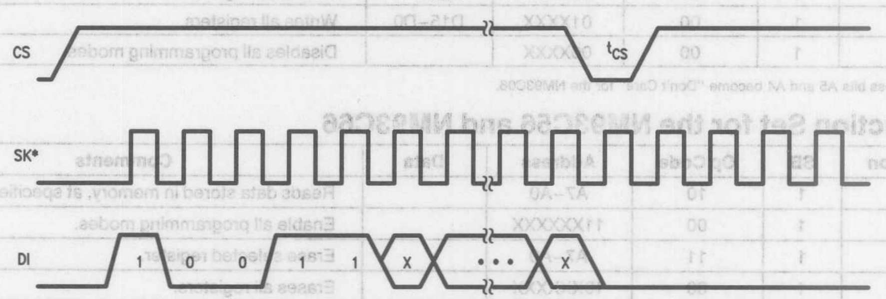
TL/D/10751-4

READ



TL/D/10751-5

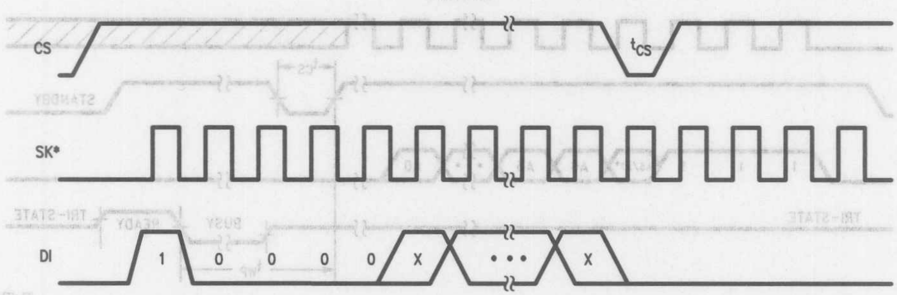
WEN



TL/D/10751-6

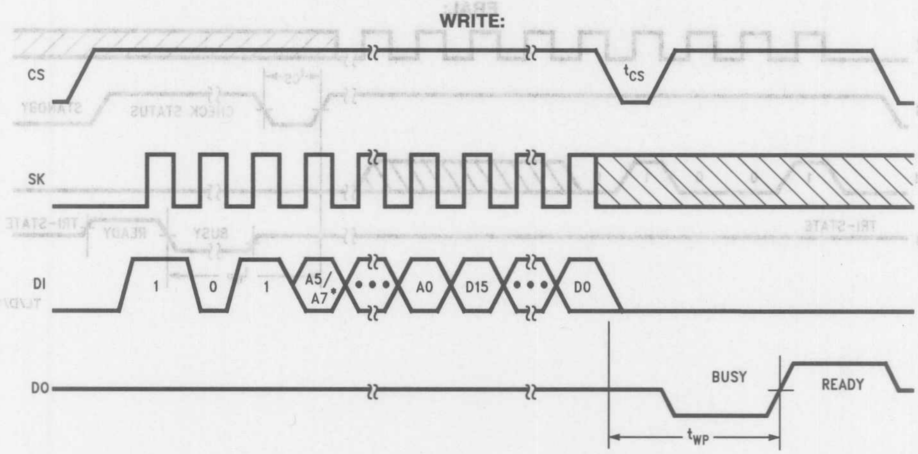
Timing Diagrams (Continued)

WDS:



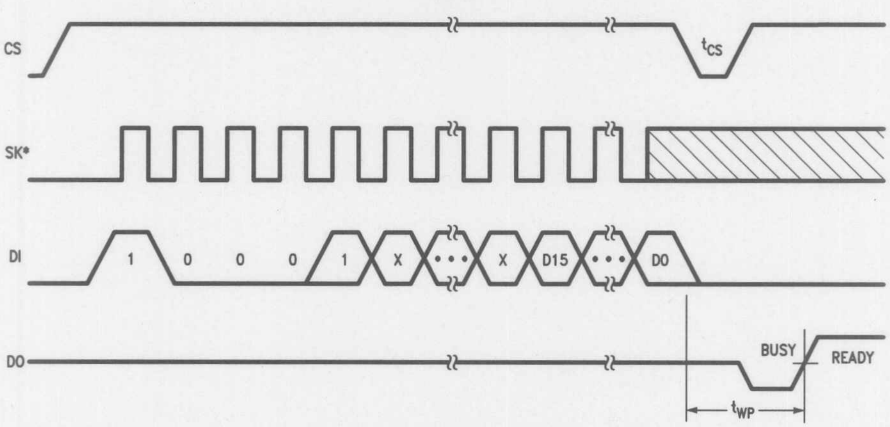
TL/D/10751-7

WRITE:



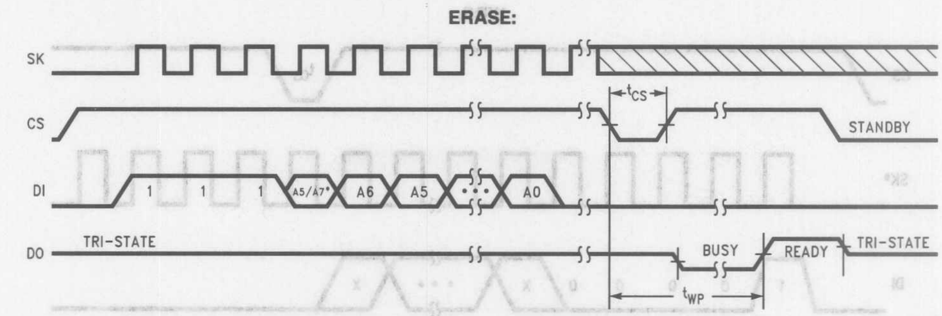
TL/D/10751-8

WRALL:

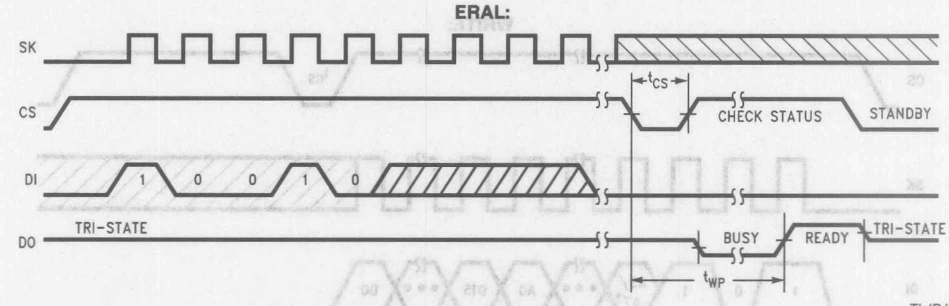


TL/D/10751-9

Timing Diagrams (Continued)



TL/D/10751–10



TL/D/10751–11

NM93CS06/CS46/CS56/CS66 (MICROWIRE™ Bus Interface) 256-/1024-/2048-/4096-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

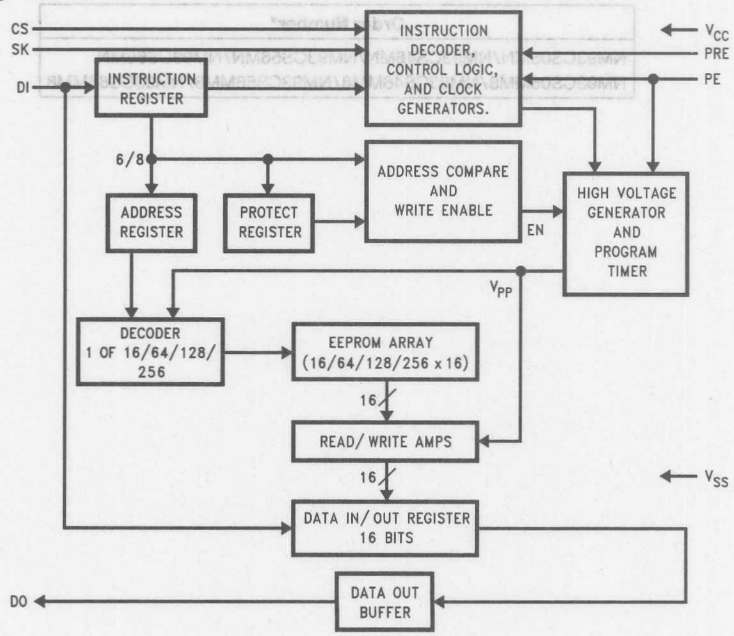
The NM93CS06/CS46/CS56/CS66 devices are 256/1024/2048/4096 bits, respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. Selected registers can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification (all registers greater than, or equal to, the selected address are then protected from further change). Additionally, this address can be "locked" into the device, making all future attempts to change data impossible. These devices are fabricated using National Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption. The NM93CSXX Family is offered in an SO package for small space considerations.

The EEPROM interfacing is MICROWIRE compatible providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory, and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PRENABLE, PRCLEAR, and PRDISABLE.

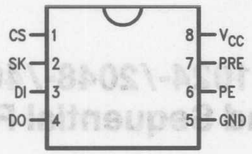
Features

- Write protection in a user defined section of memory
- Sequential register read
- Typical active current of 400 μA and standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: 10^6 data changes
- 4.5V to 5.5V operation in all modes of operation
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



TL/D/10750–1



TL/D/10750-2

Top View

NS Package Number
N08E and M08A

SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number*
NM93CS06N/NM93CS46N/NM93CS56N/NM93CS66N
NM93CS06M8/NM93CS46M8/NM93CS56M8/NM93CS66M8

Extended Temp. Range (−40°C to +85°C)

Order Number*
NM93CS06EN/NM93CS46EN/NM93CS56EN/NM93CS66EN
NM93CS06EM8/NM93CS46EM8/NM93CS56EM8/NM93CS66EM8

Military Temp. Range (−55°C to +125°C)

Order Number*
NM93CS06MN/NM93CS46MN/NM93CS56MN/NM93CS66MN
NM93CS06MM8/NM93CS46MM8/NM93CS56MM8/NM93CS66MM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	$-65°C$ to $+150°C$
All Input or Output Voltages with Respect to Ground	$+6.5V$ to $-0.3V$
Lead Temperature (Soldering, 10 sec.)	$+300°C$
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CSxx	$0°C$ to $+70°C$
NM93CSxxE	$-40°C$ to $+85°C$
NM93CSxxM	$-55°C$ to $+125°C$
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Throughout this table, "M" refers to temperature range ($-55°C$ to $+125°C$), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	CS = V_{IH}, SK = 1.0 MHz SK = 1.0 MHz SK = 0.5 MHz		1 1 1	mA
I_{CCS}	Standby Current	NM93CS06–NM93CS66 NM93CS06E–NM93CS06E NM93CS06M–NM93CS06M	CS = V_{IL}		50 50 100	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)		± -1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 $V_{CC}+1$	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 $V_{CC}-0.2$	0.2	V
f_{SK}	SK Clock Frequency	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	(Note 5)	0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M		250 300 500		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS goes high	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	(Note 2)	250 250 500		ns
t_{CSS}	CS Setup Time			100		ns
t_{PRES}	PRE Setup Time	NM93CS06-NM93CS66 NM93CS06E-NM93CS66E NM93CS06M–NM93CS66M		50 50 100		ns
t_{DH}	DO Hold Time			10		ns
t_{PES}	PE Setup Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M		50 50 100		ns
t_{DIS}	DI Setup Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M		100 100 200		ns
t_{CSH}	CS Hold Time			0		ns

2

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PEH}	PE Hold Time	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M		250 250 500		ns
t_{PREH}	PRE Hold Time			50		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M			500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M			500 500 1000	ns
t_{SV}	CS to Status Valid	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M			500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93CS06–NM93CS66 NM93CS06E–NM93CS66E NM93CS06M–NM93CS66M	CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 3)

T_A = 25°C, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (this is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH\,(minimum)} + t_{SKL\,(minimum)}$ for shorter SK cycle time operation.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/ 0.4 mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

vice on the low-to-high SK transition.

Read and Sequential Register Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **sequential register read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction, however, after loading the WRITE instruction the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Write All (WRALL):

The WRALL instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction, however, after loading the instruction the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. This function is DISABLED if the Protect Register is in use to lock out a section of memory.

Write Disable (WDS):

To protect against accidental data disturb, the Write Disable (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

EEPROM array, rather than the Protect Register.

Protect Register Read (PRREAD):

The PRREAD instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction sequence. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

Protect Register Enable (PREN):

The PREN instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction sequence.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The PRCLEAR instruction clears the address stored in the Protect Register and, therefore, enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction sequence, however, after loading the PRCLEAR instruction the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Please note that the PRCLEAR instruction and the PRWRITE instruction will both program the Protect Register with all 1s. However, the PRCLEAR instruction will allow the LAST register to be programmed, whereas the PRWRITE instruction = all 1s will PREVENT the last register from being programmed. In addition, the PRCLEAR instruction will allow the use of the WRALL command, where the PRWRITE = all 1s will lock out the Bulk programming opcode.

Protect Register Write (PRWRITE):

The PRWRITE instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction the Protect Register must first be cleared by executing a PRCLEAR operation and that the PRE and PE pins **must** be held high while loading the instruction, however, after loading the PRWRITE instruction the PRE and PE pins become 'don't care'. Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The PRDS instruction is a **ONE** TIME ONLY instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Instruction Set for the NM93CS06 and NM93CS46

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Enable all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered.

Note: Address bits A5 and A4 become "Don't Care" for the NM93CS06.

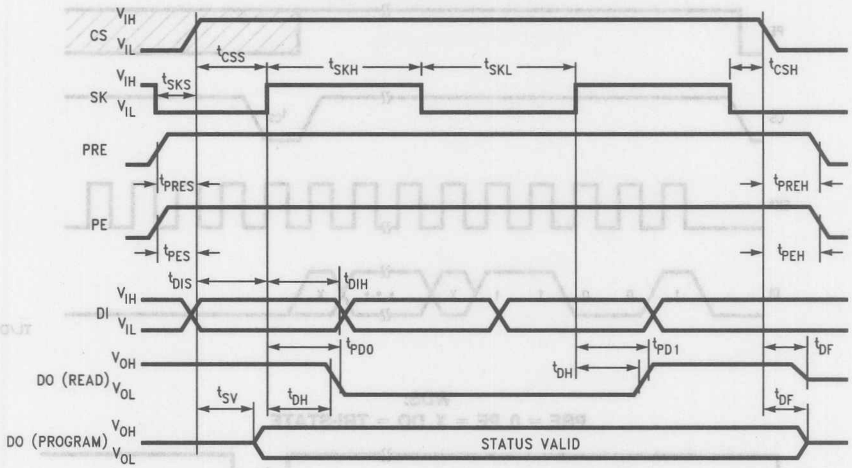
Instruction Set for the NM93CS56 and NM93CS66

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Enable all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	ONE TIME ONLY instruction after which the address in the Protect Register cannot be altered.

Note: Address bit A7 becomes "Don't Care" for the NM93CS56.

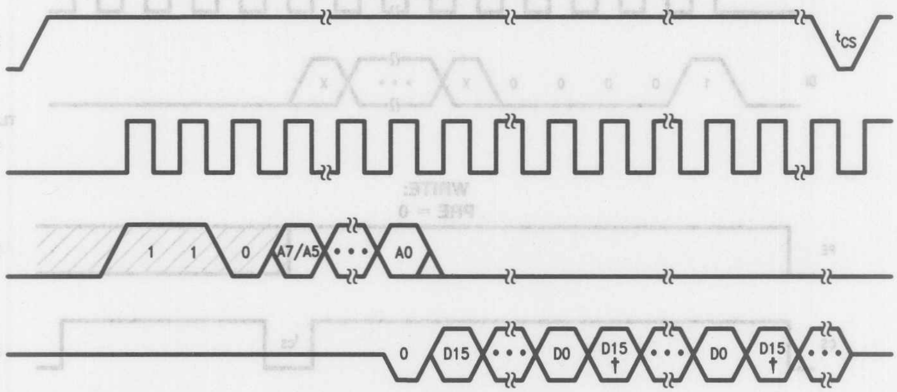
Timing Diagrams

Synchronous Data Timing



TL/D/10750–15

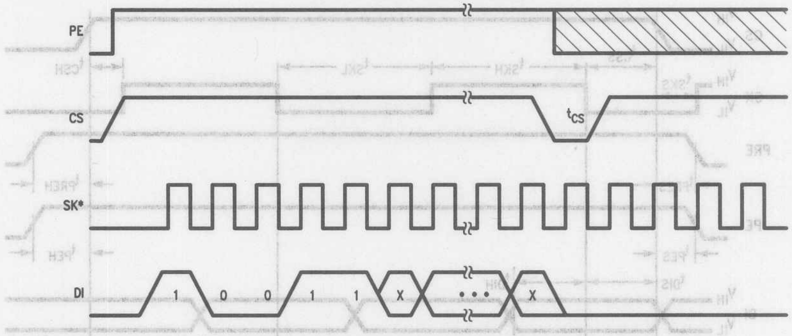
READ:
PRE = 0, PE = X



†The memory automatically cycles to the next register with continued clocking of SK.

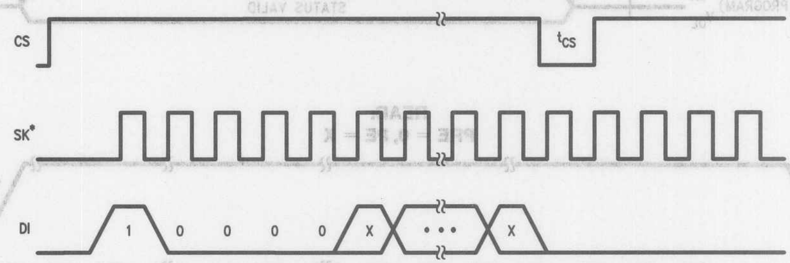
TL/D/10750–4

PRE = 0, DO = TRI-STATE



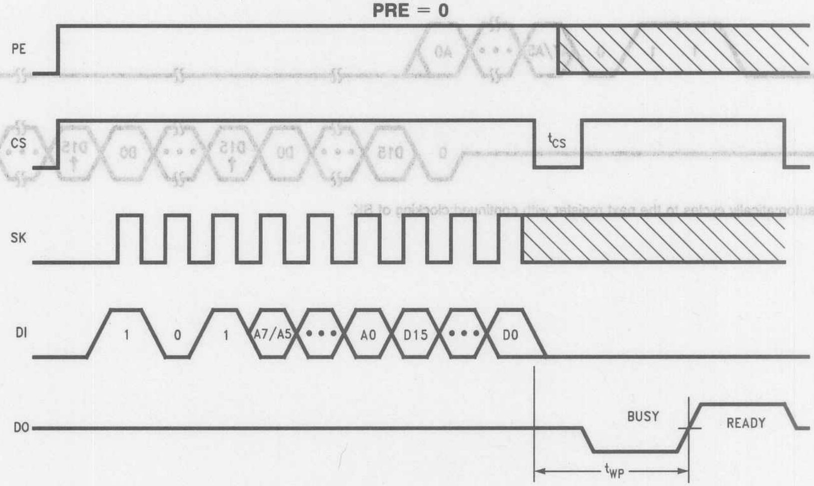
TL/D/10750-5

WDS:
PRE = 0, PE = X, DO = TRI-STATE

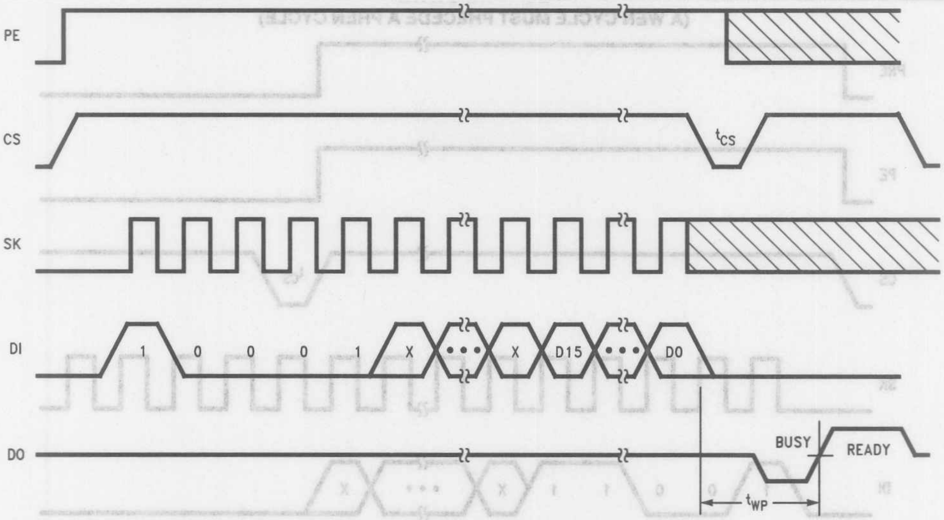


TL/D/10750-6

WRITE:
PRE = 0

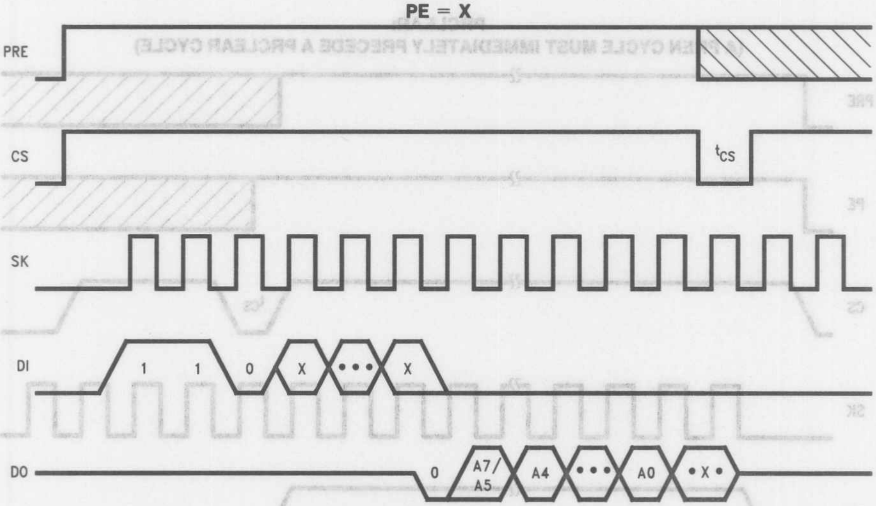


TL/D/10750-7



TL/D/10750-8

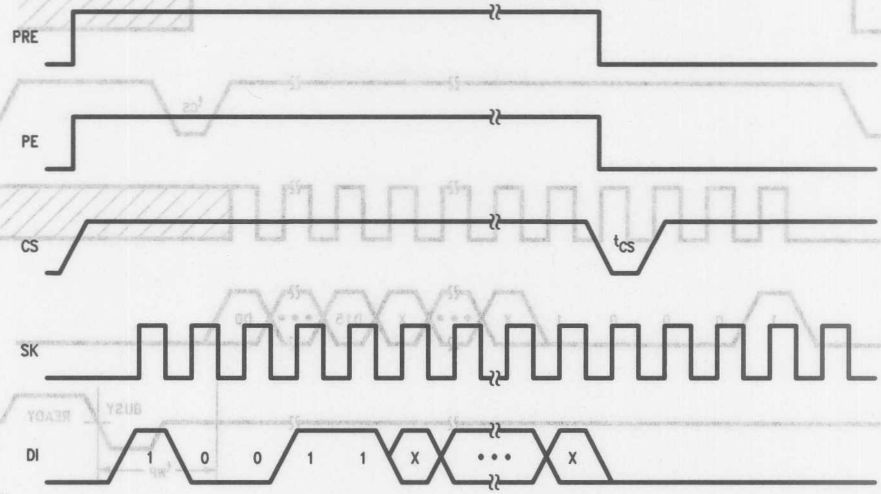
PRREAD:
PE = X



TL/D/10750-9

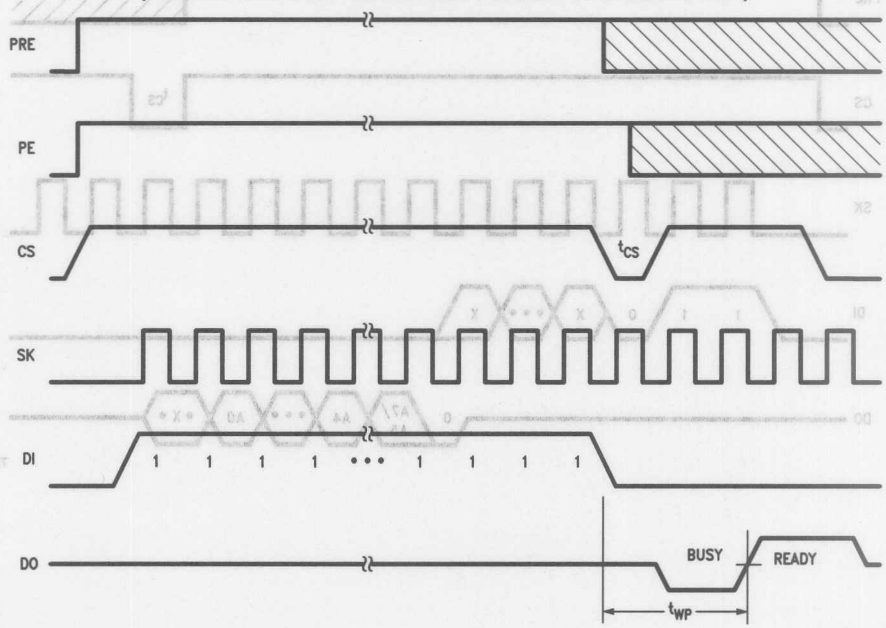
Timing Diagrams (Continued)

PREN:
D0 = TRI-STATE
(A WEN CYCLE MUST PRECEDE A PREN CYCLE)



TL/D/10750–10

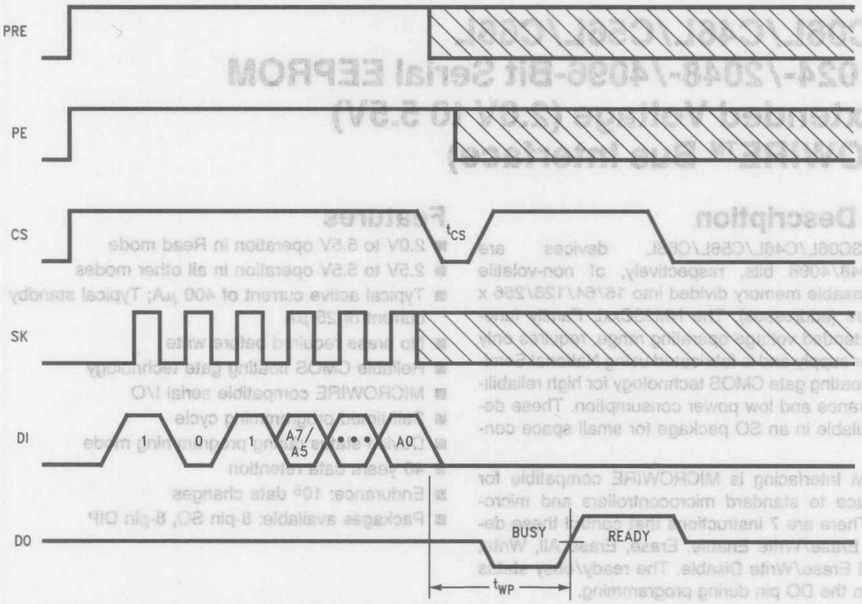
PRCLEAR:
(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRCLEAR CYCLE)



TL/D/10750–11

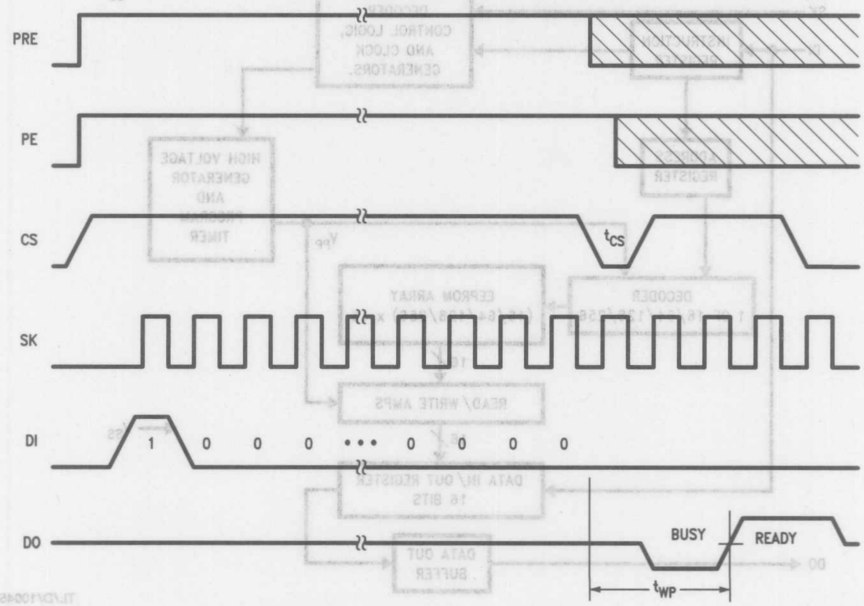
Timing Diagrams (Continued)

PRWRITE:
(PREN CYCLES MUST IMMEDIATELY PRECEDE A PRWRITE CYCLE.)



TL/D/10750–12

PRDS:
(*ONE TIME ONLY INSTRUCTION. A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRDS CYCLE.)



TL/D/10750–13

2

NM93C06L/C46L/C56L/C66L 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.0V t0 5.5V) (MICROWIRE™ Bus Interface)

General Description

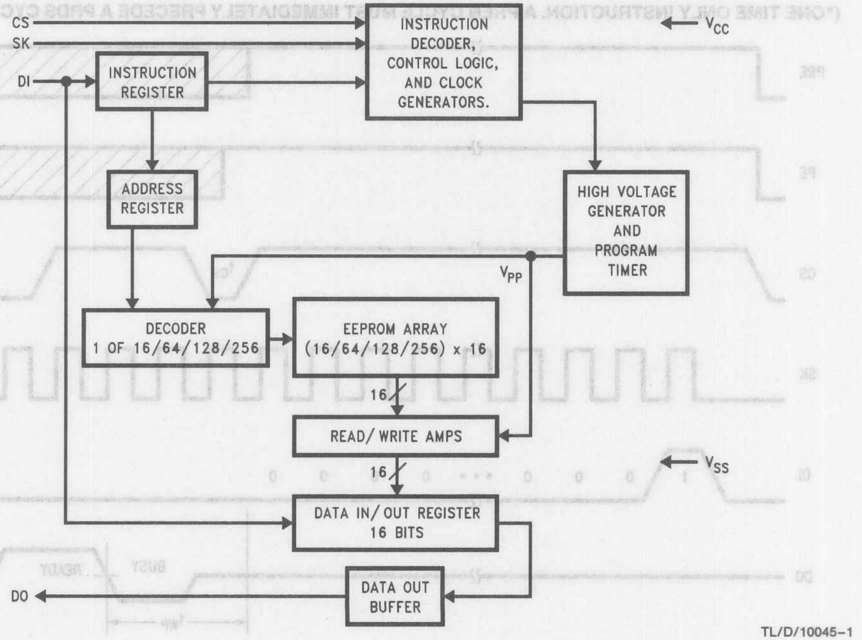
The NM93C06L/C46L/C56L/C66L devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CxxL Family functions in an extended voltage operating range, requires only a single power supply and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. These devices are available in an SO package for small space considerations.

The EEPROM Interfacing is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- 2.0V to 5.5V operation in Read mode
- 2.5V to 5.5V operation in all other modes
- Typical active current of 400 μA; Typical standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



TL/D/10045–1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)

TL/D/10045–2

Top View

NS Package Number N08E or M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C06LN/NM93C46LN NM93C56LN/NM93C66LN NM93C06LM8/NM93C46LM8 NM93C56LM8/NM93C66LM8

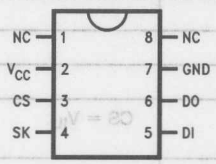
Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C06LEN/NM93C46LEN NM93C56LEN/NM93C66LEN NM93C06LEM8/NM93C46LEM8 NM93C56LEM8/NM93C66LEM8

Alternate (Turned) SO Pinout

Order Number
NM93C06TLM8/NM93C46TLM8/NM93C56TLM8 NM93C06TLEM8/NM93C46TLEM8/NM93C56TLEM8

Alternate SO Pinout (TM8)



TL/D/10045–12

NS Package Number M08A

2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06L–NM93C66L	0°C to +70°C
NM93C06LE–NM93C66LE	−40°C to +85°C
Power Supply (V_{CC}) Range	
Read Mode	2.0V to 5.5V
Bulk (ERAL/WRALL) Programming	3.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics: 2V < V_{CC} < 4.5V

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250 kHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} + 1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}	0.1 V_{CC}	V
f_{SK}	SK Clock Frequency		(Note 5)	0	250	kHz
t_{SKH}	SK High Time			1		μs
t_{SKL}	SK Low Time			1		μs
t_{SKS}	SK Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS goes high	0.2		μs
t_{CS}	Minimum CS Low Time		(Note 2)	1		μs
t_{CSS}	CS Setup Time			0.2		μs
t_{DH}	DO Hold Time			10		ns
t_{DIS}	DI Setup Time			0.4		μs
t_{CSH}	CS Hold Time			0		μs
t_{DIH}	DI Hold Time			0.4		μs
t_{PD1}	Output Delay to "1"				2	μs
t_{PD0}	Output Delay to "0"				2	μs
t_{SV}	CS to Status Valid				1	μs
t_{DF}	CS to DO in TRI-STATE®		CS = V_{IL}		0.4	μs
t_{WP}	Write Cycle Time				15	ms

DC and AC Electrical Characteristics: $4.5V < V_{CC} < 5.5V$

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current		$CS = V_{IH}$, SK = 1 MHz		1	mA
I_{CCS}	Standby Current		$CS = V_{IL}$		50	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 $V_{CC} + 1$	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OL} = −10μA	 $V_{CC} - 0.2$	0.2	V
f_{SK}	SK Clock Frequency		(Note 5)	0	1	MHz
t_{SKH}	SK High Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS goes high	50		ns
t_{CS}	Minimum CS Low Time		(Note 2)	250		ns
t_{CSS}	CS Setup Time			50		ns
t_{DH}	DO Hold Time			10		ns
t_{DIS}	DI Setup Time	NM93C06L-NM93C66L NM93C06LE-NM93C66LE		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"				500	ns
t_{PD0}	Output Delay to "0"				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE		$CS = V_{IL}$		100	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 3)

$T_A = 25°C$, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (this is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/t_{SK} = t_{SKH\ (minimum)} + t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Levels	V_{OL}/V_{OH} Timing Levels	I_{OL}/I_{OH}
$2.0V \le V_{CC} < 4.5V$ (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	±10 μA
$4.5V \le V_{CC} \le 5.5V$ (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/0.4 mA

Output Load: 1 TTL Gate (C_L = 100 pF)

Functional Description

The NM93C06L/C46L/C56L/C66L device have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10-bits carry the op code and the 8-bit address for register selection.

Read (READ):

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN):

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable WEN instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part.

Erase (ERASE):

The ERASE instruction will program all bits in the selected register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL):

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" CS is brought high after the t_{CS} interval.

Write All (WRALL):

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS):

To protect against accidental data distrub, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: NSC CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C06L and NM93C46L

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory at specified address.
WEN	1	00	11XXXX		Enable all programming modes.
ERASE	1	11	A5–A0		Erase selected register.
WRITE	1	01	A5–A0	D15–D0	Writes selected register.
ERAL	1	00	10XXXX		Erases all registers.
WRALL	1	00	01XXXX	D15–D0	Writes all registers.
WDS	1	00	00XXXX		Disables all programming modes.

Note: Address bits A5 and A4 become "Don't Care" for the NM93C06L.

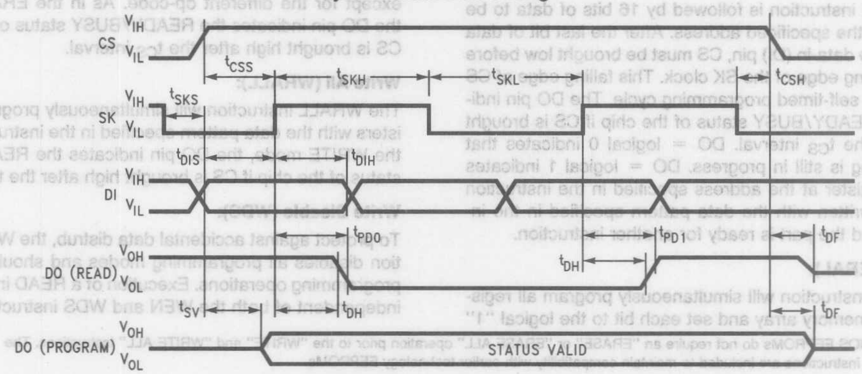
Instruction Set for the NM93C56L and NM93C66L

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Reads data stored in memory at specified address.
WEN	1	00	11XXXXXX		Enable all programming modes.
ERASE	1	11	A7–A0		Erase selected register.
WRITE	1	01	A7–A0	D15–D0	Writes selected register.
ERAL	1	00	10XXXXXX		Erases all registers.
WRALL	1	00	01XXXXXX	D15–D0	Writes all registers.
WDS	1	00	00XXXXXX		Disables all programming modes.

Note: Address bit A7 is "Don't Care" for the NM93C56L.

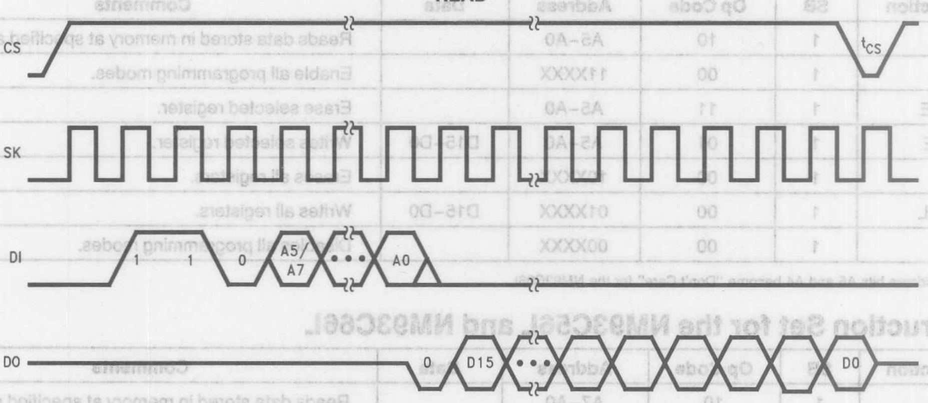
Timing Diagrams

Synchronous Data Timing



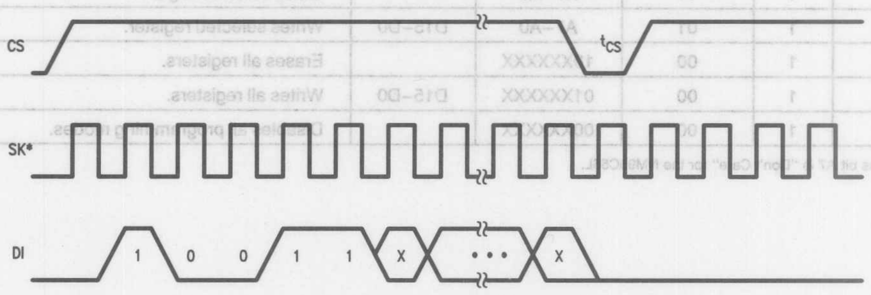
TL/D/10045-13

READ



TL/D/10045-5

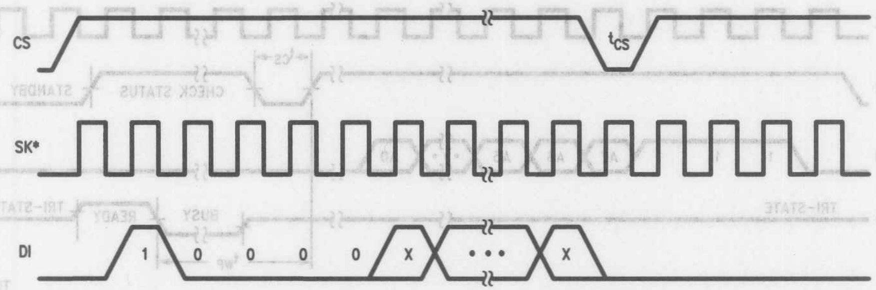
WEN



TL/D/10045-6

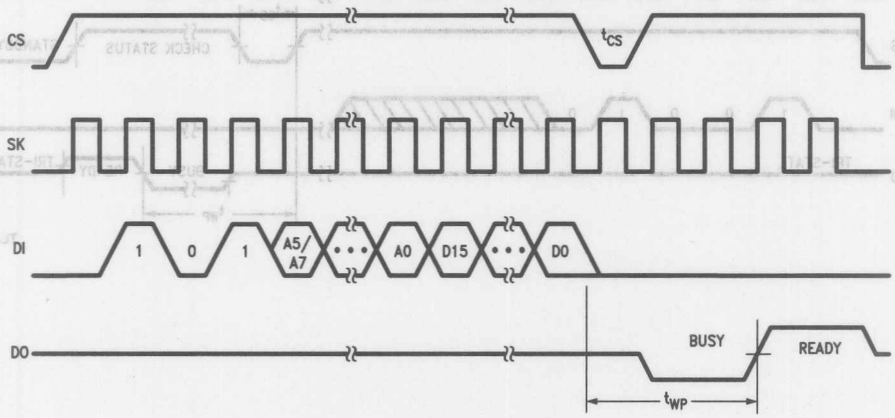
Timing Diagrams (Continued)

WDS



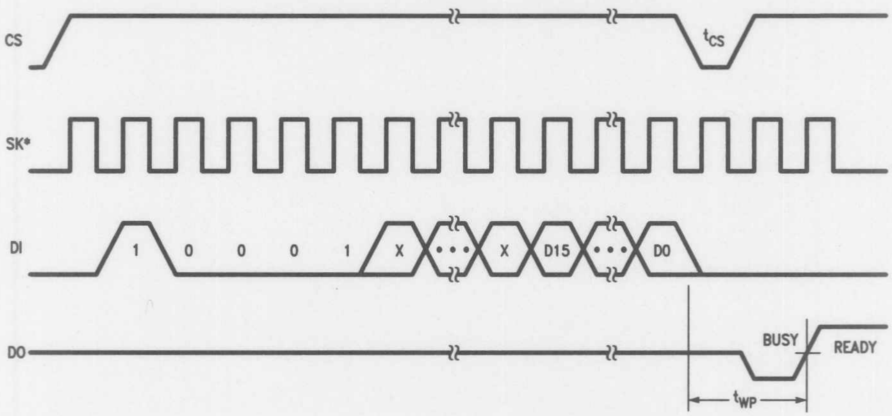
TL/D/10045–7

WRITE



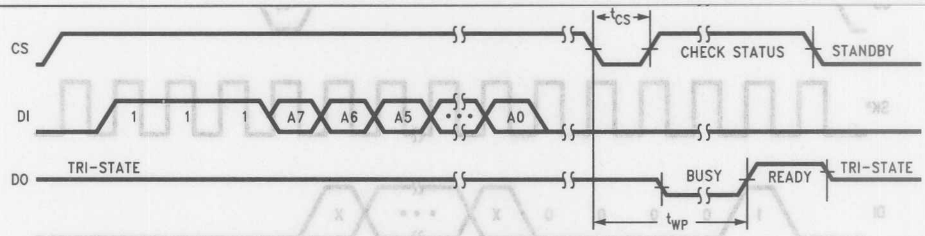
TL/D/10045–8

WRALL



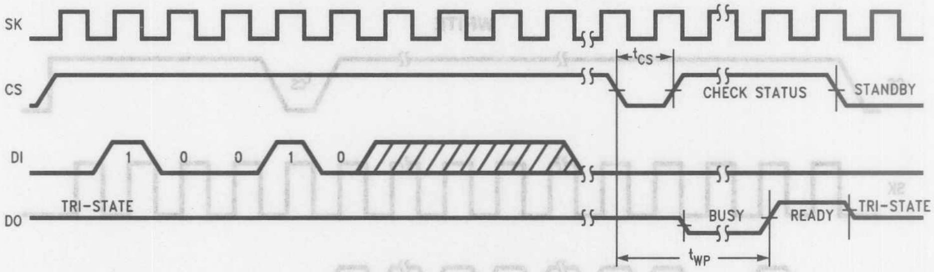
TL/D/10045–9

2



TL/D/10045-10

ERAL



TL/D/10045-11

National Semiconductor

NM93CS06L/CS46L/CS56L/CS66L 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.0V to 5.5V) and Data Protect (MICROWIRE™ Bus Interface)

General Description

The NM93CS06L/CS46L/CS56L/CS66L devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CSxxL Family functions in an extended voltage operating range, and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. N registers ($N \leq 16$, $N \leq 64$, $N \leq 128$, $N \leq 256$) can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification. (All registers greater than, or equal to, the selected address are then protected from further change.) Additionally, this address can be "locked" into the device, making all future attempts to change data impossible.

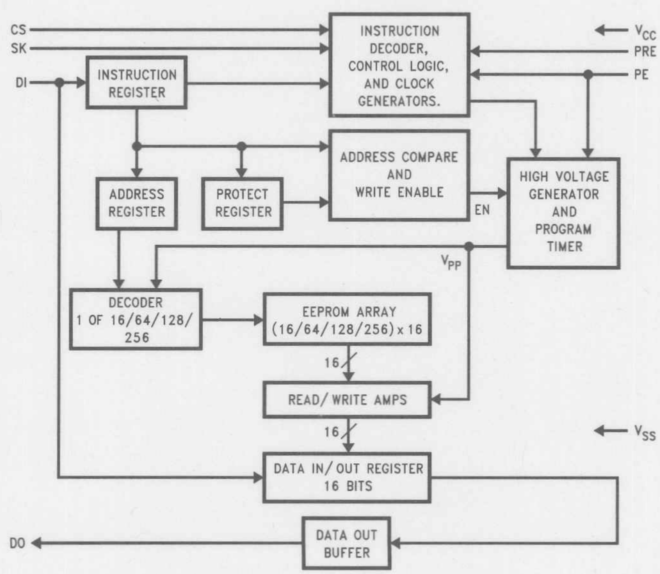
These devices are available in an SO package for small space considerations.

The serial interface that controls these EEPROMs is MICROWIRE compatible, providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PRCLEAR, PRDISABLE and PRENABLE.

Features

- Sequential register read
- Write protection in a user defined section of memory
- 2.0V to 5.5V operating range in read mode
- 2.5V to 5.5V operating range in other modes
- Typical active current of 400 μA; typical standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self timed write cycle
- Device status during programming mode
- 40 year data retention
- Endurance: 10^6 data changes
- Packages Available: 8-pin SO, 8-pin DIP

Block Diagram

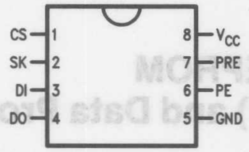


TL/D/10044-1

2

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO Package (M8)



TL/D/10044-2

Top View

See NS Package Number N08E (N)
See NS Package Number M08A (M8)

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93CS06LN/NM93CS46LN/NM93CS56LN/NM93CS66LN NM93CS06LM8/NM93CS46LM8/NM93CS56LM8/NM93CS66LM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93CS06LEN/NM93CS46LEN/NM93CS56LEN/NM93CS66LEN NM93CS06LEM8/NM93CS46LEM8/NM93CS56LEM8/NM93CS66LEM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CSxxL	0°C to +70°C
NM93CSxxLE	−40°C to +85°C
Power Supply (V_{CC}) Range	
Read Mode	2.0V to 5.5V
WRALL Bulk Programming	3.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics: 2V < V_{CC} < 4.5V

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK = 250 kHz		1	mA
I_{CCS}	Standby Current	CS = V_{IL}		50	μA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		−0.1 0.8 V_{CC}	0.15 V_{CC} V_{CC} + 1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}	0.1 V_{CC}	V
f_{SK}	SK Clock Frequency	(Note 5)	0	250	kHz
t_{SKH}	SK High Time		1		μs
t_{SKL}	SK Low Time		1		μs
t_{SKS}	SK Setup Time	SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		μs
t_{CS}	Minimum CS Low Time	(Note 2)	1		μs
t_{CSS}	CS Setup Time		0.2		μs
t_{PRES}	PRE Setup Time		0.2		μs
t_{PES}	PE Setup Time		0.2		μs
t_{DIS}	DI Setup Time		0.4		μs
t_{DH}	DO Hold Time		10		ns
t_{CSH}	CS Hold Time		0		μs
t_{PEH}	PE Hold Time		0.4		μs
t_{PREH}	PRE Hold Time		0.4		μs
t_{DIH}	DI Hold Time		0.4		μs
t_{PD1}	Output Delay to "1"			2	μs
t_{PD0}	Output Delay to "0"			2	μs
t_{SV}	CS to Status Valid			1	μs
t_{DF}	CS to DO in TRI-STATE®	CS = V_{IL}		0.4	μs
t_{WP}	Write Cycle Time			15	ms

2

I_{CCA}	Operating Current CMOS Input Levels		$CS = V_{IH}$, SK = 1.0 MHz		1	mA
I_{CCS}	Standby Current		$CS = V_{IL}$		50	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 $V_{CC}+1$	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OL} = 400 μA	 2.4V	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OL} = −10 μA	 $V_{CC}-0.2$	0.2	V
f_{SK}	SK Clock Frequency		(Note 5)	0	1	MHz
t_{SKH}	SK High Time	NM93CS06L-NM93CS66L NM93CS06LE-NM93CS66LE		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes High	50		ns
t_{CS}	Minimum CS Low Time		(Note 2)	250		ns
t_{CSS}	CS Setup Time			50		ns
t_{PRES}	PRE Setup Time			50		ns
t_{DH}	DO Hold Time			10		ns
t_{PES}	PE Setup Time			50		ns
t_{DIS}	DI Setup Time			100		ns
t_{CSH}	CS Hold Time			0		ns
t_{PEH}	PE Hold Time			250		ns
t_{PREH}	PRE Hold Time			50		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"				500	ns
t_{PD0}	Output Delay to "0"				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE		$CS = V_{IL}$		100	ns
t_{WP}	Write Cycle Time				10	ms

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (This is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH\ (minimum)} + t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
$2.0V \le V_{CC} < 4.5V$ (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	$\pm 10\ \mu A$
$4.5V \le V_{CC} \le 5.5V$ (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/0.4 mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

The extended voltage EEPROMs of the NM93CSxxL Family have 10 instructions as described below. Note that MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the CS06 and CS46 the next 8 bits carry the opcode and the 6-bit address for register selection. For the CS56 and CS66, the next 10 bits carry the opcode and the 8-bit address for register selection. All Data In signals are clocked into the device on the low-to-high SK transition.

Read and Sequential Register Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **Sequential Read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is allocated to the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} internal. D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and that the part is ready for another instruction.

Write All (WRALL):

The WRALL instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. This function is DISABLED if the protect register is in use to lock out a section memory.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: For all protect register operations: If the PRE pin is not held at V_{IH}, all instructions will be applied to the EEPROM array, rather than the Protect Register.

Protect Register Read (PRREAD):

The PRREAD instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction sequence. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

Protect Register Enable (PREN):

The PREN instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction sequence.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The PRCLEAR instruction clears the address stored in the Protect Register and therefore enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction sequence; however, after loading the PRCLEAR instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Please note that the PRCLEAR instruction and the PRWRITE instruction will both program the Protect Register with all 1s. However, the PRCLEAR instruction will allow the LAST register to be programmed, whereas the PRWRITE instruction = all 1s will PREVENT the last register from being programmed. In addition, the PRCLEAR instruction will allow the use of the WRALL command, where the PRWRITE = all 1s will lock out the Bulk programming opcode.

Protect Register Write (PRWRITE):

The PRWRITE instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction, the Protect Register must first be cleared by executing a PRCLEAR operation and the PRE and PE pins **must** be held high while loading the instruction; however, after loading the PRWRITE instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The PRDS instruction is a **ONE** TIME ONLY instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Instruction Set for the NM93CS06L and NM93CS46L

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Enable all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	**ONE TIME ONLY** instruction after which the address in the Protect Register cannot be altered.

Note: Address bits A5 and A4 become "Don't Care" for the NM93CS06L.

Instruction Set for the NM93CS56L and NM93CS66L

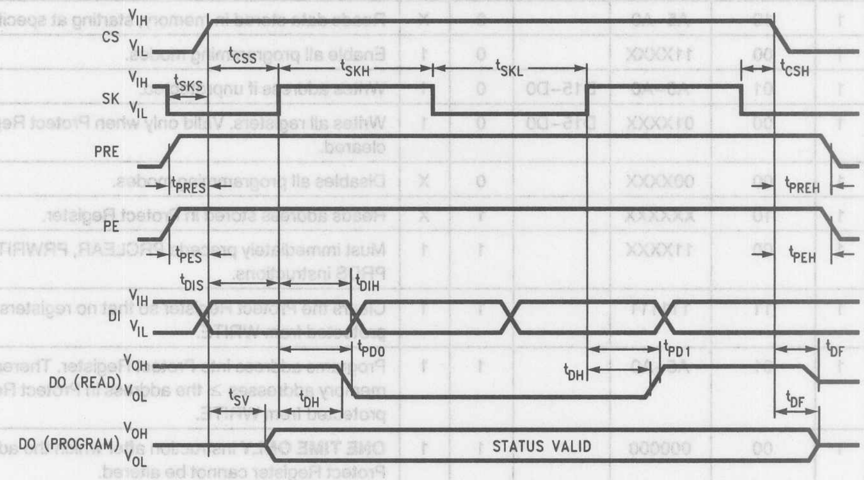
Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Enable all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	**ONE TIME ONLY** instruction after which the address in the Protect Register cannot be altered.

Note: Address bit A7 becomes "Don't Care" for the NM93CS56L.

2

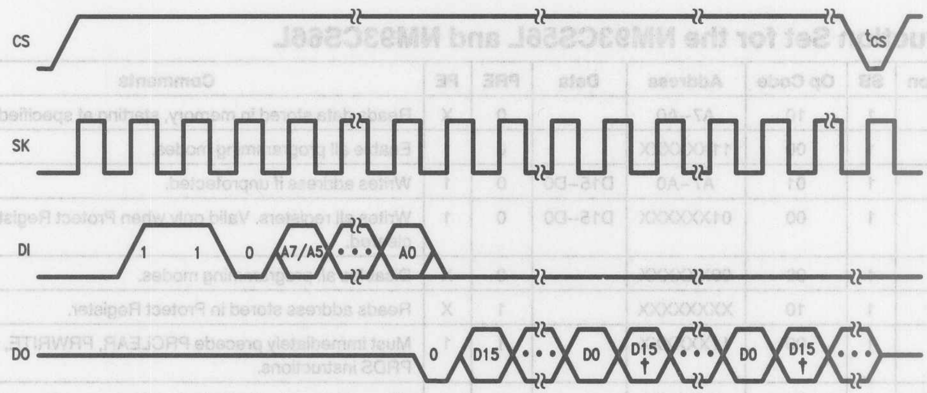
Timing Diagrams

Synchronous Data Timing



TL/D/10044-15

READ:
PRE = 0, PE = X

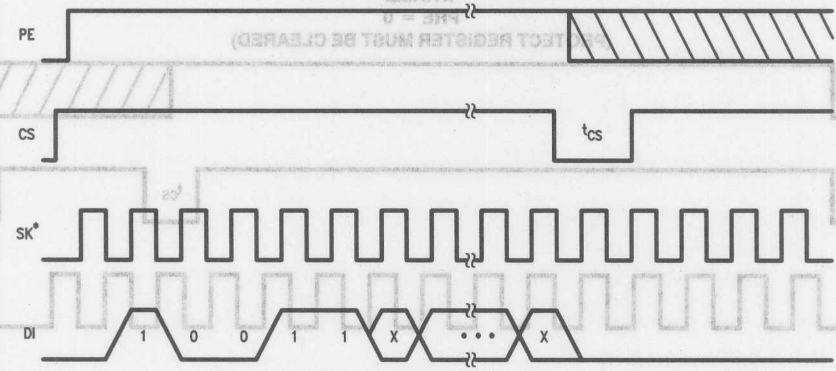


TL/D/10044-5

†The memory automatically cycles to the next register.

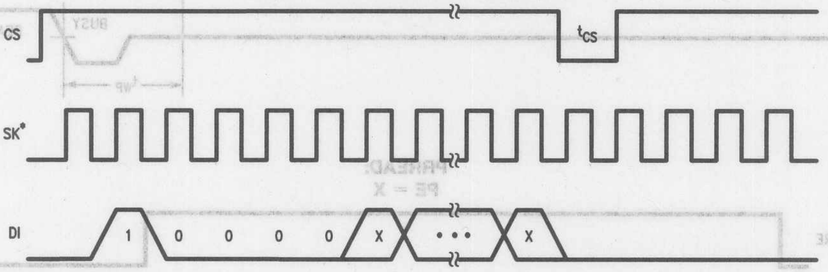
Timing Diagrams (Continued)

WEN:
PRE = 0, D0 = TRI-STATE



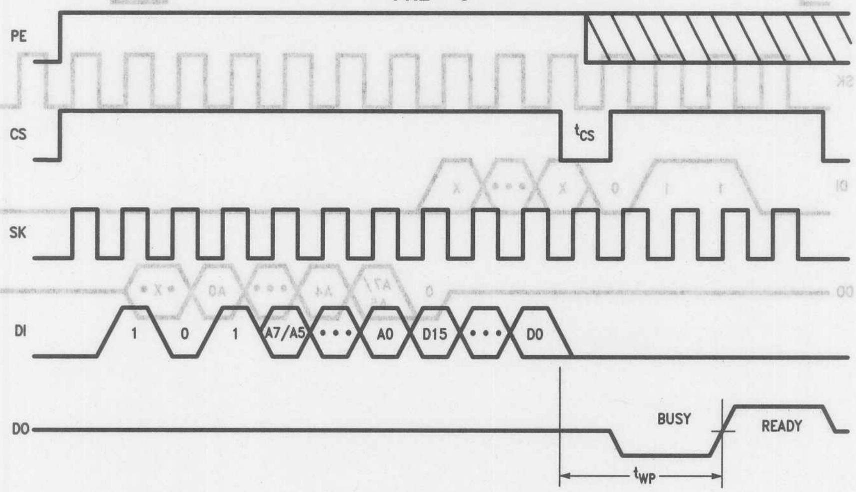
TL/D/10044-6

WDS:
PRE = 0, PE = X, DO = TRI-STATE



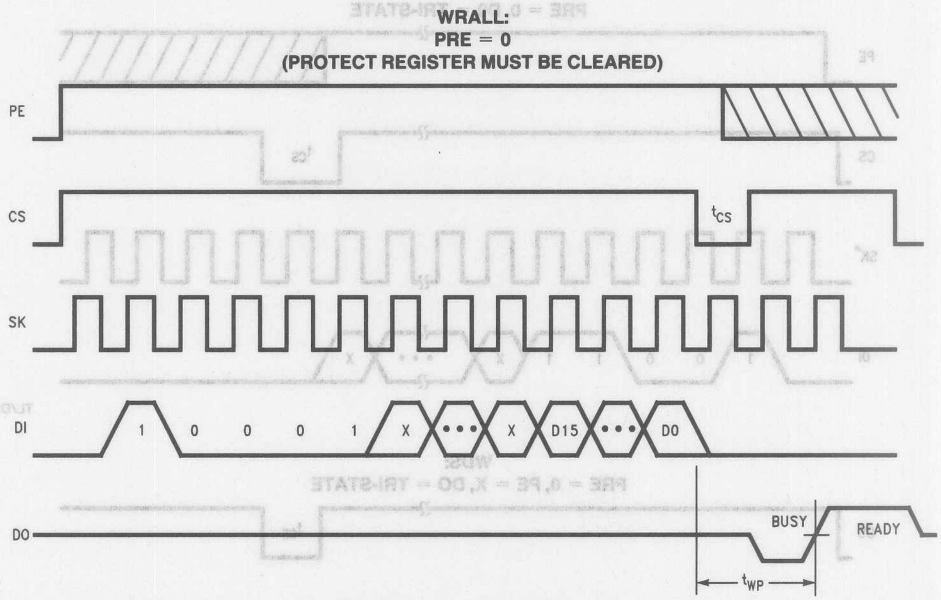
TL/D/10044-7

WRITE:
PRE = 0

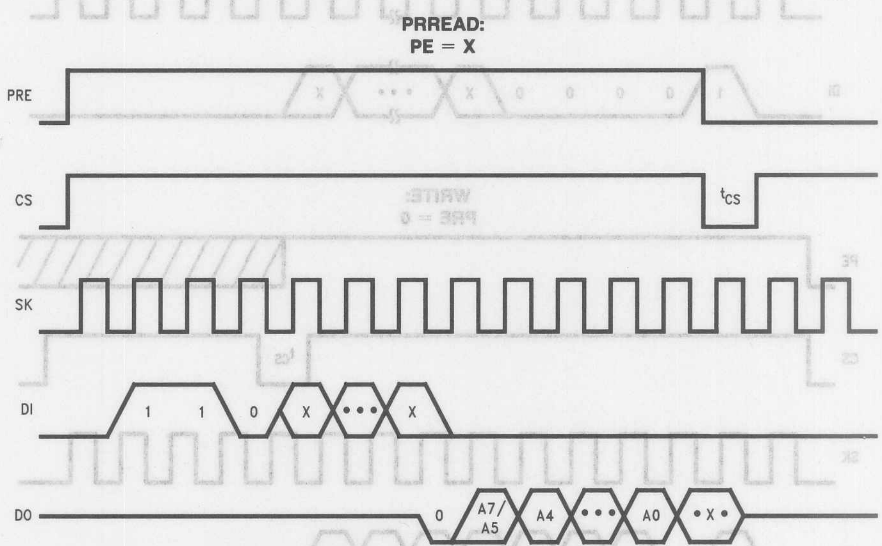


TL/D/10044-8

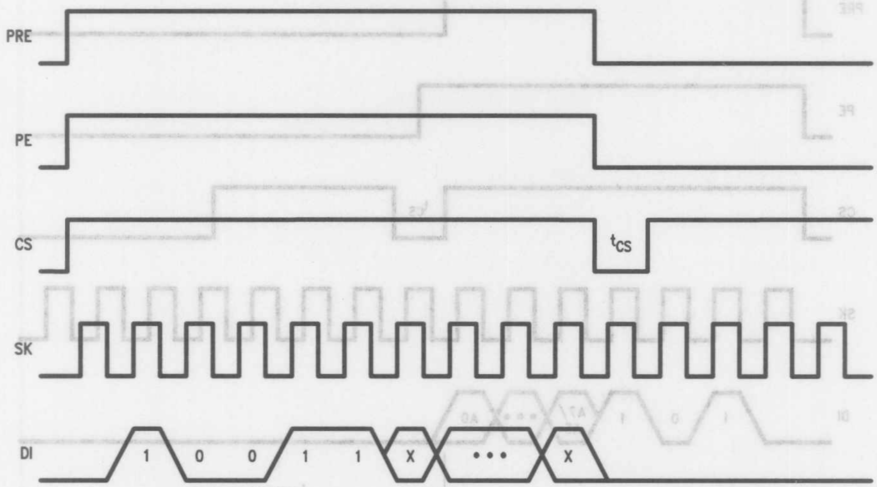
Timing Diagrams (Continued)



TL/D/10044–9

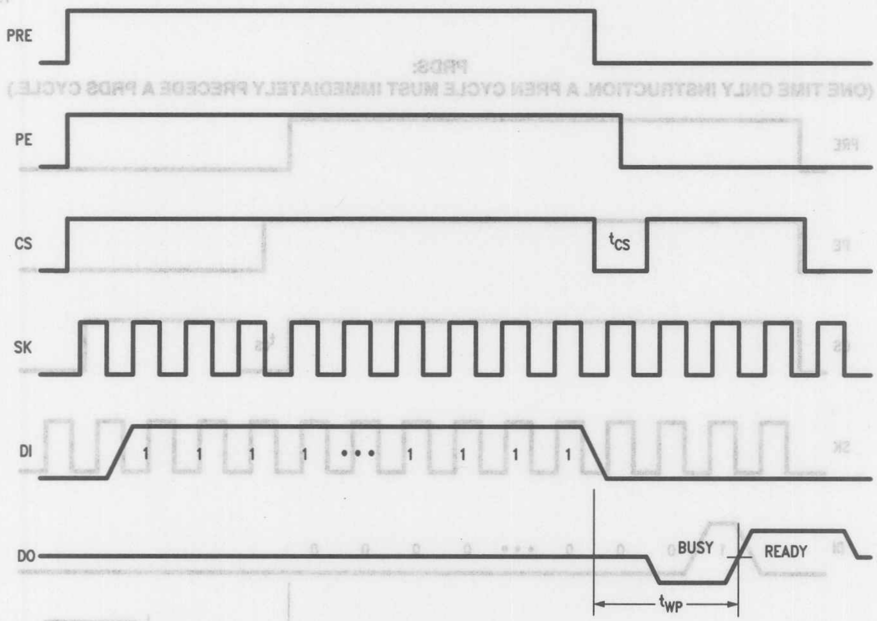


TL/D/10044–10



TL/D/10044–11

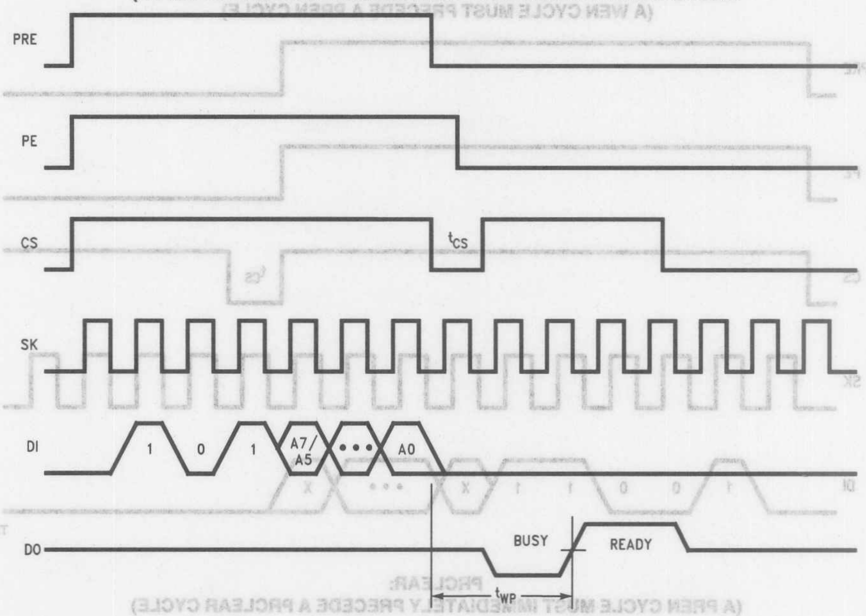
PRCLEAR:
(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRCLEAR CYCLE)



TL/D/10044–12

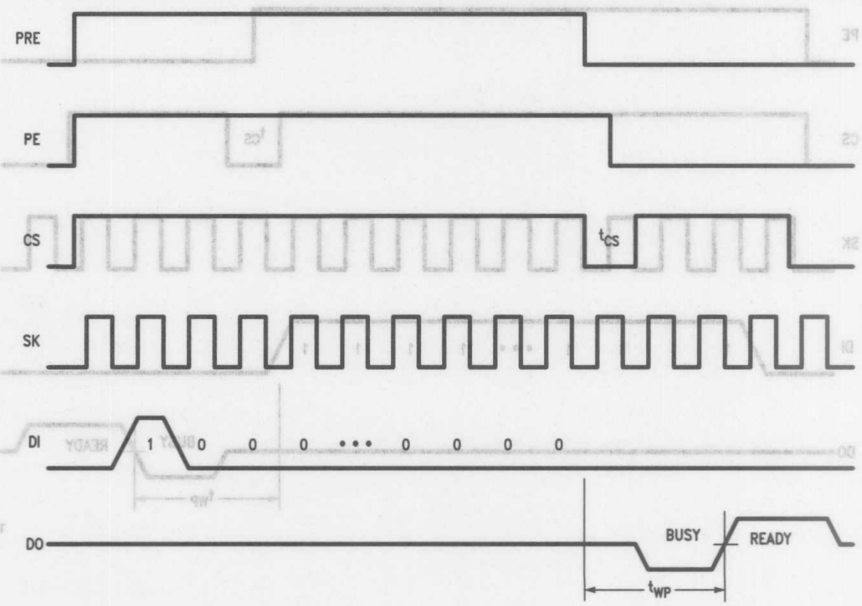
Timing Diagrams (Continued)

PRWRITE:
(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRWRITE CYCLE.



TL/D/10044–13

PRDS:
(ONE TIME ONLY INSTRUCTION. A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRDS CYCLE.)



TL/D/10044–14

National Semiconductor

PRELIMINARY

NM93C06LZ/C46LZ/C56LZ/C66LZ 256-/1024-/2048-/4096-Bit Serial EEPROM with Zero Power and Extended Voltage (2V to 6V) (MICROWIRE™ Bus Interface)

General Description

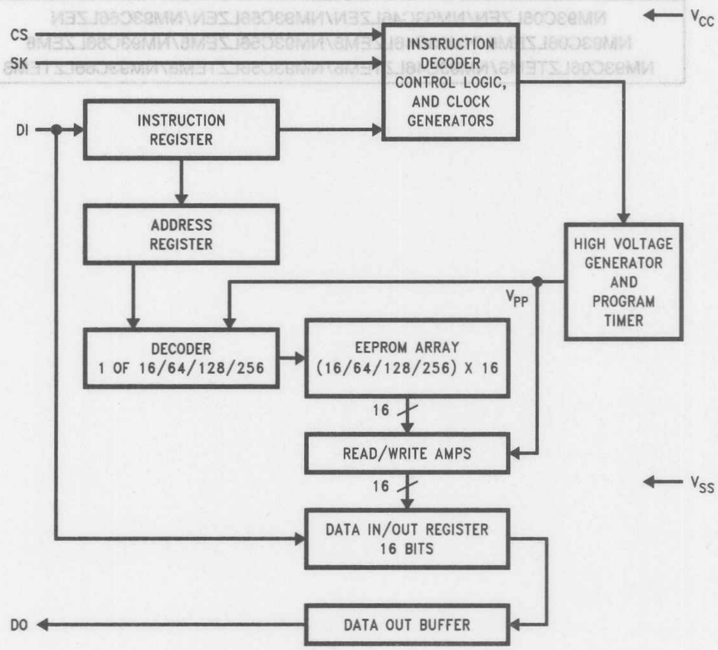
The NM93C06LZ/C46LZ/C56LZ/C66LZ devices are 256/1024/2048/4096 bits respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in an SO package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- **2.0V to 6.0V operation in all modes**
- **Less than 1.0 μA standby current**
- Typical active current of 400 μA
- Direct write: no erase before program
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status indication during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



TL/D/11865–1

Connection Diagrams

Dual-in-Line Package (N) and 8-Pin SO (M8)

TL/D/11865-2

Top View

See NS Package Number N08E and M08A

Alternate SO Pinout (TM8)

TL/D/11865-3

NS Package Number M08A

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM93C06LZN/NM93C46LZN/NM93C56LZN/NM93C66LZN
NM93C06LZM8/NM93C46LZM8/NM93C56LZM8/NM93C66LZM8
NM93C06LZTM8/NM93C46LZTM8/NM93C56LZTM8/NM93C66LZTM8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM93C06LZEN/NM93C46LZEN/NM93C56LZEN/NM93C66LZEN
NM93C06LZEM8/NM93C46LZEM8/NM93C56LZEM8/NM93C66LZEM8
NM93C06LZTEM8/NM93C46LZTEM8/NM93C56LZTEM8/NM93C66LZTEM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	V_{CC} + 1 to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C06LZ/46LZ/56LZ/66LZ	0°C to +70°C
NM93C06LZE/46LZE/56LZE/66LZE	−40°C to +85°C
Power Supply (V_{CC}) Range:	
ERAL/WRALL Operation	3.0V to 6.0V
All Other Modes (Note 6)	2.0V to 6.0V

DC and AC Electrical Characteristics: 2V < V_{CC} < 4.5V

Symbol	Parameter	Part Number	Conditions	Min	Typ	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 250 kHz		0.4	1	mA
I_{CCS}	Standby Current		CS = 0V		0.5	1	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)			±200	nA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 0.8 V_{CC}		0.15 V_{CC} V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 0.9 V_{CC}		0.2	V
f_{SK}	SK Clock Frequency		(Note 5)	0		250	kHz
t_{SKH}	SK High Time			1			μs
t_{SKL}	SK Low Time			1			μs
t_{SKS}	SK Setup Time			0.2			μs
t_{CS}	Minimum CS Low Time		(Note 2)	1			μs
t_{CSS}	CS Setup Time			0.2			μs
t_{DH}	DO Hold Time			70			ns
t_{DIS}	DI Setup Time			0.4			μs
t_{CSH}	CS Hold Time			0			μs
t_{DIH}	DI Hold Time			0.4			μs
t_{PD1}	Output Delay to "1"					2	μs
t_{PD0}	Output Delay to "0"					2	μs
t_{SV}	CS to Status Valid					1	μs
t_{DF}	CS to DO in TRI-STATE®		CS = V_{IL}			0.4	μs
t_{WP}	Write Cycle Time	NM93C06LZ NM93C46LZ NM93C56LZ	V_{CC} = 2.0V V_{CC} = 2.5V V_{CC} = 3.0V		15 10 8	25 15 10	ms ms ms
		NM93C06LZE NM93C46LZE NM93C56LZE NM93C66LZE	V_{CC} = 2.0V V_{CC} = 2.5V V_{CC} = 3.0V		40 12 10	50 15 15	ms ms ms

I_{CCA}	Operating Current		$CS = V_{IH}$, SK = 1 MHz		0.4	1	mA
I_{CCS}	Standby Current		CS = 0V		0.4	1	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC} (Note 4)			±200	nA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		(Note 7)	−0.1 2		0.8 $V_{CC} + 1$	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA $I_{OL} = -400\ \mu A$	 2.4		0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		$I_{OL} = 10\ \mu A$ $I_{OH} = -10\ \mu A$	 0.9 V_{CC}		0.2	V
f_{SK}	SK Clock Frequency		(Note 5)	0		1	MHz
t_{SKH}	SK High Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE		250 300			ns
t_{SKL}	SK Low Time			250			ns
t_{SKS}	SK Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS goes high	50			ns
t_{CS}	Minimum CS Low Time		(Note 2)	250			ns
t_{CSS}	CS Setup Time			50			ns
t_{DH}	DO Hold Time			70			ns
t_{DIS}	DI Setup Time			100			ns
t_{CSH}	CS Hold Time			0			ns
t_{DIH}	DI Hold Time			20			ns
t_{PD1}	Output Delay to "1"					500	ns
t_{PD0}	Output Delay to "0"					500	ns
t_{SV}	CS to Status Valid					500	ns
t_{DF}	CS to DO in TRI-STATE		$CS = V_{IL}$			100	ns
t_{WP}	Write Cycle Time				6	10	ms

Capacitance $T_A = 25°C, f = 1\ MHz$ (Note 3)

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (this is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period $= 1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH\ (minimum)} + t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

Note 6: LOW VOLTAGE OPERATION: All functional modes are guaranteed over the specified V_{CC} range (as shown in the **Operating Conditions** and **DC/AC Electrical Characteristics**) EXCEPT the ERAL and WRALL bulk programming modes. These bulk programming commands, which reprogram the entire array, are only guaranteed for the V_{CC} range shown on page 3.

Note 7: For operation at V_{CC} levels greater than 5.5V, V_{IH} must conform to EXTENDED VOLTAGE levels where $V_{IH} = V_{CC} - 0.2V$.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
$2.0V \le V_{CC} < 4.5V$ (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	$\pm 10\ \mu A$
$4.5V \le V_{CC} \le 5.5V$ (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/ 0.4 mA
$5.5V < V_{CC} \le 6.0V$ (Extended Voltage Levels)	0.3V/5.8V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/ 0.4 mA
Output Load: 1 TTL Gate ($C_L = 100\ pF$)				

Functional Description

The NM93C06LZ/C46LZ/C56LZ/C66LZ devices have 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the C06 and C46 the next 8 bits carry the op code and the 6-bit address for register selection. For the C56 and C66 the next 10 bits carry the op code and the 8-bit address for register selection. All data in signals are clocked into the device on the low-to-high SK transition.

Read (READ): The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN): When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (WEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or until V_{CC} is completely removed from the part.

Erase (ERASE): The ERASE instruction will program all bits in the selected register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE): The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL): The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write All (WRALL): The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval.

Write Disable (WDS): To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: NSC CMOS EEPROMs do not require an "ERASE" or "ERASE ALL" operation prior to the "WRITE" or "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with earlier technology EEPROMs.

Instruction Set for the NM93C06LZ and NM93C46LZ

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Read data stored in memory, at selected address
WEN	1	00	11XXXX		Enable all programming modes
ERASE	1	11	A5–A0		Erase selected register
WRITE	1	01	A5–A0	D15–D0	Writes selected register
ERAL	1	00	10XXXX		Erases all registers
WRALL	1	00	01XXXX	D15–D0	Writes all registers
WDS	1	00	00XXXX		Disables all programming modes

Note: Address bits A5 and A4 become "Don't Care" for the NM93C06LZ.

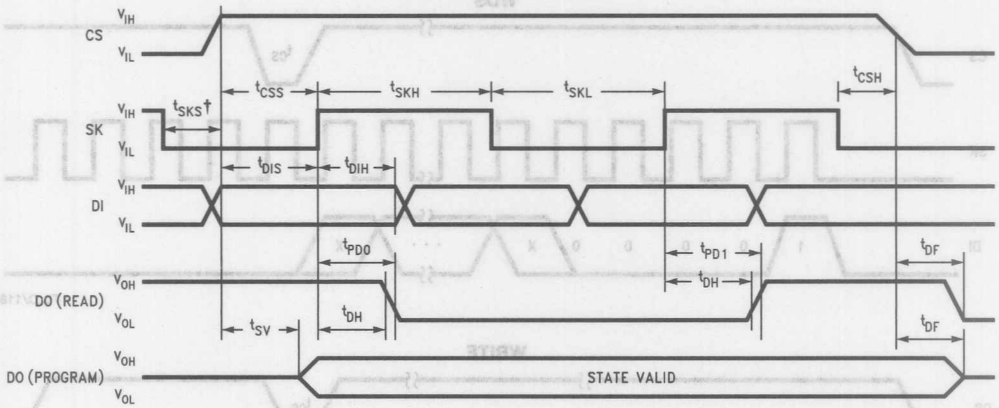
Instruction Set for the NM93C56LZ and NM93C66LZ

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Read data stored in memory, at specified address
WEN	1	00	11XXXXXX		Enable all programming modes
ERASE	1	11	A7–A0		Erase selected register
ERAL	1	00	10XXXXXX		Erases all registers
WRITE	1	01	A7–A0	D15–D0	Write selected registers
WRALL	1	00	01XXXXXX	D15–D0	Writes all registers
WDS	1	00	00XXXXXX		Disables all programming modes

Note: Address bits A7 becomes "Don't Care" for the NM93C56LZ.

Timing Diagrams

Synchronous Data Timing



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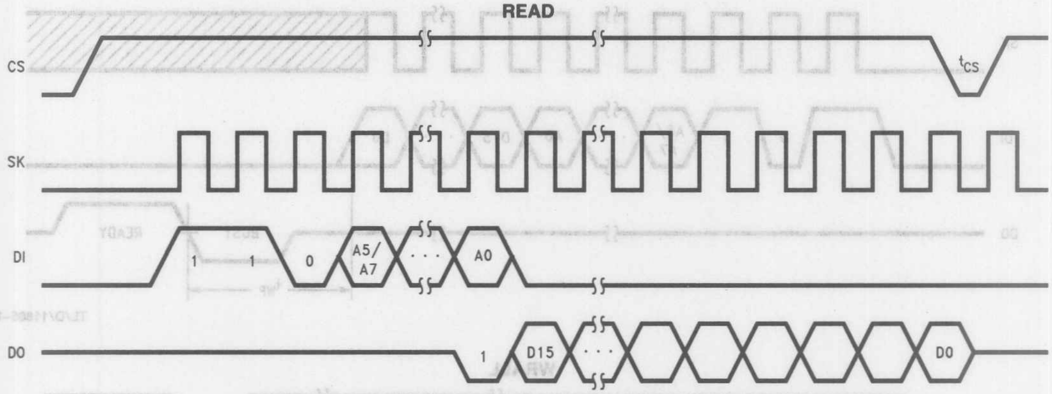
READ



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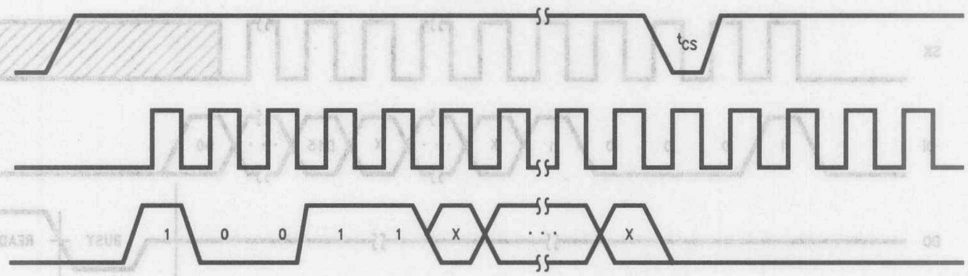
WEN



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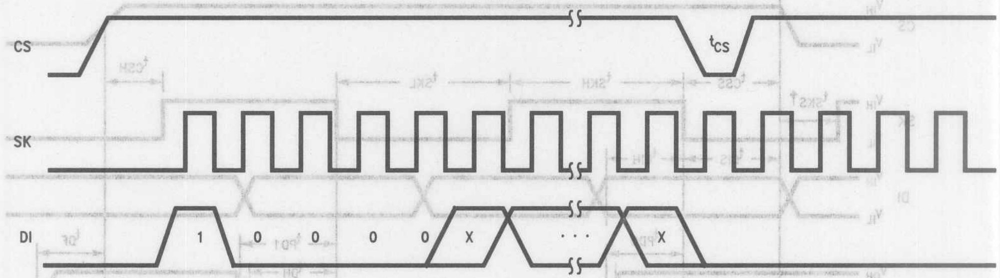
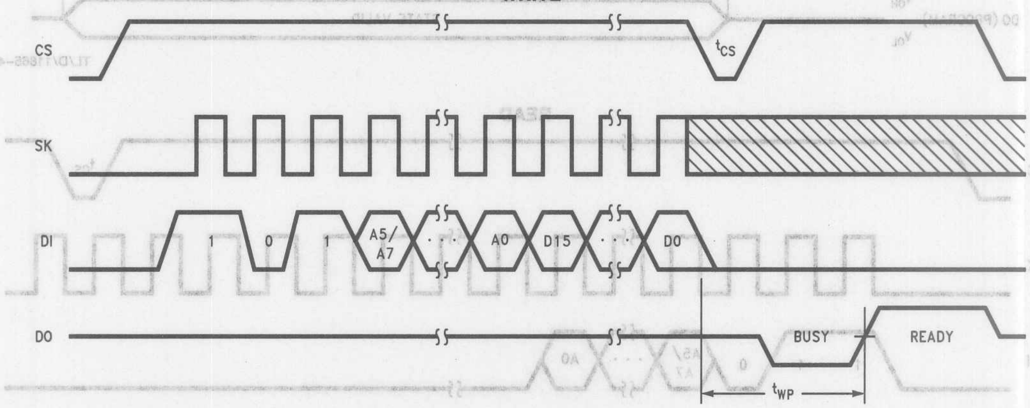
Timing Diagrams (Continued)

WDS



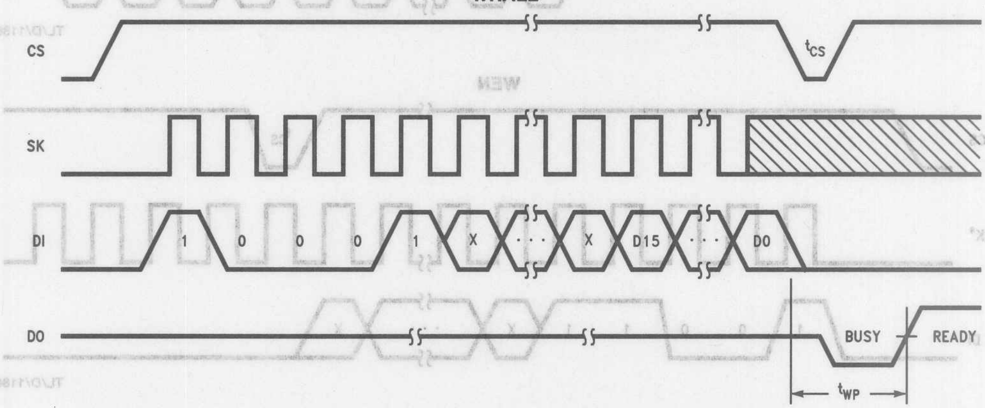
TL/D/11865-7

WRITE



TL/D/11865-8

WRALL



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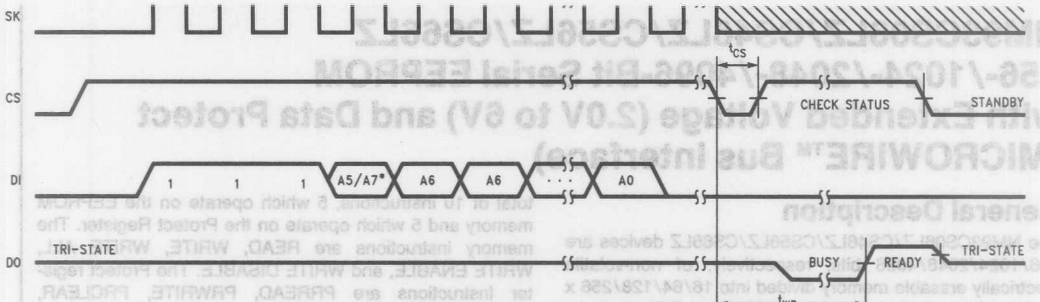
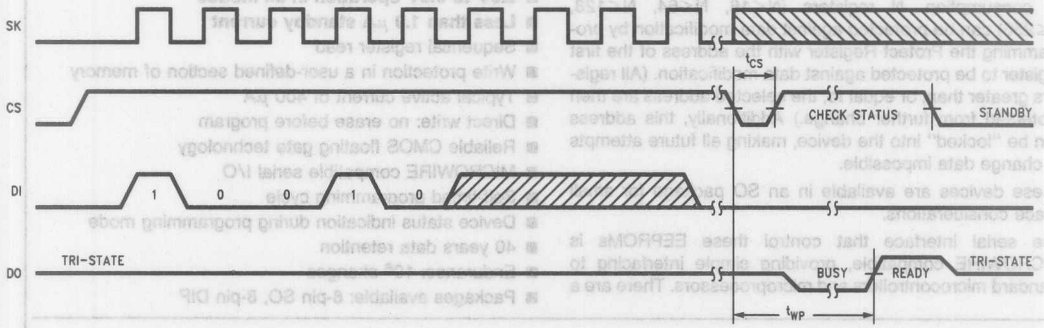


TL/D/11865-10

ERAL



TL/D/11865-11

National Semiconductor

PRELIMINARY

NM93CS06LZ/CS46LZ/CS56LZ/CS66LZ 256-/1024-/2048-/4096-Bit Serial EEPROM with Extended Voltage (2.0V to 6V) and Data Protect (MICROWIRE™ Bus Interface)

General Description

The NM93CS06LZ/CS46LZ/CS56LZ/CS66LZ devices are 256/1024/2048/4096 bits, respectively, of non-volatile electrically erasable memory divided into 16/64/128/256 x 16-bit registers (addresses). The NM93CSxxLZ Family functions in an extended voltage operating range and is fabricated using National Semiconductor's floating gate CMOS technology for high reliability, high endurance and low power consumption. N registers ($N \leq 16$, $N \leq 64$, $N \leq 128$, $N \leq 256$) can be protected against data modification by programming the Protect Register with the address of the first register to be protected against data modification. (All registers greater than, or equal to, the selected address are then protected from further change.) Additionally, this address can be "locked" into the device, making all future attempts to change data impossible.

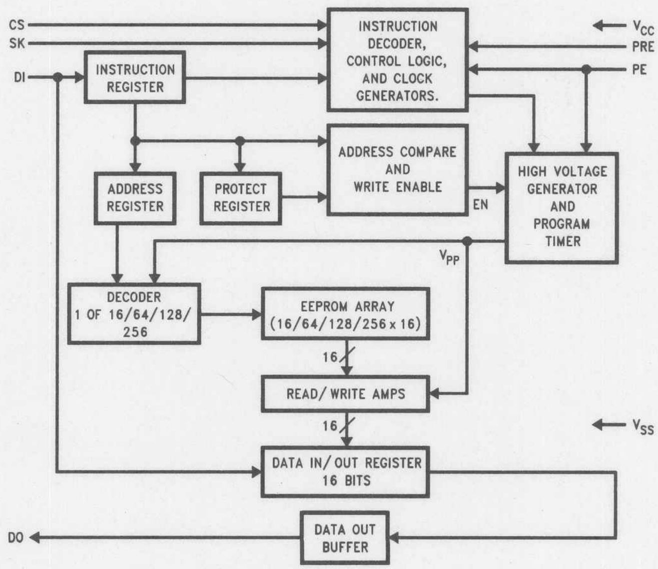
These devices are available in an SO package for small space considerations.

The serial interface that control these EEPROMs is MICROWIRE compatible, providing simple interfacing to standard microcontrollers and microprocessors. There are a total of 10 instructions, 5 which operate on the EEPROM memory and 5 which operate on the Protect Register. The memory instructions are READ, WRITE, WRITE ALL, WRITE ENABLE, and WRITE DISABLE. The Protect register instructions are PRREAD, PRWRITE, PRCLEAR, PRDISABLE and PRENABLE.

Features

- **2.0V to 6.0V operation in all modes**
- **Less than 1.0 μA standby current**
- Sequential register read
- Write protection in a user-defined section of memory
- Typical active current of 400 μA
- Direct write: no erase before program
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status indication during programming mode
- 40 years data retention
- Endurance: 10^6 changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram



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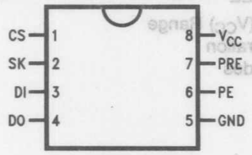
Connection Diagrams

Dual-In-Line Package (N)
and 8-Pin SO Package (M8)



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Top View

NS Package Number N08E (N)
NS Package Number M08A (M8)

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93CS06LZN/NM93CS46LZN/NM93CS56LZN/NM93CS66LZN NM93CS06LZM8/NM93CS46LZM8/NM93CS56LZM8/NM93CS66LZM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93CS06LZEN/NM93CS46LZEN/NM93CS56LZEN/NM93CS66LZEN NM93CS06LZEM8/NM93CS46LZEM8/NM93CS56LZEM8/NM93CS66LZEM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	$-65°C$ to $+150°C$
All Input or Output Voltages with Respect to Ground	$V_{CC} + 1V$ to $-0.3V$
Lead Temperature (Soldering, 10 sec.)	$+300°C$
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93CSxxLZ	$0°C$ to $+70°C$
NM93CSxxLZE	$-40°C$ to $+85°C$
Power Supply (V_{CC}) Range	
WRALL Operation	3.0V to 6.0V
All Other Modes (Note 6)	2.0V to 6.0V

DC and AC Electrical Characteristics: $2V < V_{CC} < 4.5V$

Symbol	Parameter	Part Number	Conditions	Min	Typ	Max	Units
I_{CCA}	Operating Current		$CS = V_{IH}$, $SK = 250$ kHz			1	mA
I_{CCS}	Standby Current		$CS = 0V$			1	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		$V_{IN} = 0V$ to V_{CC} (Note 4)			± 200	nA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		(Note 7)	-0.1 $0.8\ V_{CC}$		$0.15\ V_{CC}$ $V_{CC} + 1$	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage		$I_{OL} = 10\ \mu A$ $I_{OH} = -10\ \mu A$	 $0.9\ V_{CC}$		$0.1\ V_{CC}$	V
f_{SK}	SK Clock Frequency		(Note 5)	0		250	kHz
t_{SKH}	SK High Time			1			μs
t_{SKL}	SK Low Time			1			μs
t_{SKS}	SK Setup Time			0.4			μs
t_{CS}	Minimum CS		(Note 2)	1			μs
t_{CSS}	CS Setup Time			0.2			μs
t_{PRES}	PRE Setup Time			0.2			μs
t_{PES}	PE Setup Time			0.2			μs
t_{DIS}	DI Setup Time			0.4			μs
t_{DH}	DO Hold Time			70			ns
t_{CSH}	CS Hold Time			0			μs
t_{PEH}	PE Hold Time			0.4			μs
t_{PREH}	PRE Hold Time			0.4			μs
t_{DIH}	DI Hold Time			0.4			μs
t_{PD1}	Output Delay to "1"					2	μs
t_{PD0}	Output Delay to "0"					2	μs
t_{SV}	CS to Status Valid					1	μs
t_{DF}	CS to DO in TRI-STATE®		$CS = V_{IL}$			0.4	μs
t_{WP}	Write Cycle Time	NM93CS06LZ NM93CS46LZ NM93CS56LZ	$V_{CC} = 2.0V$ $V_{CC} = 2.5V$ $V_{CC} = 3.0V$		15 10 8	25 15 10	ms ms ms
		NM93CS06LZE NM93CS46LZE NM93CS56LZE	$V_{CC} = 2.0V$ $V_{CC} = 2.5V$ $V_{CC} = 3.0V$		40 12 10	50 15 15	ms ms ms

DC and AC Electrical Characteristics: 4.5V < V_{CC} < 6.0V

Symbol	Parameter	Part Number	Conditions	Min	Typ	Max	Units
I_{CCA}	Operating Current		CS = V_{IH}, SK = 1.0 MHz		0.4	1	mA
I_{CCS}	Standby Current		CS = 0V			1	μA
I_{IL} I_{OL}	Input Leakage Output Leakage		V_{IN} = 0V to V_{CC}			±200	nA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		(Note 7)	−0.1 2		0.8 V_{CC} + 1	V V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4		0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OL} = −10 μA	 V_{CC} − 0.2		0.2	V V
f_{SK}	SK Clock Frequency		(Note 5)	0		1	MHz
t_{SKH}	SK High Time	NM93CS06LZ-NM93CS66LZ NM93CS06LZE-NM93CS66LZE		250 300			ns
t_{SKL}	SK Low Time			250			ns
t_{SKS}	SK Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS goes high	50			ns
t_{CS}	Minimum CS Low Time		(Note 2)	250			ns
t_{CSS}	CS Setup Time			50			ns
t_{PRES}	PRE Setup Time			50			ns
t_{DH}	DO Hold Time			70			ns
t_{PES}	PE Setup Time			50			ns
t_{DIS}	DI Setup Time			100			ns
t_{CSH}	CS Hold Time			0			ns
t_{PEH}	PE Hold Time			250			ns
t_{PREH}	PRE Hold Time			50			ns
t_{DIH}	DI Hold Time			20			ns
t_{PD1}	Output Delay to "1"					500	ns
t_{PD0}	Output Delay to "0"					500	ns
t_{SV}	CS to Status Valid					500	ns
t_{DF}	CS to DO in TRI-STATE®		CS = V_{IL}			100	ns
t_{WP}	Write Cycle Time					10	ms

C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (this is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH\ (minimum)} + t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

Note 6: LOW VOLTAGE OPERATION: All functional modes are guaranteed over specified V_{CC} range (as shown in the **Operating Conditions** and **DC/AC Electrical Characteristics**) EXCEPT the WRALL bulk programming mode. This bulk programming command, which reprograms the entire array, are only guaranteed for the V_{CC} range shown on page 3.

Note 7: For operation at V_{CC} levels greater than 5.5V, V_{IH} must conform to EXTENDED VOLTAGE levels where $V_{IH} = V_{CC} - 0.2V$.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
$2.0V \le V_{CC} < 4.5V$ (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	±10 μA
$4.5V \le V_{CC} \le 5.5V$ (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	− 2.1 mA/0.4 mA
$5.5V < V_{CC} \le 6.0V$ (Extended Voltage Levels)	0.3V/5.8V	1.0V/2.0V	0.4V/2.4V	− 2.1 mA/0.4 mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Functional Description

The extended voltage EEPROMs of the NM93CSxxLZ Family have 10 instructions as described below. Note that MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. For the CS06 and CS46 the next 8 bits carry the op code and the 6-bit address for register selection. For the CS56 and CS66, the next 10 bits carry the op code and the 8-bit address for register selection. All Data In signals are clocked into the device on the low-to-high SK transition.

Read and Sequential Register Read (READ):

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock. In the **Sequential Read** mode of operation, the memory automatically cycles to the next register after each 16 data bits are clocked out. The dummy-bit is suppressed in this mode and a continuous string of data is obtained.

Write Enable (WEN):

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming modes must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Write (WRITE):

The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is allocated to the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The PE pin **MUST** be held high while loading the WRITE instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". The D0 pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. D0 = logical 0 indicates that programming is still in progress. D0 = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and that the part is ready for another instruction.

Write All (WRALL):

The WRALL instruction is valid only when the Protect Register has been cleared by executing a PRCLEAR instruction. The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. Like the WRITE instruction, the PE pin **MUST** be held high while loading the WRALL instruction; however, after loading the WRITE instruction, the PE pin becomes a "don't care". As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. This function is DISABLED if the protect register is in use to lock out a section memory.

Write Disable (WDS):

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: For all protect register operations: If the PRE pin is not held at V_{IH}, all instructions will be applied to the EEPROM array, rather than the Protect Register.

Protect Register Read (PRREAD):

The PRREAD instruction outputs the address stored in the Protect Register on the DO pin. The PRE pin **MUST** be held high while loading the instruction sequence. Following the PRREAD instruction the 6- or 8-bit address stored in the memory protect register is transferred to the serial out shift register. As in the READ mode, a dummy bit (logical 0) precedes the 6- or 8-bit address string.

Protect Register Enable (PREN):

The PREN instruction is used to enable the PRCLEAR, PRWRITE, and PRDS modes. Before the PREN mode can be entered, the part must be in the Write Enable (WEN) mode. Both the PRE and PE pins **MUST** be held high while loading the instruction sequence.

Note that a PREN instruction must **immediately** precede a PRCLEAR, PRWRITE, or PRDS instruction.

Protect Register Clear (PRCLEAR):

The PRCLEAR instruction clears the address stored in the Protect Register and therefore enables **all** registers for the WRITE and WRALL instruction. The PRE and PE pins **must** be held high while loading the instruction sequence; however, after loading the PRCLEAR instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRCLEAR instruction.

Please note that the PRCLEAR instruction and the PRWRITE instruction will both program the Protect Register with all 1s. However, the PRCLEAR instruction will allow the LAST register to be programmed, whereas the PRWRITE instruction = all 1s will PREVENT the last register from being programmed. In addition, the PRCLEAR instruction will allow the use of the WRALL command, where the PRWRITE = all 1s will lock out the Bulk programming opcode.

Protect Register Write (PRWRITE):

The PRWRITE instruction is used to write into the Protect Register the address of the first register to be protected. After the PRWRITE instruction is executed, all memory registers whose addresses are greater than or equal to the address specified in the Protect Register are protected from the WRITE operation. Note that before executing a PRWRITE instruction, the Protect Register must first be cleared by executing a PRCLEAR operation and the PRE and PE pins **must** be held high while loading the instruction; however, after loading the PRWRITE instruction, the PRE and PE pins become "don't care". Note that a PREN instruction must **immediately** precede a PRWRITE instruction.

Protect Register Disable (PRDS):

The PRDS instruction is a ONE TIME ONLY instruction which renders the Protect Register unalterable in the future. Therefore, the specified registers become **PERMANENTLY** protected against data changes. As in the PRWRITE instruction the PRE and PE pins **must** be held high while loading the instruction, and after loading the PRDS instruction the PRE and PE pins become "don't care".

Note that a PREN instruction must **immediately** precede a PRDS instruction.

Instruction Set for the NM93CS06LZ and NM93CS46LZ

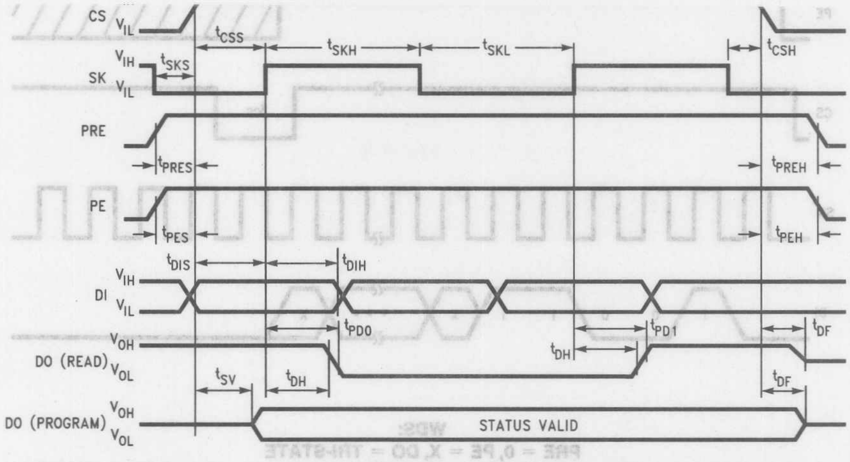
Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Enable all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	**ONE TIME ONLY** instruction after which the address in the Protect Register cannot be altered.

Note: Address bits A5 and A4 become "Don't Care" for the NM93CS06LZ.

Instruction Set for the NM93CS56LZ and NM93CS66LZ

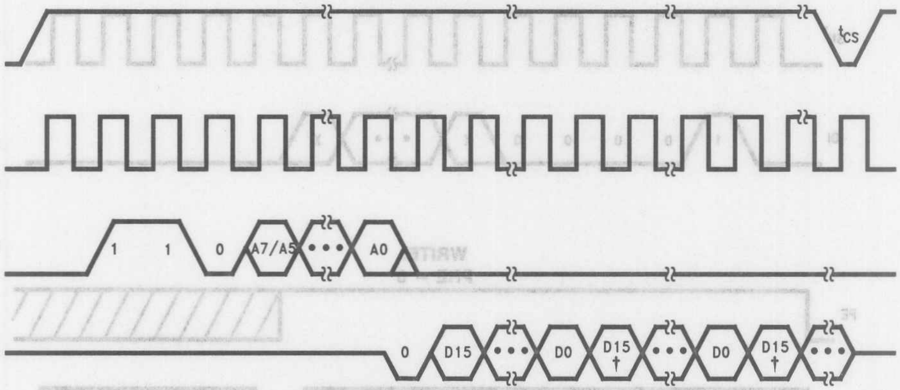
Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXXXX		0	1	Enable all programming modes.
WRITE	1	01	A7–A0	D15–D0	0	1	Writes address if unprotected.
WRALL	1	00	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXXXX		0	X	Disables all programming modes.
PRREAD	1	10	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	11111111		1	1	Clears the "protect register" so that no registers are protected from WRITE.
PRWRITE	1	01	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	00000000		1	1	**ONE TIME ONLY** instruction after which the address in the Protect Register cannot be altered.

Note: Address bit A7 becomes "Don't Care" for the NM93CS56LZ.



TL/D/11807-4

READ:
PRE = 0, PE = X



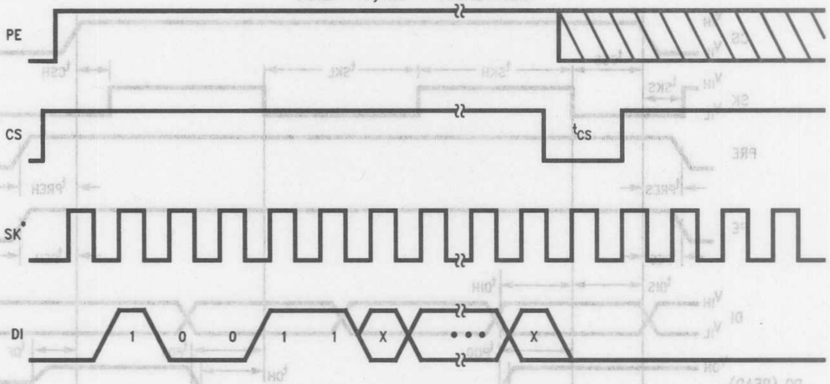
TL/D/11807-5

†Sequential read is possible when CS is held high. The device will automatically cycle to the next register and output sequentially.

2

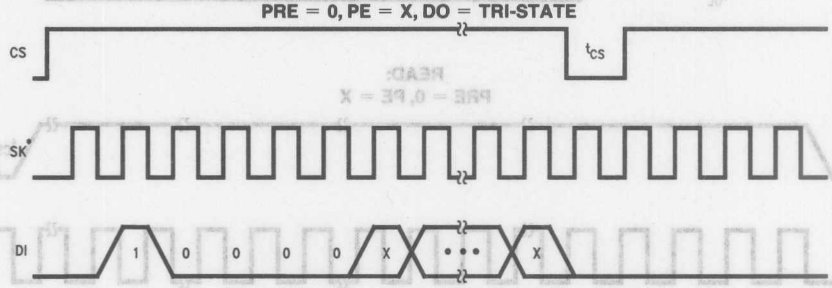
Timing Diagrams (Continued)

WEN:
PRE = 0, D0 = TRI-STATE



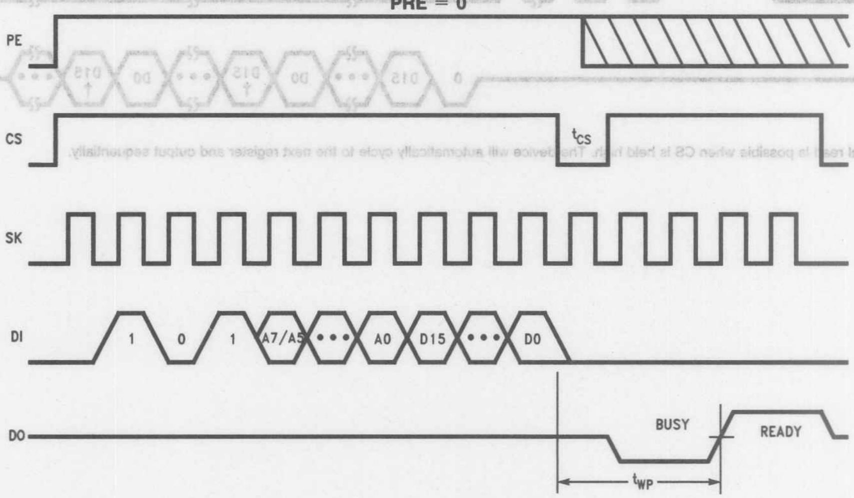
TL/D/11807-6

WDS:
PRE = 0, PE = X, DO = TRI-STATE



TL/D/11807-7

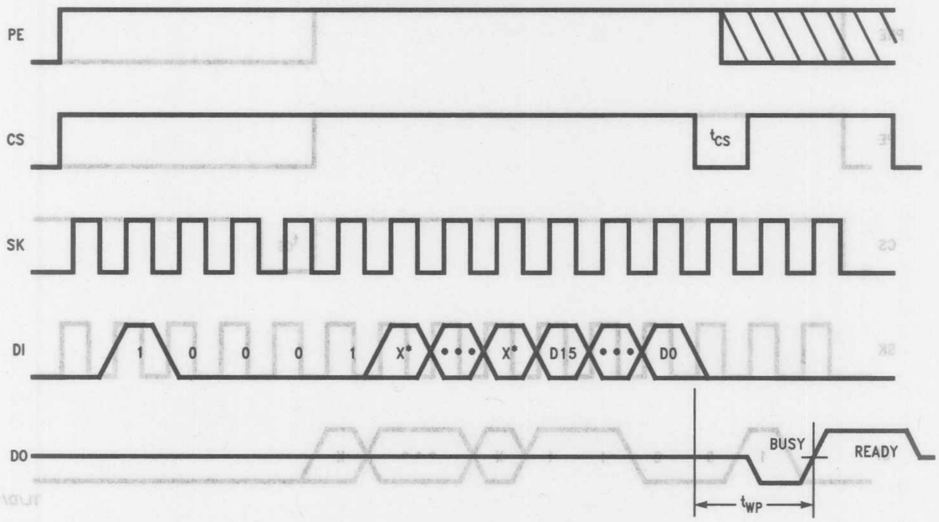
WRITE:
PRE = 0



TL/D/11807-8

Timing Diagrams (Continued)

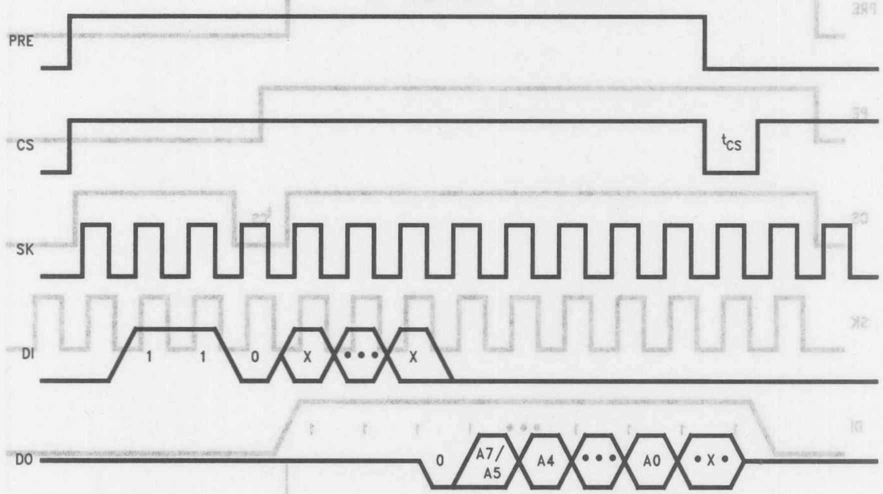
WRALL:
PRE = 0
(PROTECT REGISTER MUST BE CLEARED)



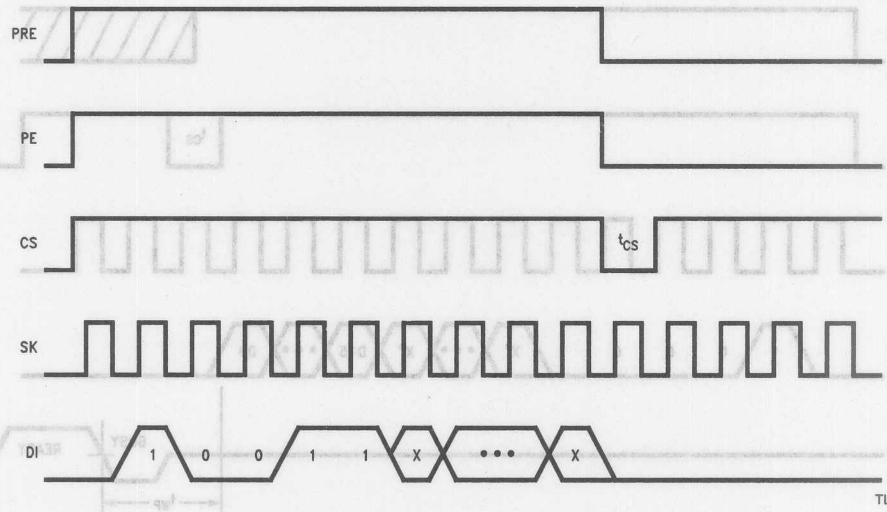
*Don't care

TL/D/11807–9

PRREAD:
PE = X

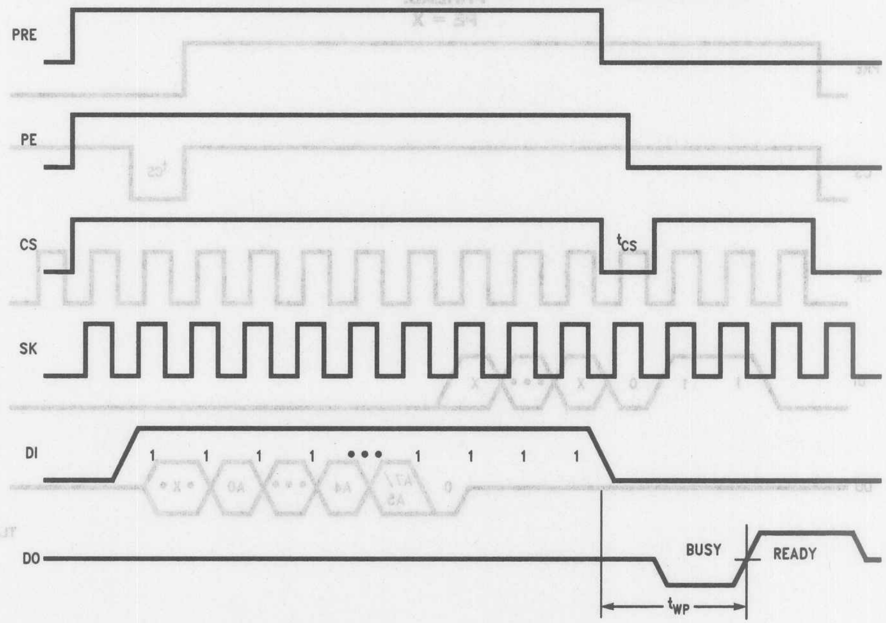


TL/D/11807–10



TL/D/11807-11

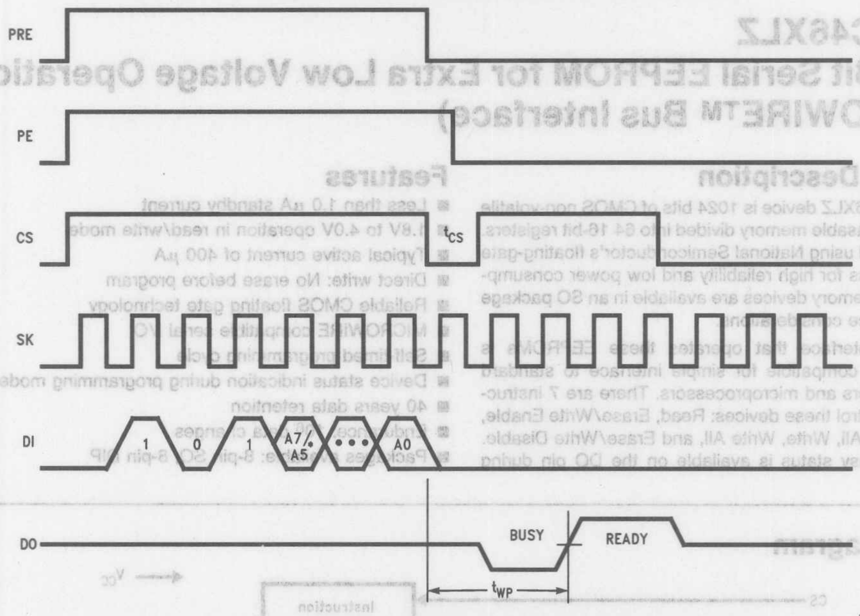
PRCLEAR:
(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRCLEAR CYCLE)



TL/D/11807-12

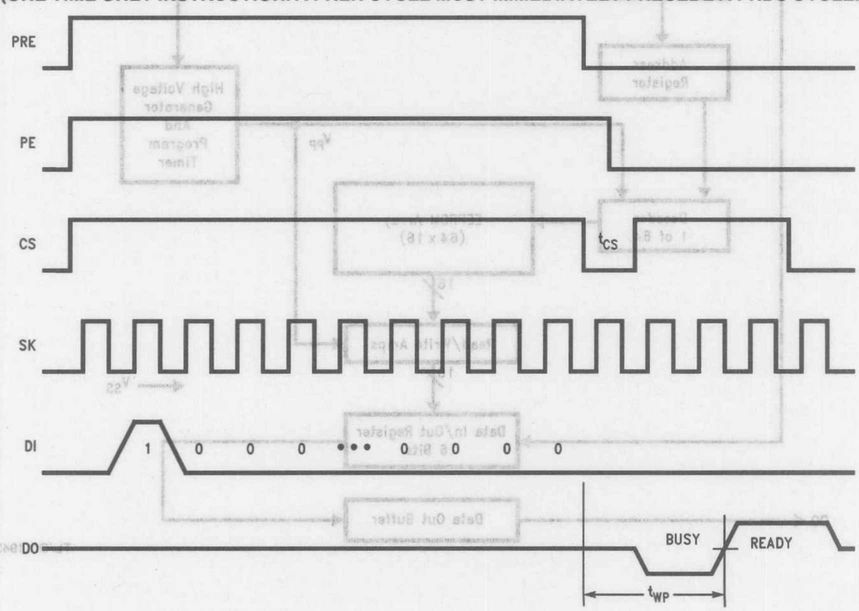
Timing Diagrams (Continued)

PRWRITE†:
(A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRWRITE CYCLE.)



TL/D/11807-13

PRDS:
(ONE TIME ONLY INSTRUCTION. A PREN CYCLE MUST IMMEDIATELY PRECEDE A PRDS CYCLE.)



TL/D/11807-14

National Semiconductor

NM93C46XLZ 1024-Bit Serial EEPROM for Extra Low Voltage Operation (MICROWIRE™ Bus Interface)

General Description

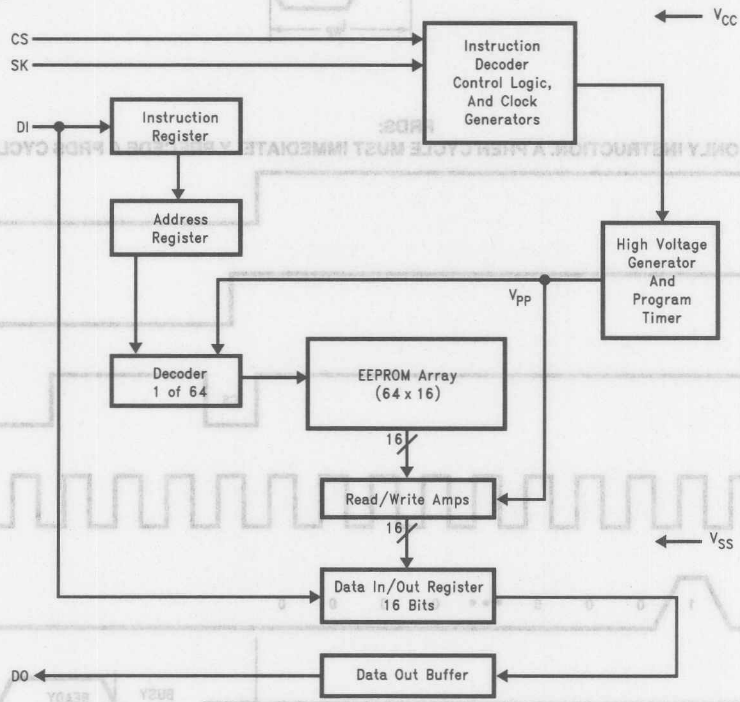
The NM93C46XLZ device is 1024 bits of CMOS non-volatile electrically erasable memory divided into 64 16-bit registers. It is fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in an SO package for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin during programming.

Features

- Less than 1.0 μA standby current
- 1.8V to 4.0V operation in read/write mode
- Typical active current of 400 μA
- Direct write: No erase before program
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status indication during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

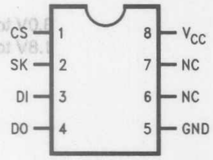
Block Diagram



TL/D/11943-1

Connection Diagrams

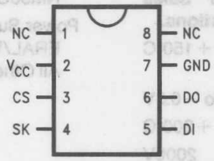
Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/11943-2

Top View
See NS Package Number N08E and M08A

Alternate SO Pinout (TM8)



TL/D/11943-11

See NS Package Number M08A

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46XLZN NM93C46XLZM8/NM93C46XLZTM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to −0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46XL	0°C to +70°C
Power Supply (V_{CC}) Range	
ERAL/WRALL Operation	3.0V to 4.0V
All Other Modes (Note 6)	1.8V to 4.0V

DC and AC Electrical Characteristics: $1.8V < V_{CC} < 4.0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK = 250 kHz		0.4	1	mA
I_{CCS}	Standby Current	CS = 0V		0.5	1	μA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 3)			±200	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		−0.1 0.8 V_{CC}		0.15 V_{CC}	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 10 μA I_{OH} = −10 μA	 0.8 V_{CC}		0.2	V
f_{SK}	SK Clock Frequency	(Note 4)	0		250	kHz
t_{SKH}	SK High Time		1			μs
t_{SKL}	SK Low Time		1			μs
t_{SKS}	SK Setup Time		0.4			μs
t_{CS}	Minimum CS Low Time	(Note 2)	1			μs
t_{CSS}	CS Setup Time		0.2			μs
t_{DH}	DO Hold Time		70			ns
t_{DIS}	DI Setup Time		0.4			μs
t_{CSH}	CS Hold Time		0			μs
t_{DIH}	DI Hold Time		0.4			μs
t_{PD1}	Output Delay to "1"				2	μs
t_{PD0}	Output Delay to "0"				2	μs
t_{SV}	CS to Status Valid				1	μs
t_{DF}	CS to DO in TRI-STATE®	CS = V_{IL}			0.4	μs
t_{WP}	Write Cycle Time			100	150	ms

V_{CC} Range	AC Test Conditions	
$1.8V < V_{CC} < 4.0V$	Input Pulse Levels	0.3V and 1.8V
	Timing Measurement Level (V_{IL}/V_{IH})	1.0V
	Timing Measurement Level (V_{OL}/V_{OH})	0.8V and 1.5V
	(CMOS Load Condition: $I_{OL} = 10\ \mu A$, $I_{OH} = -10\ \mu A$)	

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (This is shown in the opcode diagrams on the following pages).

Note 3: Typical leakage values are in the 20 nA range.

Note 4: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 5: LOW VOLTAGE OPERATION: All functional codes are guaranteed over the specified V_{CC} range (as shown in the **Operating Conditions** and **DC/AC Electrical Characteristics**) EXCEPT the ERAL and WRALL bulk programming modes. These bulk programming commands, which reprogram the entire array, are only guaranteed for the operating range shown on page 3.

Functional Description

The NM93C46XLZ device has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bits in the interface sequence. The next 8 bits carry the op code and the 6-bit address for register selection.

All Data-In signals are clocked into the device on the low-to-high SK transition.

Read (READ): The READ instruction outputs serial data on the DO pin. After the READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN): When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (WEN) instruction. Once an Erase/Write Enable instruction is executed programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or until V_{CC} is completely removed from the part.

Erase (ERASE): The ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after an interval of t_{CS}. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE): The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after an interval of t_{CS}. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL): The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after an interval of t_{CS}.

Write All (WRALL): The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after an interval of t_{CS}.

Erase/Write Disable (WDS): To protect against accidental data disturb, the (WDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

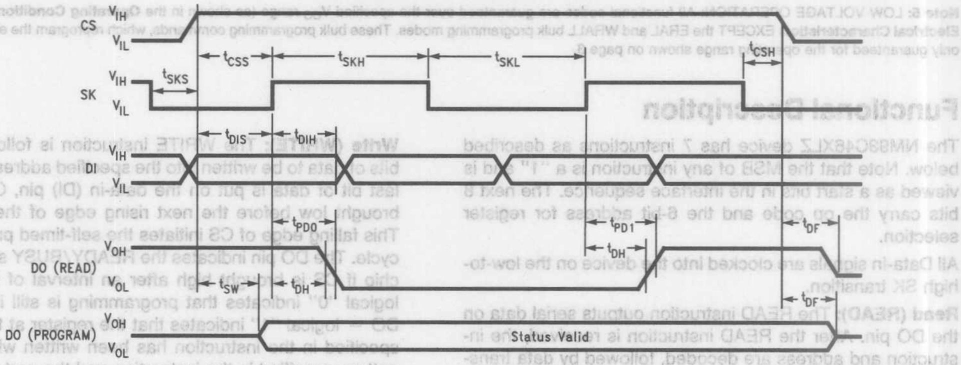
Note: The NM93C46XLZ devices do not require an "ERASE" or "ERASE ALL" prior to the "WRITE" or "WRITE ALL" instructions.

Instruction Set for the NM93C46XLZ

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Read data stored in memory, at specified address
WEN	1	00	11XXXX		Enables all programming modes
WDS	1	00	00XXXX		Disables all programming modes
ERASE	1	11	A5–A0		Erase selected register
WRITE	1	01	A5–A0	D15–D0	Writes selected register
ERAL	1	00	10XXXX		Erases all registers
WRALL	1	00	01XXXX	D15–D0	Writes all registers

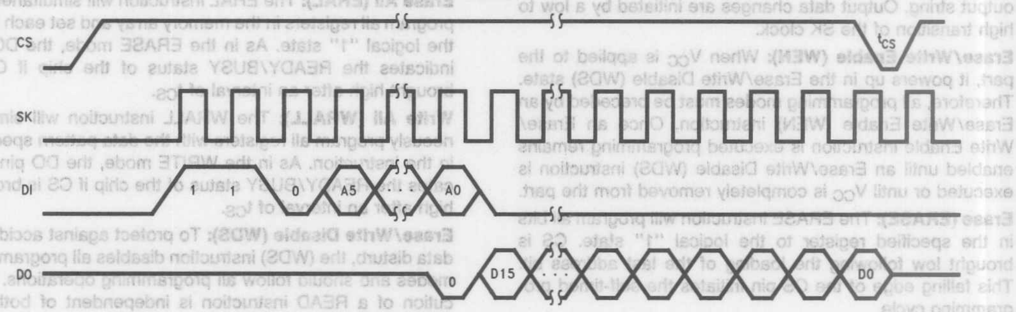
Timing Diagrams

Synchronous Data Timing



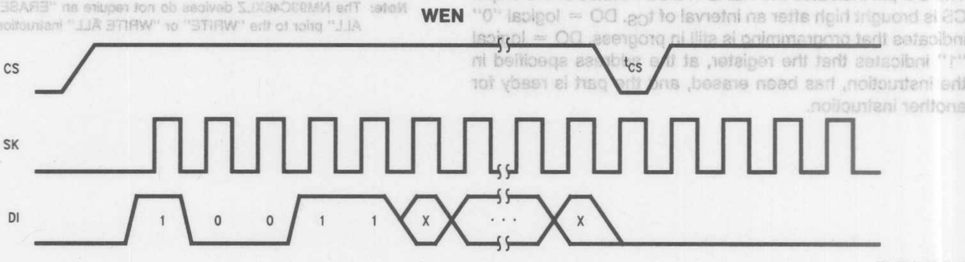
TL/D/11943–3

READ



TL/D/11943–4

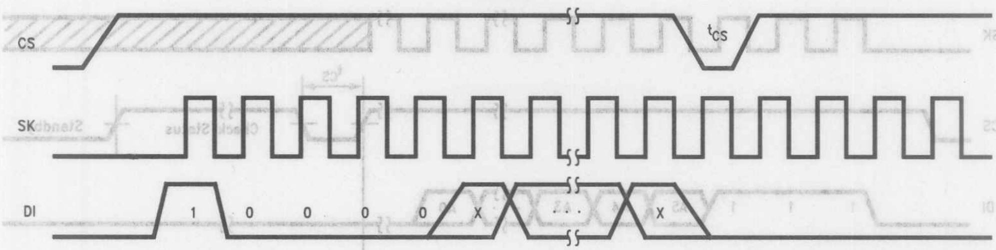
WEN



TL/D/11943–5

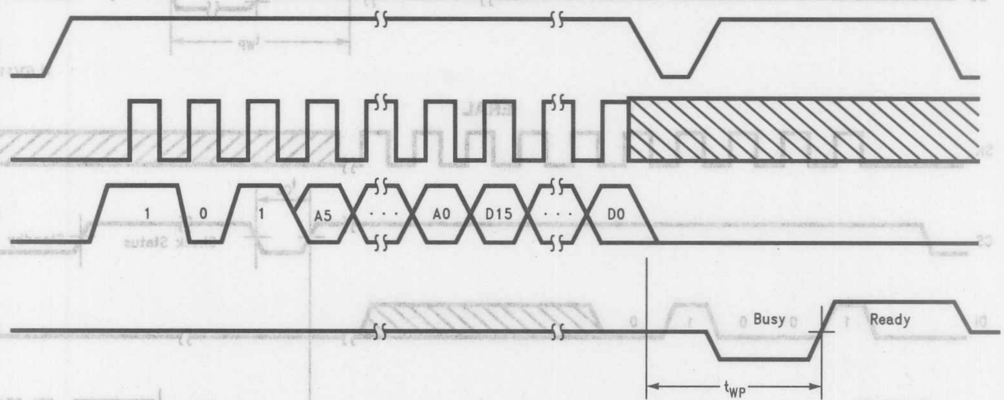
Timing Diagrams (Continued)

WDS



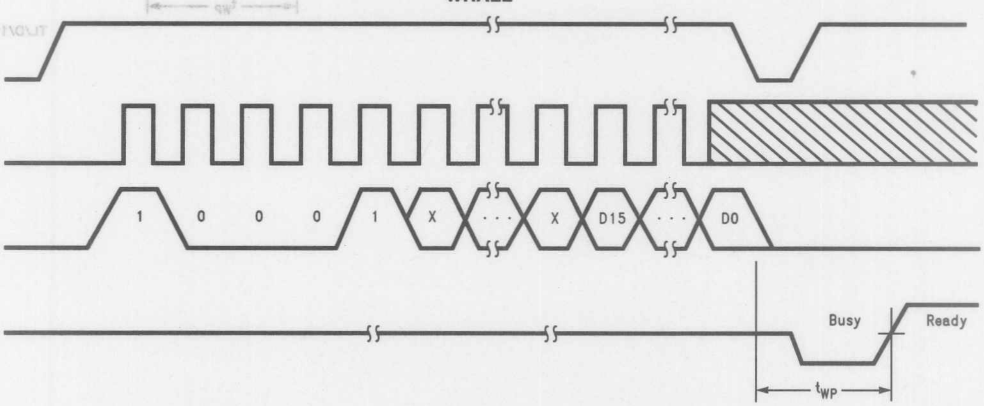
TL/D/11943-6

WRITE

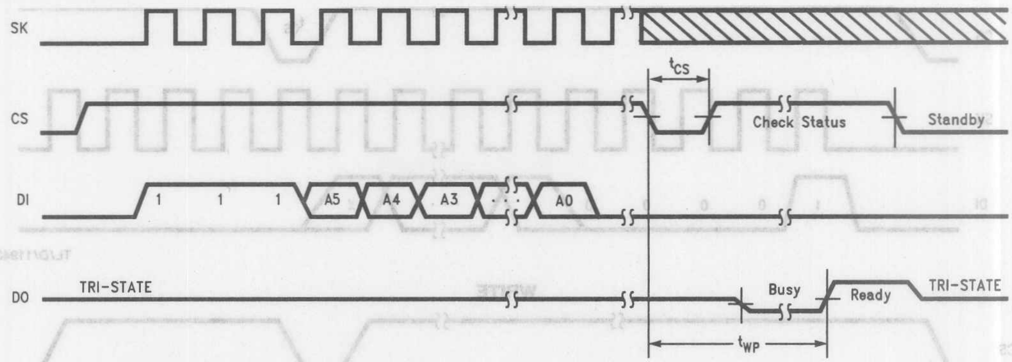


TL/D/11943-7

WRALL

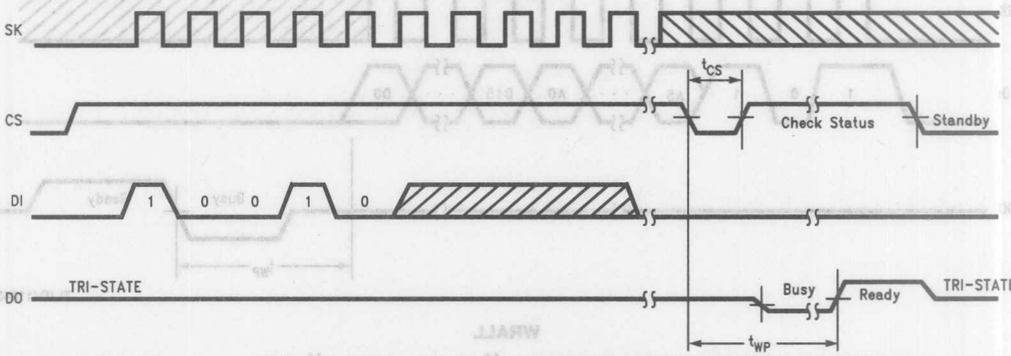


TL/D/11943-8



TL/D/11943-9

ERAL



TL/D/11943-10

National Semiconductor

NM93C46A
1024-Bit Serial EEPROM 64 x 16-Bit or 128 x 8-Bit Configurable (MICROWIRE™ Bus Interface)

General Description

The NM93C46A is 1024 bits of CMOS non-volatile electrically erasable memory organized as either 64 16-bit registers or 128 8-bit registers. The organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM93C46A is available in an SO package for space considerations.

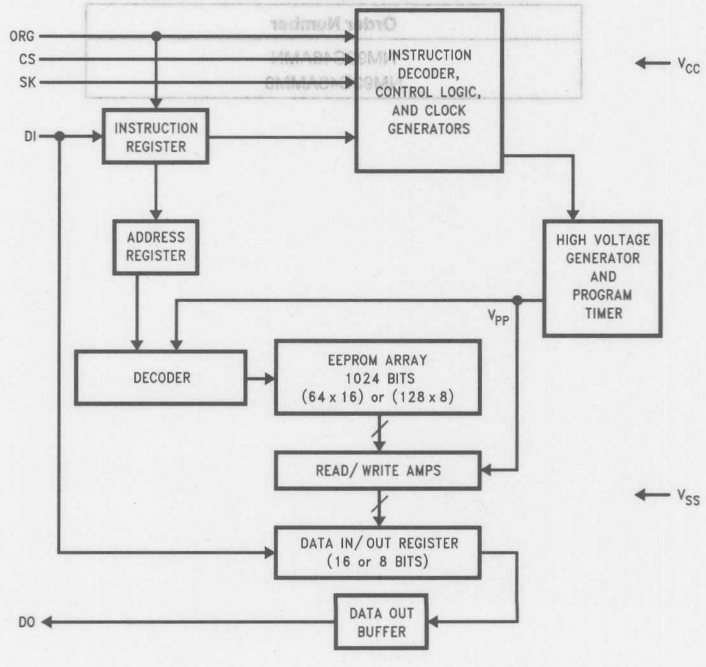
The EEPROM interfacing is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C46A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All. The Ready/Busy status is available on the D_{OUT} pin during programming.

The NM93C46A is compatible with National Semiconductor's NM93C46 if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC} to default to the 64 x 16 configuration.

Features

- Device status during programming mode
- Typical active current of 400 μA; typical standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

Block Diagram

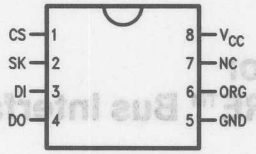


TL/D/11042–1

2

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/11042–2

Top View

NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Organization

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46AN
NM93C46AM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C46AEN
NM93C46AEM8

Military Temp. Range (−55°C to +125°C)

Order Number
NM93C46AMN
NM93C46AMM8

Ambient Storage Temperature	$-65°C$ to $+150°C$	NM93C46AM	$-55°C$ to $+125°C$
All Input or Output Voltages with Respect to Ground	$+6.5V$ to $-0.3V$	Power Supply (V_{CC})	4.5V to 5.5V
Lead Temperature (Soldering, 10 Seconds)	$+300°C$		
EDS Rating	2000V		

DC and AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$ Unless Otherwise Specified

Note: Throughout this table, "M" refers to temperature range ($-55°C$ to $+125°C$), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current	NM93C46A	$CS = V_{IH}$, SK = 1 MHz			
		NM93C46AE	SK = 1 MHz		1	mA
		NM93C46AM	SK = 0.5 MHz			
I_{CCS}	Standby Current	NM93C46A	$CS = V_{IL}$		50	
		NM93C46AE		50		μA
		NM93C46AM		100		
I_{IL}	Input Leakage		$V_{IN} = 0V$ to V_{CC}		± 1	μA
I_{OL}	Output Leakage		(Note 4)			
V_{IL}	Input Low Voltage			-0.1	0.8	V
V_{IH}	Input High Voltage			2	$V_{CC}+1$	
V_{OL1}	Output Low Voltage		$I_{OL} = 2.1$ mA		0.4	V
V_{OH1}	Output High Voltage		$I_{OH} = -400\ \mu A$	2.4		
V_{OL2}	Output Low Voltage		$I_{OL} = 10\ \mu A$		0.2	V
V_{OH2}	Output High Voltage		$I_{OH} = -10\ \mu A$	$V_{CC} - 0.2$		
f_{SK}	SK Clock Frequency	NM93C46A	(Note 5)	0	1	
		NM93C46AE		0	1	MHz
		NM93C46AM		0	0.5	
t_{SKH}	SK High Time	NM93C46A		250		
		NM93C46AE		300		ns
		NM93C46AM		500		
t_{SKL}	SK Low Time	NM93C46A		250		
		NM93C46AE		250		ns
		NM93C46AM		500		
t_{SKS}	SK Setup Time		SK must be at V_{IL} for t_{SKS} before CS goes High	50		ns
t_{CS}	Minimum CS Low Time	NM93C46A	(Note 2)	250		
		NM93C46AE		250		ns
		NM93C46AM		500		

2

t_{CSS}	CS Setup Time	NM93C46AE NM93C46AM		50 100		ns
t_{DH}	D0 Hold Time			10		ns
t_{DIS}	DI Setup Time	NM93C46A NM93C46AE NM93C46AM		100 100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"	NM93C46A NM93C46AE NM93C46AM			500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C46A NM93C46AE NM93C46AM			500 500 1000	ns
t_{SV}	CS to Status Valid	NM93C46A NM93C46AE NM93C46AM			500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C46A NM93C46AE NM93C46AM	CS = V_{IL}		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 3)

$T_A = +25°C$, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/t_{SK} = t_{SKH\ (minimum)} + t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

AC Test Conditions:

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
$4.5V \le V_{CC} \le 5.5V$ (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/0.4 mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

2

Functional Description

The NM93C46A has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8/9 bits carry the op code and the 6/7-bit address for register selection.

All Data-in signals are clocked into the device on the low-to-high SK transition.

Read (READ)

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into an 8- or 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 8- or 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN)

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an WEN instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE)

The ERASE instruction will program all bits in the specified register to the logical '1' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE)

The WRITE instruction is followed by 8 or 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL)

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical '1' state. The Erase All cycle is identical to the ERASE cycle except for the different op-code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. The ERASE ALL instruction is not required, see note below.

Write All (WRALL)

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status.

Erase/Write Disable (WDS)

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

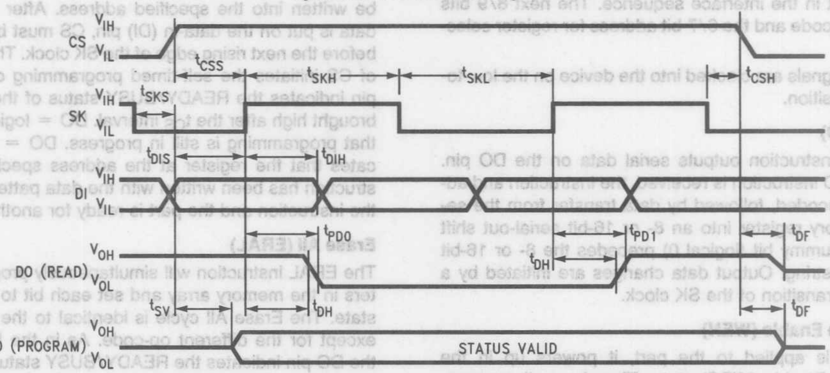
Note: The NM93C46A device does not require an 'ERASE' or 'ERASE ALL' prior to the 'WRITE' and 'WRITE ALL' instructions. The 'ERASE' and 'ERASE ALL' instructions are included to maintain compatibility with the NMOS NMC9346.

Instruction Set

Instruction	Start Bit	Opcode		Address		Data		Comments
				128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1	0	A6–A0	A5–A0			Read Selected Address
ERASE	1	1	1	A6–A0	A5–A0			Erase Selected Address
WRITE	1	0	1	A6–A0	A5–A0	D7–D0	D15–D0	Write Selected Address
WEN	1	0	0	11XXXXX	11XXXX			Program Enable
WDS	1	0	0	00XXXXX	00XXXX			Program Disable
ERAL	1	0	0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0	0	01XXXXX	01XXXX	D7–D0	D15–D0	Program All Addresses

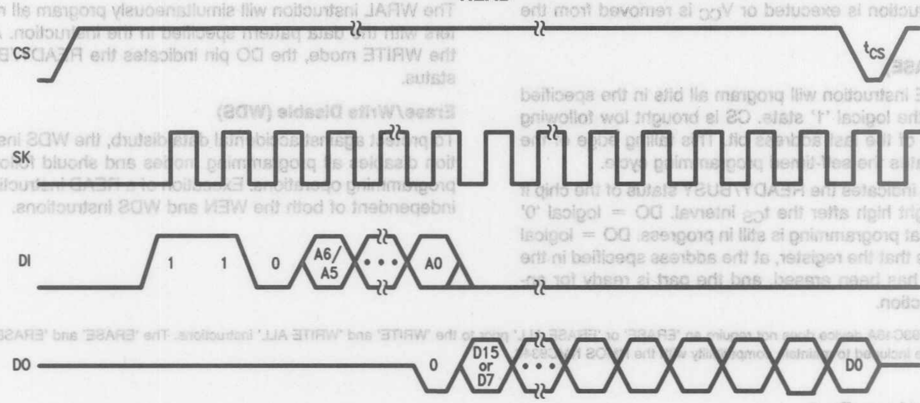
Timing Diagrams

Synchronous Data Timing



TL/D/11042-3

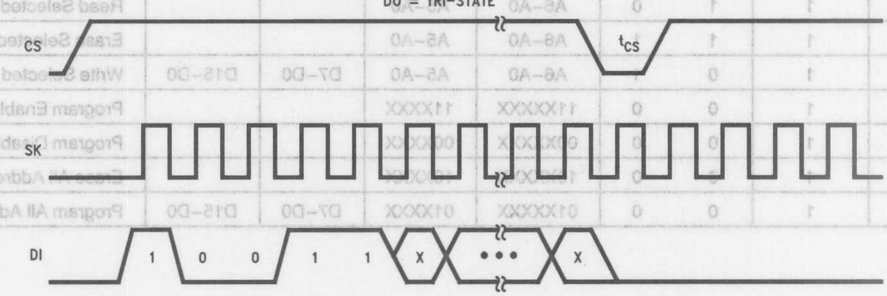
READ



TL/D/11042-4

WEN

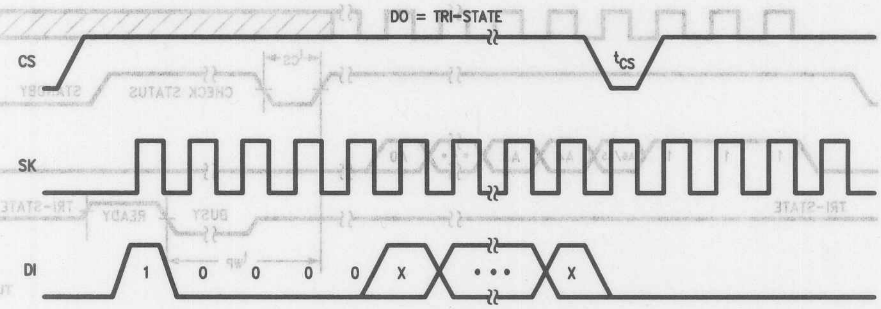
DO = TRI-STATE



TL/D/11042-5

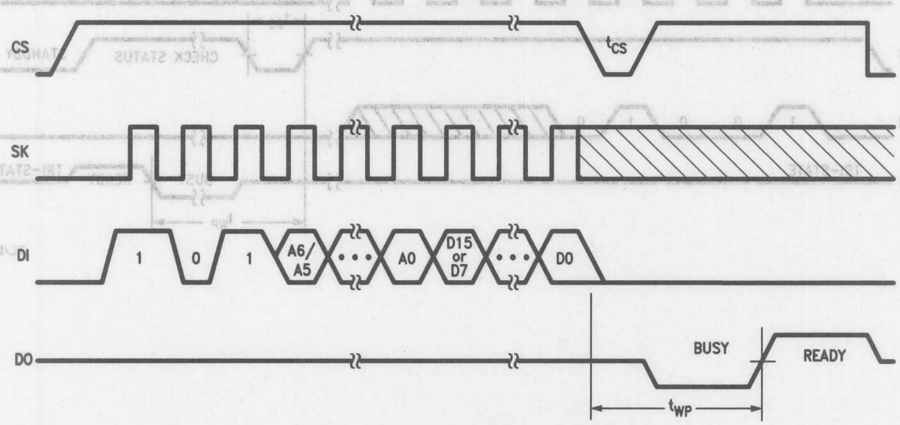
Timing Diagrams (Continued)

WDS



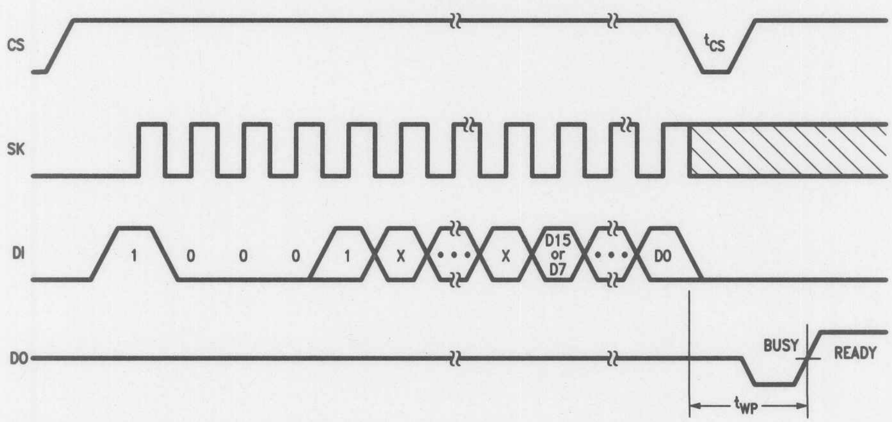
TL/D/11042-6

WRITE



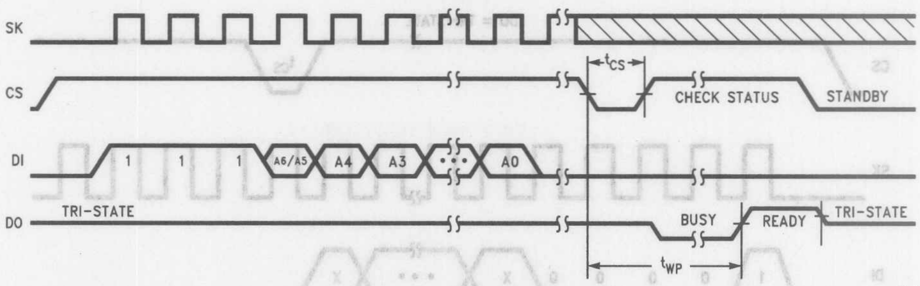
TL/D/11042-7

WRALL



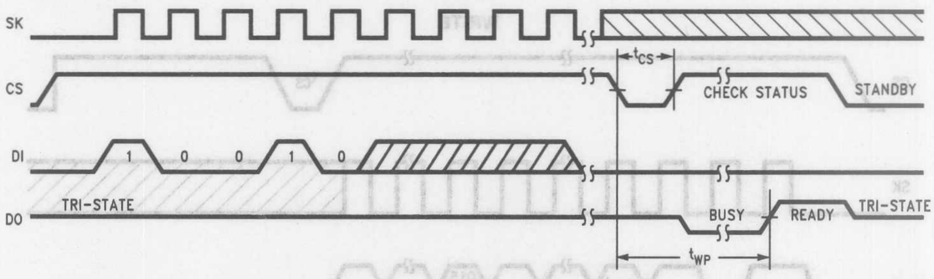
TL/D/11042-8

ERASE



TL/D/11042-9

ERAL



TL/D/11042-10

National Semiconductor

NM93C46AL 1024-Bit Serial EEPROM 64 x 16-Bit or 128 x 8-Bit Configurable with Extended Voltage (2.0V to 5.5V) (MICROWIRE™ Bus Interface)

General Description

The NM93C46AL is 1024 bits of CMOS non-volatile electrically erasable memory organized as either 64 16-bit registers or 128 8-bit registers. The organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, low power consumption and a wide operating voltage range. The NM93C46AL is available in an SO package for space considerations.

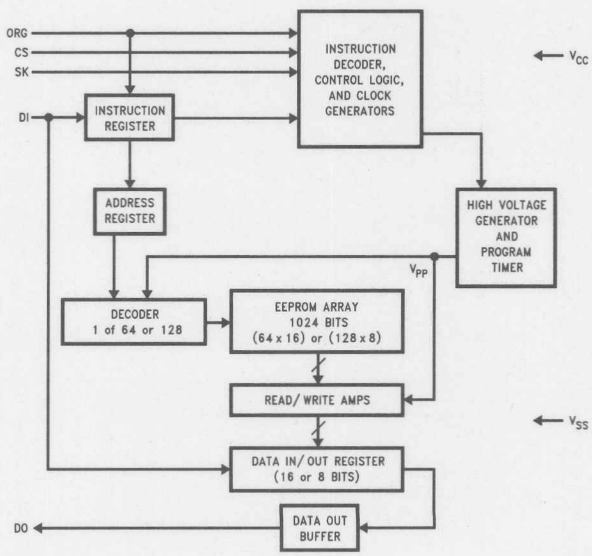
The interface is MICROWIRE™ compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C46AL: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All. The READY/BUSY status is available on the D_{OUT} pin during programming.

The NM93C46AL is compatible with National Semiconductor's NM93C46L if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC} to default to the 64 x 16 configuration.

Features

- 2.0V to 5.5V operation in read mode
- 2.5V to 5.5V operation in all other modes
- Typical active current of 400 μA; typical standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

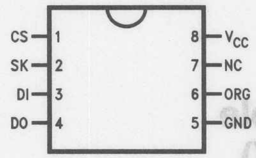
Block Diagram



TL/D/11330-1

Connection Diagrams

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/11330-2

Top View

NS Package Number N08E and M08A

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Organization

Ordering Information

Commercial Temp. Range (0°C to +70°C)

Order Number
NM93C46ALN NM93C46ALM8

Extended Temp. Range (−40°C to +85°C)

Order Number
NM93C46ALEN NM93C46ALEM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 Seconds)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM93C46AL	0°C to +70°C
NM93C46ALE	−40°C to +85°C
Power Supply Range	
Read Mode	2.0V to 5.5V
Bulk (ERAL/WRALE) Programming	3.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics: 2V < V_{CC} < 4.5V

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK = 250 kHz		1	mA
I_{CCS}	Standby Current	CS = V_{IL}		50	μA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC} (Note 4)		±1	μA
	Pin 6			±10	
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}		±1	μA
V_{IL}	Input Low Voltage		−0.1	0.2 V_{CC}	V
V_{IH}	Input High Voltage		0.8 V_{CC}	V_{CC} + 1	
V_{OL}	Output Low Voltage	I_{OL} = 10 μA		0.1 V_{CC}	V
V_{OH}	Output High Voltage	I_{OH} = −10 μA	0.9 V_{CC}		
f_{SK}	SK Clock Frequency	(Note 5)	0	250	kHz
t_{SKH}	SK High Time		1		μs
t_{SKL}	SK Low Time		1		μs
t_{CS}	Minimum CS Low Time	(Note 2)	1		μs
t_{SKS}	SK Setup Time	SK must be at V_{IL} for t_{SKS} before CS goes high	0.2		μs
t_{CSS}	CS Setup Time		0.2		μs
t_{DIS}	DI Setup Time		0.4		μs
t_{CSH}	CS Hold Time		0		μs
t_{DIH}	DI Hold Time		0.4		μs
t_{PD1}	Output Delay to "1"			2	μs
t_{PD0}	Output Delay to "0"			2	μs
t_{SV}	CS to Status Valid			1	μs
t_{DF}	CS to DO in	CS = V_{IL}		0.4	μs
t_{WP}	Write Cycle Time			15	ms
t_{DH}	D0 Hold Time		10		ns

DC and AC Electrical Characteristics: 4.5V < V_{CC} < 5.5V

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CCA}	Operating Current	NM93C46AL NM93C46ALE	CS = V_{IH}, SK = 1 MHZ SK = 0.5 MHz		1	mA
I_{CCS}	Standby Current		CS = V_{IL}		50	μA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC} (Note 4)			±1	μA
	Pin 6				±10	
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}			±1	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 V_{CC} + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage		I_{OL} = 2.1 mA I_{OH} = −400 μA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage		I_{OL} = 10 μA I_{OH} = −10 μA	 V_{CC} − 0.2	0.2	V
f_{SK}	SK Clock Frequency	NM93C46AL NM93C46ALE	(Note 5)	0 0	1 0.5	MHz
t_{SKH}	SK High Time	NM93C46AL NM93C46ALE		250 300		ns
t_{SKL}	SK Low Time			250		ns
t_{SKS}	SKS Setup Time		SK Must Be at V_{IL} for t_{SKS} before CS Goes High	50		ns
t_{CS}	Minimum CS Low Time		(Note 2)	250		ns
t_{DH}	DO Hold Time			10		ns
t_{CSS}	CS Setup Time			50		ns
t_{DIS}	DI Setup Time	NM93C46AL NM93C46ALE		100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			100 200		ns
t_{PD1}	Output Delay to "1"				500	ns
t_{PD0}	Output Delay to "0"				500	ns
t_{SV}	CS to Status Valid				500	ns
t_{DF}	CS to DO in TRI-STATE		CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 3)

$T_A = +25°C$, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IH}	Input Capacitance	5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle (This is shown in the opcode diagrams in the following pages).

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH(minimum)} + t_{SKL(minimum)}$ for shorter SK cycle time operation.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
$2.0V \leq V_{CC} < 4.5V$ (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	$\pm 10\ \mu A$
$4.5V \leq V_{CC} \leq 5.5V$ (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/0.4 mA

Output Load: 1 TTL Gate (C_L = 100 pF)

2

bits carry the op code and the 6/7-bit address for register selection.

All Data-in signals are clocked into the device on the low-to-high SK transition.

Read (READ)

The READ instruction outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into an 8- or 16-bit serial-out shift register. A dummy bit (logical 0) precedes the 8- or 16-bit data output string. Output data changes are intiated by a low to high transition of the SK clock.

Erase/Write Enable (WEN)

When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (WDS) state. Therefore, all programming modes must be preceded by an WEN instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (WDS) instruction is executed or V_{CC} is removed from the part.

Erase (ERASE)

This ERASE instruction will program all bits in the specified register to the logical "1" state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. DO = logical 0 indicates that programming is still in progress. DO = logical 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL)

The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state. The ERAL cycle is identical to the ERASE cycle except for the different op-code. As the ERASE mode, the DO pin indicates the READY/BUSY status of the chip if CS is brought high after the t_{CS} interval. The ERAL instruction is not required, see note below.

Write All (WRALL)

The WRALL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status.

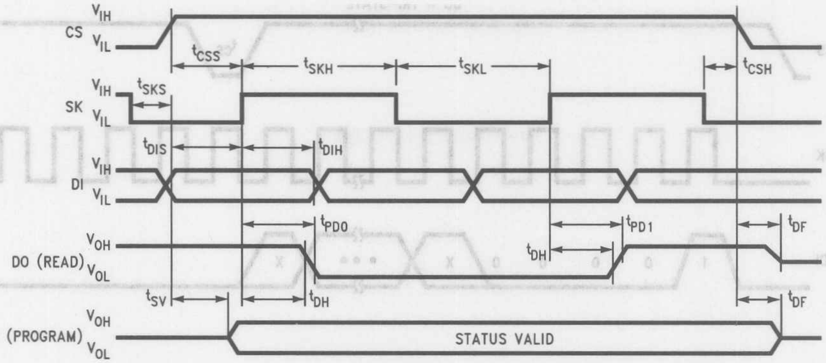
Erase/Write Disable (WDS)

To protect against accidental data disturb, the WDS instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the WEN and WDS instructions.

Note: The NM93C46AL device does not require an "ERASE" or "ERASE ALL" prior to the "WRITE" and "WRITE ALL" instructions. The "ERASE" and "ERASE ALL" instructions are included to maintain compatibility with the NMOS NMC9346.

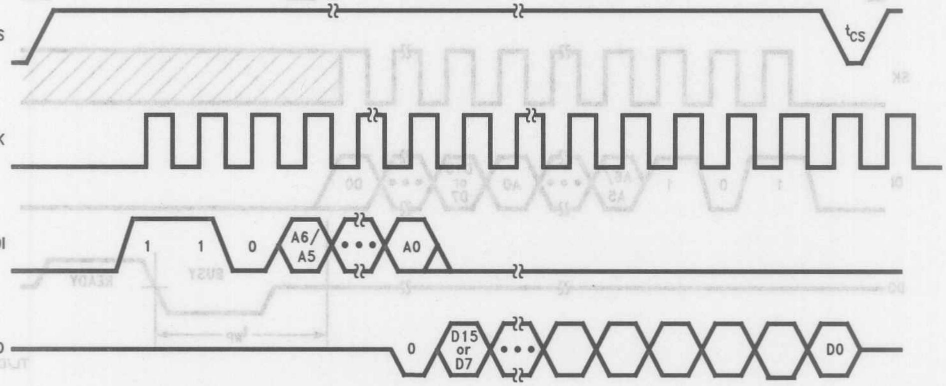
Instruction Set

Instruction	Start Bit	Opcode		Address		Data		Comments
				128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1	0	A6–A0	A5–A0			Read Selected Address
ERASE	1	1	1	A6–A0	A5–A0			Erase Selected Address
WRITE	1	0	1	A6–A0	A5–A0	D7–D0	D15–D0	Write Selected Address
WEN	1	0	0	11XXXXX	11XXXX			Program Enable
WDS	1	0	0	00XXXXX	00XXXX			Program Disable
ERAL	1	0	0	10XXXXX	10XXXX			Erase All Addresses
WRALL	1	0	0	01XXXXX	01XXXX	D7–D0	D15–D0	Program All Addresses



TL/D/11330-3

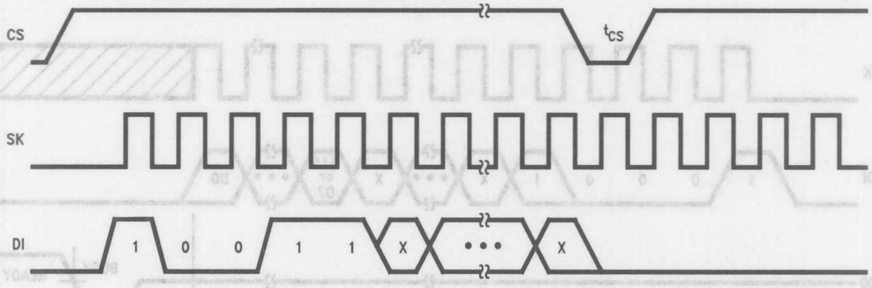
READ



TL/D/11330-4

WEN

DO = TRI-STATE

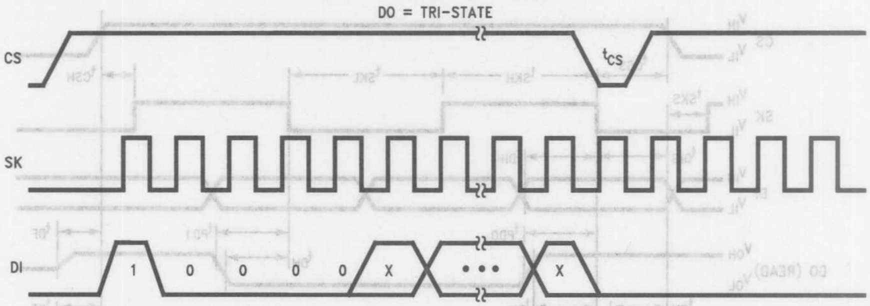


TL/D/11330-5

2

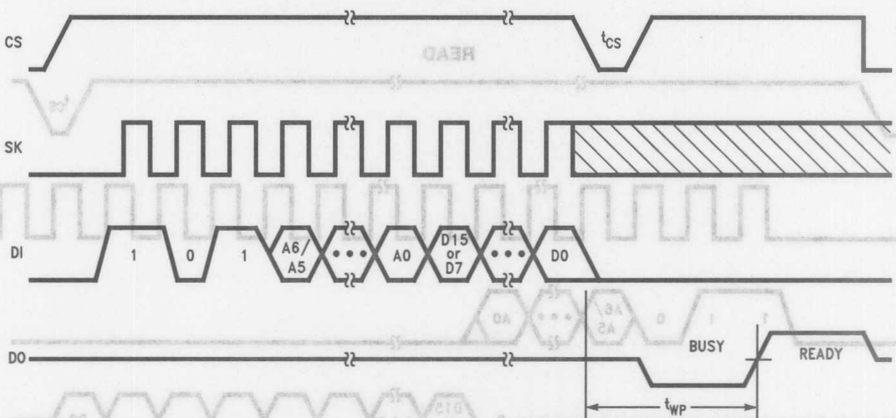
Timing Diagrams (Continued)

WDS



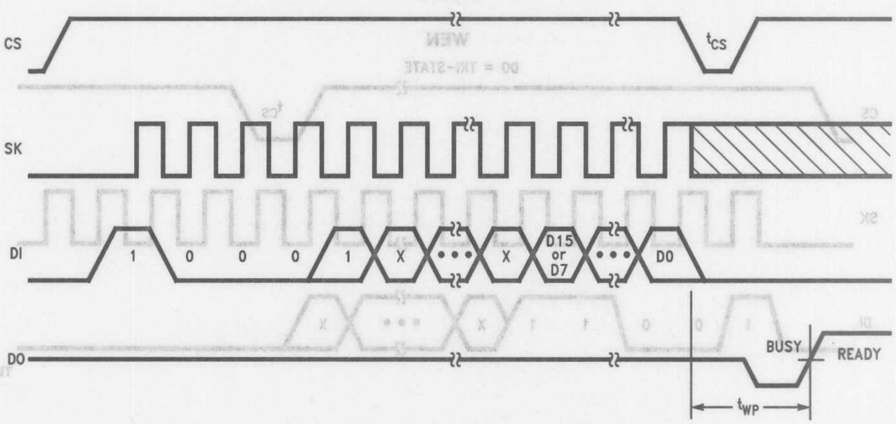
TL/D/11330-6

WRITE



TL/D/11330-7

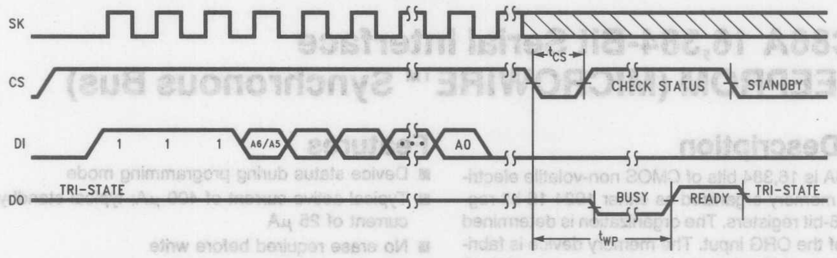
WRALL



TL/D/11330-8

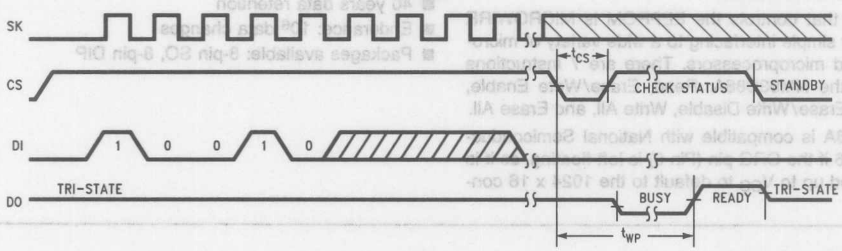
Timing Diagrams (Continued)

ERASE



TL/D/11330-9

ERAL



TL/D/11330-10

2

National Semiconductor

PRELIMINARY

NM93C86A 16,384-Bit Serial Interface CMOS EEPROM (MICROWIRE™ Synchronous Bus)

General Description

The NM93C86A is 16,384 bits of CMOS non-volatile electrically erasable memory organized as either 1024 16-bit registers or 2048 8-bit registers. The organization is determined by the status of the ORG input. The memory device is fabricated using National Semiconductor's floating gate CMOS process for high reliability, high endurance and low power consumption. The NM93C86A is available in an SO package for space considerations.

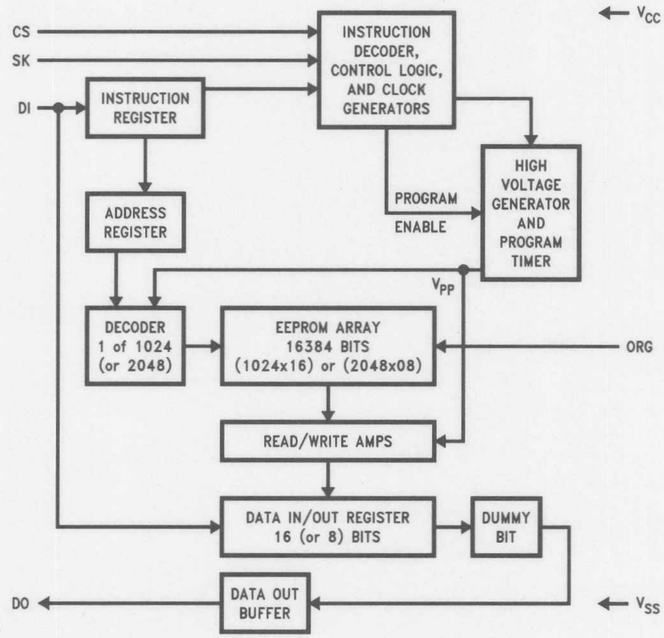
The interface that controls the EEPROM is MICROWIRE compatible for simple interfacing to a wide variety of microcontrollers and microprocessors. There are 7 instructions that operate the NM93C86A: Read, Erase/Write Enable, Erase, Write, Erase/Write Disable, Write All, and Erase All.

The NM93C86A is compatible with National Semiconductor's NM93C46 if the ORG pin (Pin 6) is left floating, as it is internally pulled up to V_{CC} to default to the 1024 x 16 configuration.

Features

- Device status during programming mode
- Typical active current of 400 μA; typical standby current of 25 μA
- No erase required before write
- Reliable CMOS floating gate technology
- MICROWIRE compatible interface
- Self-timed programming cycle
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP

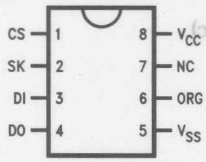
Block Diagram



TL/D/11254-2

Connection Diagram

Dual-In-Line Package (N) and 8-Pin SO (M8)



TL/D/11254–1

Top View
See NS Package Number N08E and M08A

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{SS}	Ground
ORG	Memory Organization Select
NC	Not Connected
V_{CC}	Positive Power Supply

Ordering Information

Commercial Temp Range (0°C to +70°C)

Order Number
NM93C86AN NM93C86AM8

Extended Temp Range (−40°C to +85°C)

Order Number
NM93C86AEN NM93C86AEM8

Military Temp Range (−55°C to +125°C)

Order Number
NM93C86AMN NM93C86AMM8

Office/Distributors for availability and specifications.

Ambient Storage Temperature	$-65°C$ to $+150°C$
All Input or Output Voltages with Respect to Ground	$+6.5V$ to $-0.3V$
Lead Temperature (Soldering, 10 seconds)	$+300°C$
ESD Rating	2000V

NM93C86AE	$-40°C$ to $+85°C$
NM93C86AM	$-55°C$ to $+125°C$
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$ (unless otherwise specified)

Note: Throughout this table, "M" refers to temperature range ($-55°C$ to $+125°C$), not package.

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C86A NM93C86AE NM93C86AM	$CS = V_{IH}$, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		2 2 2	mA
I_{CC2}	Operating Current TTL Input Levels	NM93C86A NM93C86AE NM93C86AM	$CS = V_{IH}$, SK = 1 MHz SK = 1 MHz SK = 0.5 MHz		3 3 4	mA
I_{CC3}	Standby Current	NM93C86A NM93C86AE NM93C86AM	CS = 0V		50 50 100	μA
I_{IL}	Input Leakage	NM93C86A NM93C86AE NM93C86AM	V_{IN} = 0V to V_{CC}	−2.5	2.5	μA
I_{OL}	Output Leakage	NM93C86A NM93C86AE NM93C86AM	V_{IN} = 0V to V_{CC}	−2.5	2.5	μA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage			−0.1 2	0.8 $V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	NM93C86A NM93C86AE NM93C86AM	I_{OL} = 2.1 mA I_{OL} = 2.1 mA I_{OL} = 1.8 mA		0.4 0.4 0.4	V
V_{OH1}	Output High Voltage		I_{OH} = −400 μA	2.4		V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	NM93C86A NM93C86AM	I_{OL} = 10 μA I_{OH} = −10 μA	 $V_{CC} - 0.2$	0.2	V
f_{SK}	SK Clock Frequency	NM93C86A NM93C86AE NM93C86AM		0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM93C86A NM93C86AE NM93C86AM	(Note 2)	250 300 500		ns
t_{SKL}	SK Low Time	NM93C86A NM93C86AE NM93C86AM	(Note 2)	250 250 500		ns
t_{SKS}	SK Setup Time	NM93C86A NM93C86AE NM93C86AM	Relative to CS	50 50 100		ns
t_{CS}	Minimum CS Low Time	NM93C86A NM93C86AE NM93C86AM	(Note 3)	250 250 500		ns

DC and AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$ (unless otherwise specified) (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{CSS}	CS Setup Time	NM93C86A NM93C86AE NM93C86AM	Relative to SK	50 50 100		ns
t_{DH}	D0 Hold Time		Relative to SK	70		ns
t_{DIS}	DI Setup Time	NM93C86A NM93C86AE NM93C86AM	Relative to SK	100 200 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93C86A NM93C86AE NM93C86AM	Relative to SK		500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM93C86A NM93C86AE NM93C86AM	Relative to SK		500 500 1000	ns
t_{SV}	CS to Status Valid	NM93C86A NM93C86AE NM93C86AM	Relative to SK		500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE®	NM93C86A NM93C86AE NM93C86AM	$CS = V_{IL}$		100 100 200	ns
t_{WP}	Write Cycle Time				10	ms

Capacitance (Note 4)

$T_A = 25°C, f = 1.0$ MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Pulse Levels	0.4V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2.0V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SK frequency specification specifies a mimimum SK clock period of 1 μs, therefore in an SK clock cycle $t_{SKH} + t_{SKL}$ must be greater than or equal to 1 μs. For example if $t_{SKL} = 250$ ns then the minimum $t_{SKH} = 750$ ns in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

2

Instruction Set for NM93C86A

The NM93C86A has 7 instructions as described below. Note that the MSB of any instruction is a "1" and is viewed as a start bit in the interface sequence. The next 2 bits carry the op code, the next 10 (or 11) bits carry the address for selection of 1 of 1024 16-bit registers or 1 of 2048 8-bit register, depending on memory array organization.

1024 by 16-Bit Organization (ORG = V_{CC} or NC)

Instruction	SB	Op Code 2 Bits	Address 10 Bits	Data 16 Bits	Comments
READ	1	10	A9–A0		Read data stored in selected register.
EWEN	1	00	11XXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXX		Disables all programming modes.
ERASE	1	11	A9–A0		Erase selected register.
WRITE	1	01	A9–A0	D15–D0	Writes data pattern D15–D0 into selected register.
ERAL	1	00	10XXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXX	D15–D0	Writes data pattern D15–D0 into all registers.

2048 by 8-Bit Organization (ORG = V_{SS})

Instruction	SB	Op Code 2 Bits	Address 11 Bits	Data 8 Bits	Comments
READ	1	10	A10–A0		Read data stored in selected register.
EWEN	1	00	11XXXXXXXXX		Enables programming modes.
EWDS	1	00	00XXXXXXXXX		Disables all programming modes.
ERASE	1	11	A10–A0		Erase selected register.
WRITE	1	01	A10–A0	D7–D0	Writes data pattern D7–D0 into selected register.
ERAL	1	00	10XXXXXXXXX		Erases all registers.
WRAL	1	00	01XXXXXXXXX	D7–D0	Writes data pattern D7–D0 into all registers.

Functional Description

The memory organization is selected by the state of the ORG input pin. If ORG is forced to V_{CC} or left unconnected, the 1024 x 16 memory organization is selected. If ORG is forced to V_{SS}, the 2048 x 8 memory organization is selected.

Read (READ)

The READ instruction outputs serial data on the D0 pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical "0") precedes the serial data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN)

When V_{CC} is applied to the part, it "powers up" in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until a Erase/Write Disable (EWDS) instruction is executed or until V_{CC} is removed from the part.

Erase/Write Disable (EWDS)

To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

In all programming modes the READY/BUSY status of the device can be determined by polling the DO pin. After clocking in the last bit of the instruction sequence and with CS held "high," the DO pin will exit the high impedance state and indicate the READY/BUSY status of the device. DO = logical "0" indicates that programming is still in progress and no other instruction can be executed, DO = logical "1" indicates that the device is READY for another instruction. If CS is forced "low" the DO pin will return to the high impedance state. After the programming cycle has completed and DO = logical "1," the DO pin can be reset back to the high impedance state, by clocking a logical "1" into the DI pin. (This is also performed with the start bit on all opcodes, thus clocking an instruction has the same affect).

register to the logical "1" state. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last address bit (A0) is clocked in. At this point CS, SK and DI become don't care states. After starting an Erase cycle the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been erased.

Write (WRITE)

The WRITE instruction is followed by 16 bits of data (or 8 bits of data depending on the organization selected) to be written into the specified address. Note that if CS is brought "low" before clocking in all of the data bits, then the WRITE instruction will be aborted. The self-timed programming cycle is initiated on the rising edge of the SK clock as the last As in the ERASE instruction, after starting a WRITE cycle, the DO pin indicates the READY/BUSY status of the chip if CS is held "high". DO = logical "0" indicates that programming is still in progress. DO = logical "1" indicates that the register, at the address specified in the instruction, has been written and that the part is ready for another instruction.

Erase All (ERAL)

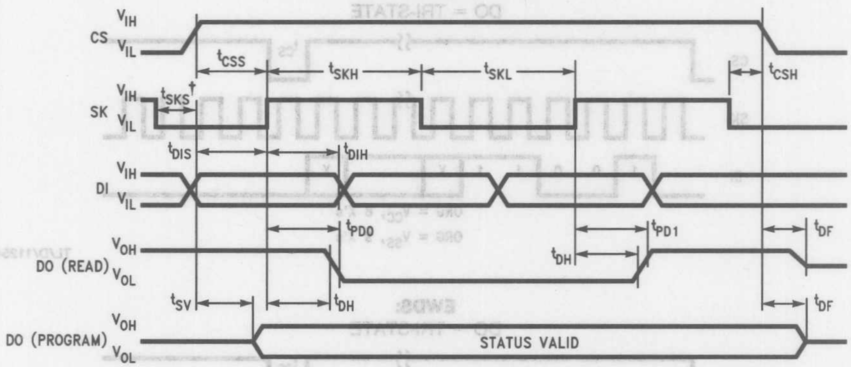
The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical "1" state.

Write All (WRAL)

The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction.

Timing Diagrams

Synchronous Data Timing



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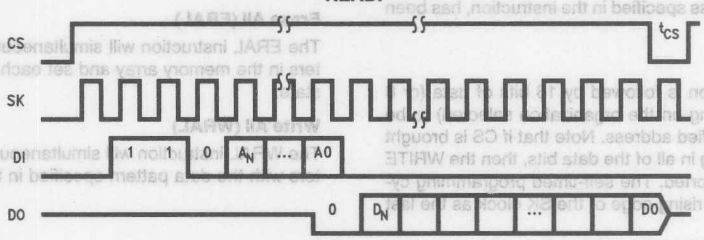
*This is the minimum SK period (See Note 2)

†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

V_{CC} or NC	1024 x 16	A9	D15
V_{SS}	2048 x 8	A10	D7

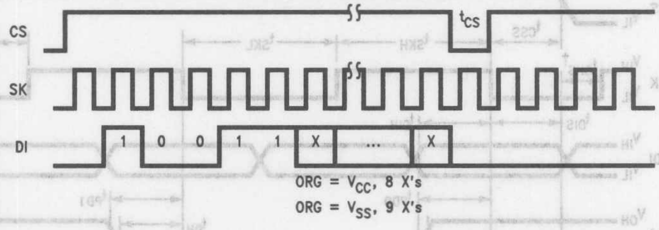
READ:



TL/D/11254-4

EWEN:

DO = TRI-STATE



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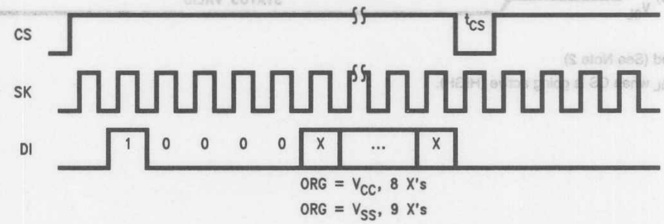
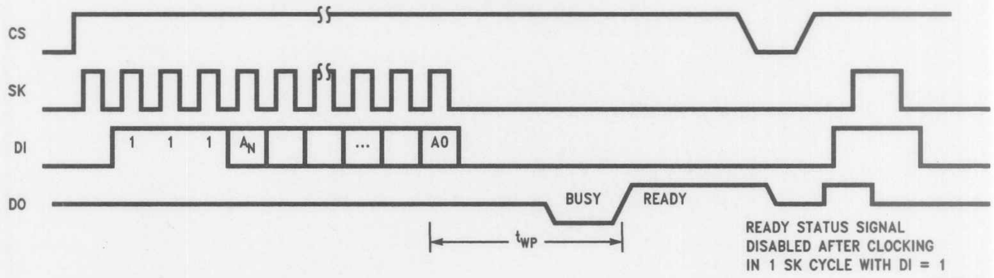
EWDS:

DO = TRI-STATE



TL/D/11254-6

ERASE:



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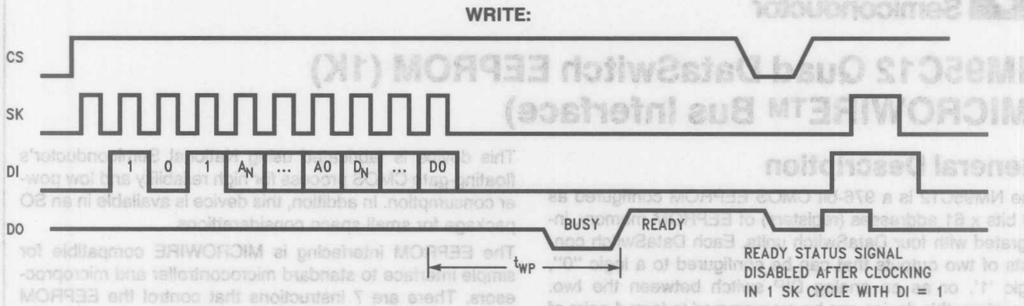
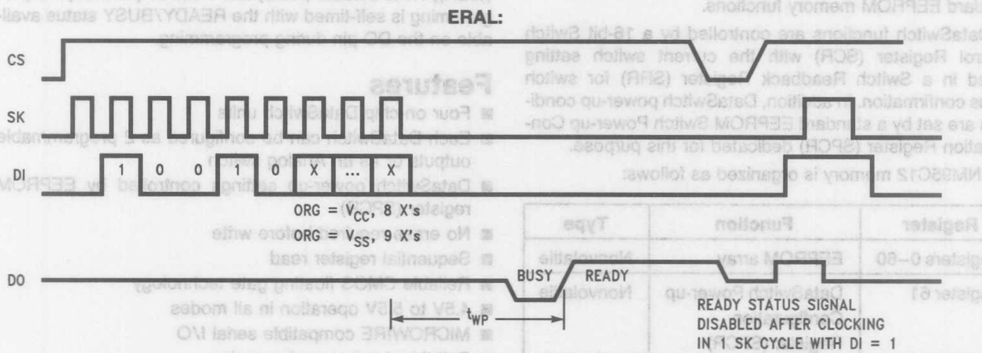
Timing Diagrams (Continued)



TL/D/11254–8



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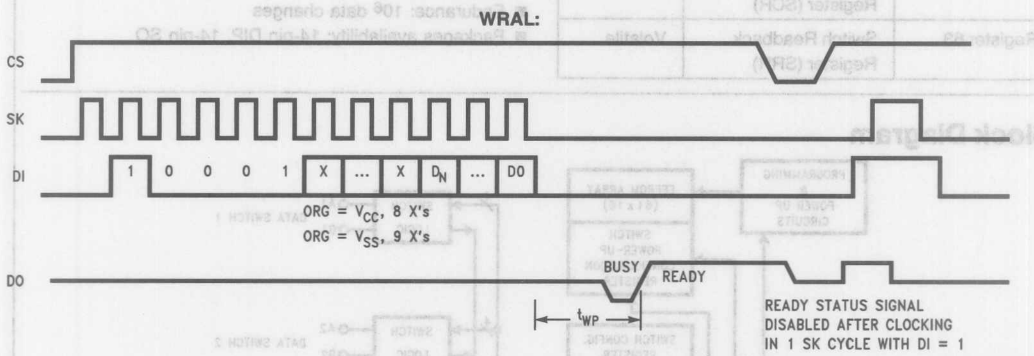


TL/D/11254–10

2

National Semiconductor

NM95C12 Quad DataSwitch EEPROM (1K) (MICROWIRE™ Bus Inferface)

General Description

The NM95C12 is a 976-bit CMOS EEPROM configured as 16 bits x 61 addresses (registers) of EEPROM memory, integrated with four DataSwitch units. Each DataSwitch consists of two outputs that can be configured to a logic "0", logic '1', or as an analog DIP switch between the two. Therefore, this device can be programmed to form 4 pairs of SPST switches or 8 configurable outputs in addition to all standard EEPROM memory functions.

All DataSwitch functions are controlled by a 16-bit Switch Control Register (SCR) with the current switch setting stored in a Switch Readback Register (SRR) for switch status confirmation. In addition, DataSwitch power-up conditions are set by a standard EEPROM Switch Power-up Configuration Register (SPCR) dedicated for this purpose.

The NM95C12 memory is organized as follows:

Register	Function	Type
Registers 0–60	EEPROM array	Nonvolatile
Register 61	DataSwitch Power-up Configuration Register (SPCR)	Nonvolatile
Register 62	Switch Control Register (SCR)	Volatile
Register 63	Switch Readback Register (SRR)	Volatile

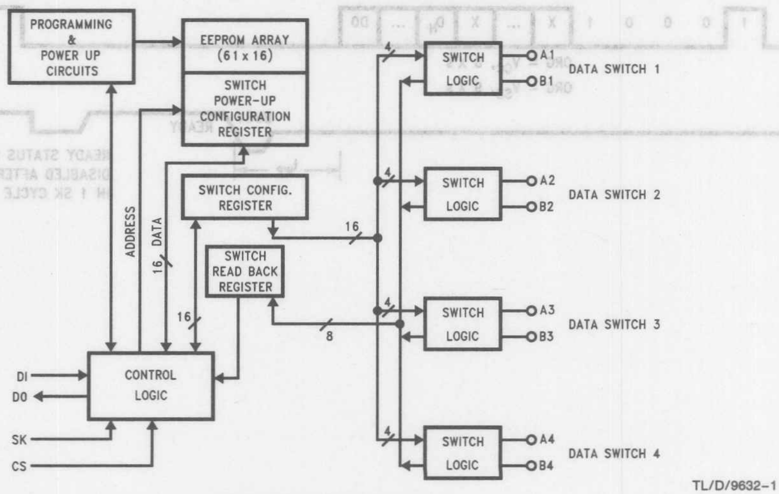
This device is fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. In addition, this device is available in an SO package for small space considerattions.

The EEPROM interfacing is MICROWIRE compatible for simple interface to standard microcontroller and microprocesors. There are 7 instructions that control the EEPROM memory: Read (READ), Write (WRITE), Write Enable (WEN), Write Disable (WDS) and Write all (WRALL). All programming is self-timed with the READY/BUSY status available on the DO pin during programming.

Features

- Four on-chip DataSwitch units
- Each DataSwitch can be configured as 2 programmable outputs or as an Analog switch
- DataSwitch power-up settings controlled by EEPROM register (SPCR)
- No erase required before write
- Sequential register read
- Reliable CMOS floating gate technology
- 4.5V to 5.5V operation in all modes
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- 40 year data retention
- Endurance: 10^6 data changes
- Packages availability: 14-pin DIP, 14-pin SO

Block Diagram

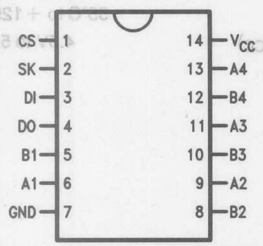


TL/D/9632–1

FIGURE 1. Block Diagram

Connection Diagrams

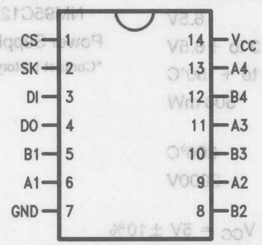
SO Package



TL/D/9632-3

Top View
Order Number NM95C12M, NM95C12EM and NM95C12MM
See NS Package M14A

Dual-In-Line Package



TL/D/9632-2

Top View
Order Number NM95C12N, NM95C12EN and NM95C12MN
See NS Package N14A

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
A1–A4 B1–B4	Switch Terminals

Pin Descriptions

Pin Name	Description
CS	Chip Select, Input—This input must be high while communicating with the NM95C12. When this input is LOW, the chip is powered down into the standby mode. It should be noted that the CS does not control the A1 through A4 and B1 through B4 outputs and hence has no effect on them. The CS input must be made LOW after completing an instruction to prepare the control logic to accept the next instruction. If the CS input becomes LOW prematurely, the operation in progress is aborted. If programming the E^2 memory is in progress and the CS goes LOW, the programming is not aborted but will proceed to its normal completion.
SK	Serial Clock, Input—This input is used for clocking the serial I/O. The CS input must be high for clocking to have any effect. Information presented on the DI input will be shifted into the device on the LOW to HIGH transition of the clock. Information from the device will be available on the DO output serially, in response to the LOW to HIGH transition of the clock.
DI	Serial Data In, Input—All information needed for the operation of the device is entered serially from this input. HIGH represents logic '1' and LOW represents logic '0'. The entry order is most significant bit first and least significant bit last.
DO	Serial Data Out, Output, TRI-STATE®—When data is read, data from the addressed location will be available on this output serially, in sync with the LOW to HIGH transitions on the SK input. Normally the DO pin is in high impedance state. During a read instruction, when the last bit of the address is shifted in, the DO will go LOW indicating that data will follow. The data will follow in response to the clock transitions. The data will come out most significant bit first and least significant bit last. During E^2 programming operations, this output is also used as the status indicator. During programming operations, LOW indicates Busy (programming in progress) and HIGH indicates Ready. The DO output will be in the high impedance state if the CS input is LOW unconditionally.
A1–A4 B1–B4	Switch Terminals—These pins provide the simulated DIP switch features and hence are called terminals. The behavior of these pins is determined by the settings in the Switch Configuration Register and are independent of the CS input.
V_{CC}	Power Supply.
GND	Ground.

Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	6.5V
Voltage at Any Pin	−0.3 to +6.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation @25°C	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating	2000V

NM95C12E	−40°C to +85°C
NM95C12M*	−55°C to +125°C
Power Supply Voltage (V_{CC})	4.5V to 5.5V

*Contact factory for availability

DC Electrical Characteristics V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	$C_S = V_{IH}$, SK = 1 MHz		4	mA
I_{CC2}	Operating Current TTL Input Levels	$C_S = V_{IH}$, SK = 1 MHz		6	mA
I_{CC3}	Standby Current CMOS Input Levels on Switches	C_S = 0V		50	µA
I_{CC4}	Standby Current TTL Input Levels on Switches	C_S = 0V		800	µA
I_{IL} I_{OL}	Input Leakage (Note 4) Output Leakage	V_{IN} = 0V to V_{CC} (Note 4)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		−0.1 2.0	0.8 V_{CC} + 1	V V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 2.1 mA I_{OH} = −400 µA	 2.4	0.4	V V
R_{ON}	Switch On Resistance			200	Ω
R_{OFF}	Switch Off Resistance		10		MΩ
V_S	Maximum Voltage Allowed on any Switch Terminal			V_{CC} + 1	V
I_S	Max Current Allowed through Switch Terminals			10	mA

AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
f_{SK}	SK Clock Frequency	NM95C12 NM95C12E NM95C12M	(Note 5)	0 0 0	1 1 0.5	MHz
t_{SKH}	SK High Time	NM95C12 NM95C12E NM95C12M		250 300 500		ns
t_{SKL}	SK Low Time	NM95C12 NM95C12E NM95C12M		250 250 500		ns
t_{SKS}	SK Setup	NM95C12 NM95C12E NM95C12M		50 50 100		ns ns ns
t_{CS}	Minimum CS Low Time	NM95C12 NM95C12E NM95C12M	(Note 2)	250 250 500		ns
t_{CSS}	CS Setup Time	NM95C12 NM95C12E NM95C12M		50 50 100		ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{PUSR}	Power Up Slew Rate			1		ms
t_{DIS}	DI Setup Time	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{CSH}	CS Hold Time			0		ns
t_{DIH}	DI Hold Time			20		ns
t_{PD1}	Output Delay to "1"	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{PD0}	Output Delay to "0"	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{SV}	CS to Status Valid	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{DF}	CS to DO in TRI-STATE	NM95C12 NM95C12E NM95C12M	$CS = V_{IL}$		100 100 200	ns
t_{ISWD}	Switch Delay from Switch Input	NM95C12 NM95C12E NM95C12M			250 250 500	ns
t_{SWPD0}	Switch Delay to 0 from Config. Change	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{SWPD1}	Switch Delay to 1 from Config. Change	NM95C12 NM95C12E NM95C12M			500 500 1000	ns
t_{SWS}	A1–A4, B1–B4 Setup Time for SRR Read	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{SWH}	A1–A4, B1–B4 Hold Time for SRR Read	NM95C12 NM95C12E NM95C12M		100 100 200		ns
t_{WP}	Write Cycle Time				10	ms
t_{DH}	DO Hold Time			10		ns

Capacitance (Note 3)

$T_A = 25°C$, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

Note 1: Stress ratings above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliabilty.

Note 2: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagrams in the following pages.)

Note 3: This parameter is periodically sampled and not 100% tested.

Note 4: Typical leakage values are in the 20 nA range.

Note 5: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKH\ (minimum)} = t_{SKL\ (minimum)}$ for shorter SK cycle time operation.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Level	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
$4.5V \le V_{CC} \le 5.5V$ (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	−2.1 mA/0.4 mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

function blocks:

- EEPROM memory array: Addresses 0–60
- Switch Control Registers:
  Switch Power-up Configuration Register (SPCR)
  Switch Control Register (SCR)
  Switch Readback Register (SRR)

ADDRESS SPACE

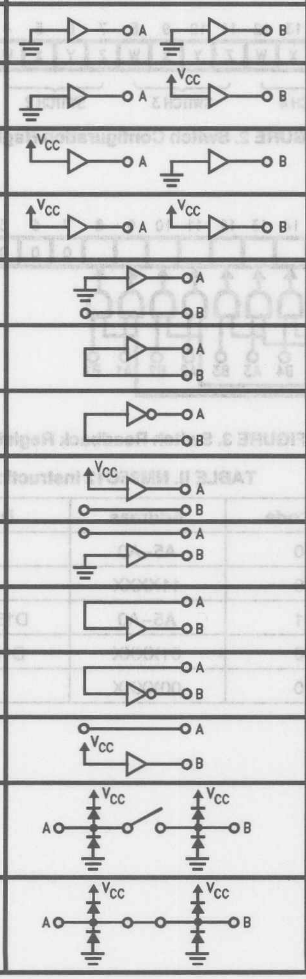
Registers 0–60 of the E[2]PROM are available to the user as general purpose non-volatile memory. Data may be read or programmed into this memory using the appropriate instructions. Address location 61 is an E[2] location which also can switch configuration information automatically on power-up (SPCR).

The switch Control Register (SCR) is located at address 62. The SCR is not an E[2] location and hence is volatile. It does not have endurance limits or programming time requirements associated with it, allowing the switches to be reconfigured an unlimited number of times.

The SCR is automatically loaded from address 61 on power-up. The SCR controls the switch logic and hence the behavior of the terminals A1 through A4 and B1 through B4.

Located at address 63 is the Switch Readback Register (SRR). This is a read only register.

TABLE I. Switch Configurations



MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0, B = 0
1	0	0	0	1		A = 0, B = 1
2	0	0	1	0		A = 1, B = 0
3	0	0	1	1		A = 1, B = 1
4	0	1	0	0		A = 0, B = TRI-STATE
5	0	1	0	1		A = B
6	0	1	1	0		A = $\overline{B}$
7	0	1	1	1		A = 1, B = TRI-STATE
8	1	0	0	0		A = TRI-STATE, B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = $\overline{A}$
11	1	0	1	1		A = TRI-STATE, B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

2

four 4-bit fields. Each field controls its corresponding switch control logic. The individual bits in each field are labelled W, X, Y, and Z. Table I shows the relationship between these bit values and the resulting behavior of the terminals. It should be remembered that the CS input has no effect on the behavior of the terminals.

SWITCH READBACK REGISTER

The SRR allows the current logic level present at the switch terminals to be read back via the Microwire bus. The SRR is loaded by the rising edge of SK immediately after the last instruction bit is clocked in (The same clock edge that loads A0). The SRR is loaded on this clock edge only when register 63 (Switch Readback Register) is being read. In the case of switch mode 13 (Analog switch mode), the SRR will not report the actual levels present at the terminals due to this done to avoid ambiguous logic levels which could exist when the device is used in the analog switch mode.

The bit assignments and conceptual function of the SRR is shown in *Figure 3*. As shown, only bits 15 thru 8 are used, and bits 7 thru 0 are always read as logical 0. The SRR is a Read-Only register and if it is written, the device will not perform a write or generate a Ready/Busy status.

INSTRUCTION SET

The NM95C12 instruction set contains five instructions, and each instruction is ten bits long. The first 2 bits of the instruction are the start bits (SB) and are always a logical "01", followed by the op code (2 bits) and the address field (6 bits). The WRITE and WRALL instructions are followed by sixteen bits of data (D15–D0) which is written into the memory. Table II is a list of the instructions and their format.

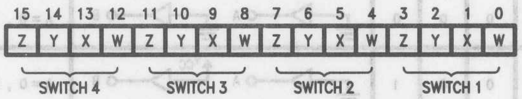

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FIGURE 2. Switch Configuration Register (SCR)

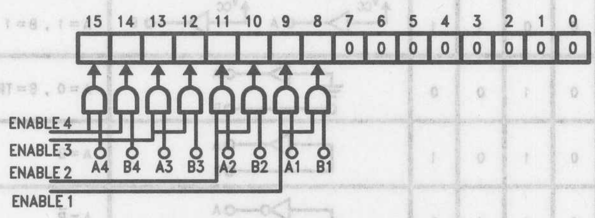

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FIGURE 3. Switch Readback Register (SRR)

TABLE II. NM95C12 Instructions

Instruction	SB	Op Code	Address	Data	Comments
READ	01	10	A5–A0		Reads data at selected address.
WEN	01	00	11XXXX		Enables all programming modes.
WRITE	01	01	A5–A0	D15–D0	Writes selected register.
WRALL	01	00	01XXXX	D15-D0	Writes all registers.
WDS	01	00	00XXXX		Disables all programming modes.

Functional Description (Continued)

WDS (Write Disable): When this instruction is issued, all programming modes are disabled. Any attempt to write into a disabled device is ignored. The NM95C12 powers up in the disabled state. The WEN is the only instruction that enables the device. The write disable operation has no effect on read operations.

WRALL (Write All): When this instruction is executed, the NM95C12 bulk-programs the same 16-bit data pattern into all of its E^2 memory locations (address 0 through 61). The SCR is unaffected since it is not an E^2 location. However, since the SPCR is included in the EEPROM array it will be programmed. The data pattern must follow immediately after the last bit of this instruction. The chip enters into the self-timed program mode after CS is brought low, before the next rising edge of SK.

WEN (Write Enable): This instruction is used to enable all programming modes. The circuits will remain enabled until the WDS instruction disables them. The NM95C12 powers up in the disabled state and hence WEN must be executed prior to any programming instructions.

WRITE (Write/Program): This instruction writes a 16-bit data word into the address location specified by the A_0–A_5 bits of the instruction. The 16 data bits must follow the last bit of the instruction. After loading the WRITE instruction and the 16-bit data, the chip enters into the self-timed program mode when CS is brought low before the next rising edge of the SK clock. If the addressed location is the SCR, then the chip does not enter into the self-timed E^2 programming mode (the SCR is not an E^2 location) but loads the switch configuration data into the SCR. The WRITE instruction can only be aborted by deselecting the chip (CS LOW) before entering all the instruction bits.

READ (Read): This instruction reads the data from the addressed location. As before, the instruction also contains the address. The data will come out serially on the D0 output on the rising edge of the clock. A logical '0' precedes the 16-bit data (dummy bit).

The NM95C12 has a convenient feature called sequential register read. Normally, the CS input is made LOW after the last data bit is shifted out. However, if the CS input is left HIGH and clocking continues, data from the next address location will be delivered on the D0 pin. This sequential read can continue indefinitely whereby the address is automatically incremented after delivering 16 bits of data. It should be noted that in the sequential register read mode, address wrap-around will occur from Amax–Amin.

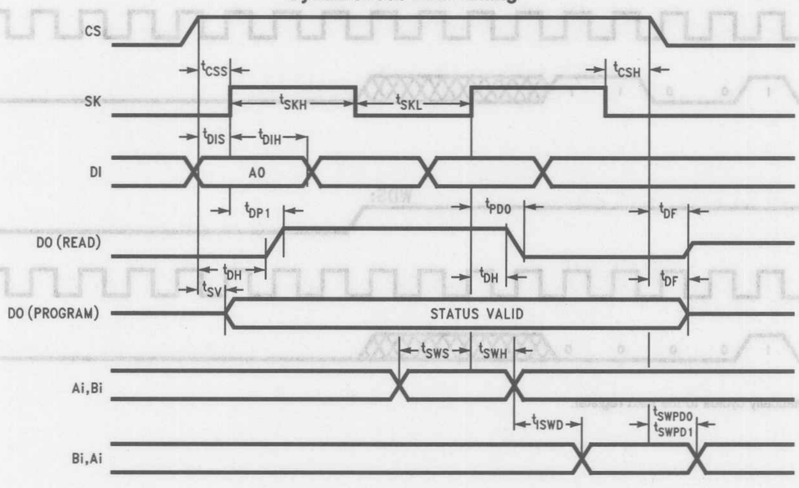
During a sequential register read there will be a dummy bit preceding the first word read, after which, the bit stream will be continuous without any dummy bits separating the data words.

Ready/Busy Indication

Programming an E^2 memory takes several milliseconds. Unlike some devices which require the user to keep track of the elapsed time to ensure completion of the programming cycle, the NM95C12 contains an on-chip timer. The timer starts when the CS input goes LOW after the last data bit is entered. After entering a programming cycle (CS forced LOW), the timer status may be observed by forcing the CS input back HIGH. The timer status is available on the D0 pin if the CS input is forced HIGH within one ms of starting the programming cycle. LOW on the D0 pin indicates that the programming is still in progress while HIGH indicates the device is READY for the next instruction. It should be noted that if the CS input is made HIGH for status observation, it must be made LOW when READY is indicated before loading the next instruction.

Timing Diagrams

Synchronous Data Timing



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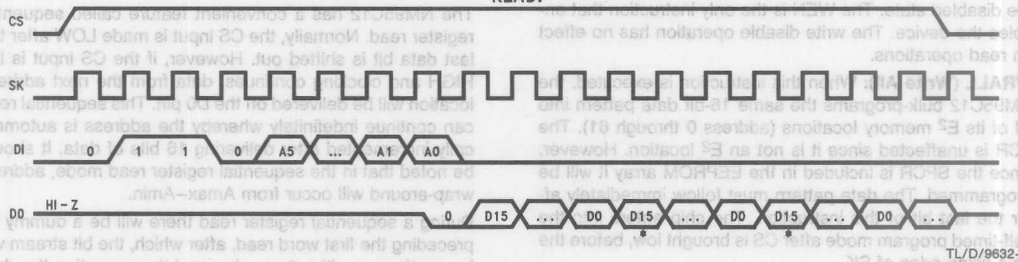
†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

Timing Diagrams (Continued)

Instruction Sequence

READ:



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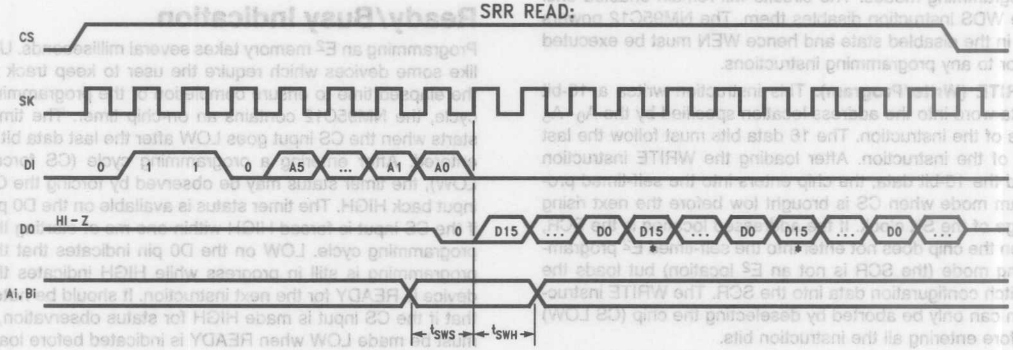
SRR READ:



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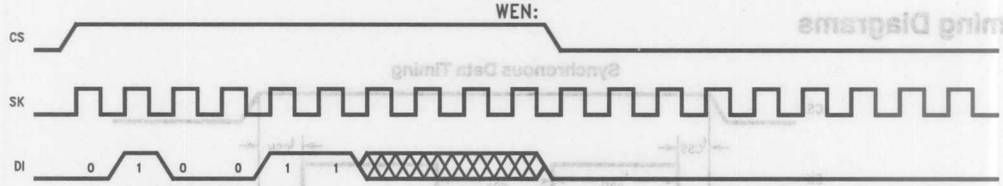
WEN:



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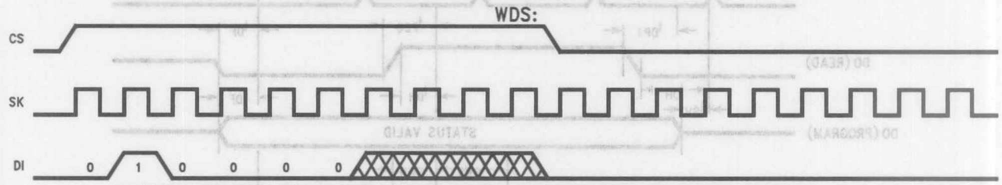
WDS:



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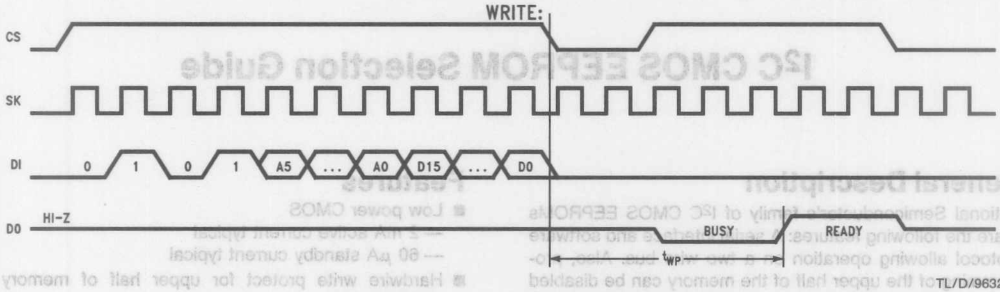
*The memory automatically cycles to the next register.

Timing Diagrams (Continued)

Instruction Sequence (Continued)



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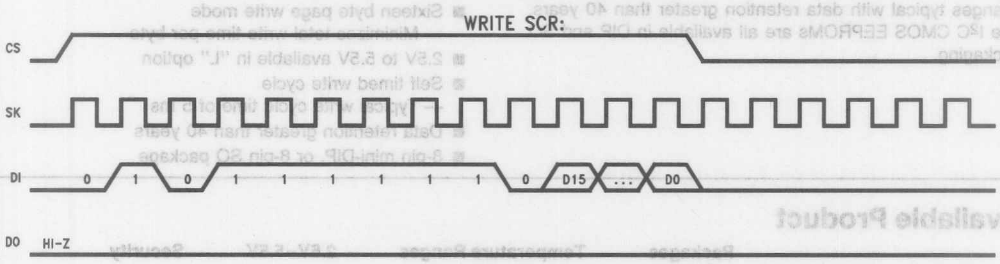

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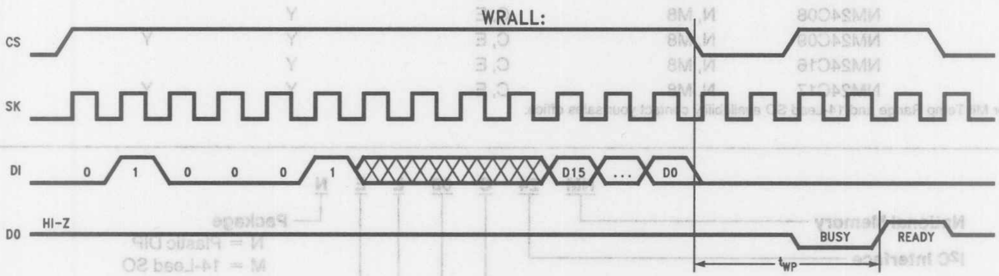

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2

I^2C CMOS EEPROM Selection Guide

General Description

National Semiconductor's family of I^2C CMOS EEPROMs share the following features: A serial interface and software protocol allowing operation on a two wire bus. Also, programming of the upper half of the memory can be disabled by connecting the WP pin to V_{CC} on certain members of the family.

National Semiconductor EEPROMs offer 1 million data changes typical with data retention greater than 40 years. The I^2C CMOS EEPROMs are all available in DIP and SO packaging.

Features

- Low power CMOS
  - — 2 mA active current typical
  - — 60 µA standby current typical
- Hardwire write protect for upper half of memory on 03/05/09/17
- 2-wire serial interface
- Bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- 2.5V to 5.5V available in "L" option
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Data retention greater than 40 years
- 8-pin mini-DIP, or 8-pin SO package

Available Product

	Packages	Temperature Ranges	2.5V–5.5V	Security
NM24C02	N, M8	C, E	Y	
NM24C03	N, M8	C, E	Y	Y
NM24C04	N, M8	C, E	Y	
NM24C05	N, M8	C, E	Y	Y
NM24C08	N, M8	C, E	Y	
NM24C09	N, M8	C, E	Y	Y
NM24C16	N, M8	C, E	Y	
NM24C17	N, M8	C, E	Y	Y

*For Mil Temp Range and 14-Lead SO availability contact your sales office.

NM 24 C 08 L E N

National Memory — NM

I^2C Interface — 24

CMOS — C

Memory Size — 08
- 02 = 2 kbit
- 03 = 2 kbit w/write protect
- 04 = 4 kbit
- 05 = 4 kbit w/write protect
- 08 = 8 kbit
- 09 = 8 kbit w/write protect
- 16 = 16 kbit
- 17 = 16 kbit w/write protect

Operating Voltage Range — L
- No Entry = 4.5V to 5.5V
- L = 2.5V to 5.5V

Operating Temperature Range — E
- No Entry = 0°C to +70°C
- E = −40°C to +85°C
- M = −55°C to +125°C

Package — N
- N = Plastic DIP
- M = 14-Lead SO
- M8 = 8-Lead SO

National Semiconductor

NM24C02/C04/C08/C16 2K-/4K-/8K-/16K-Bit Serial EEPROM (I²C Synchronous 2-Wire Bus)

General Description

The NM24C02/C04/C08/C16 devices are 2048/4096/8192/16,384 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I²C 2-wire protocol and are designed to minimize device pin count and simplify PC board layout requirements.

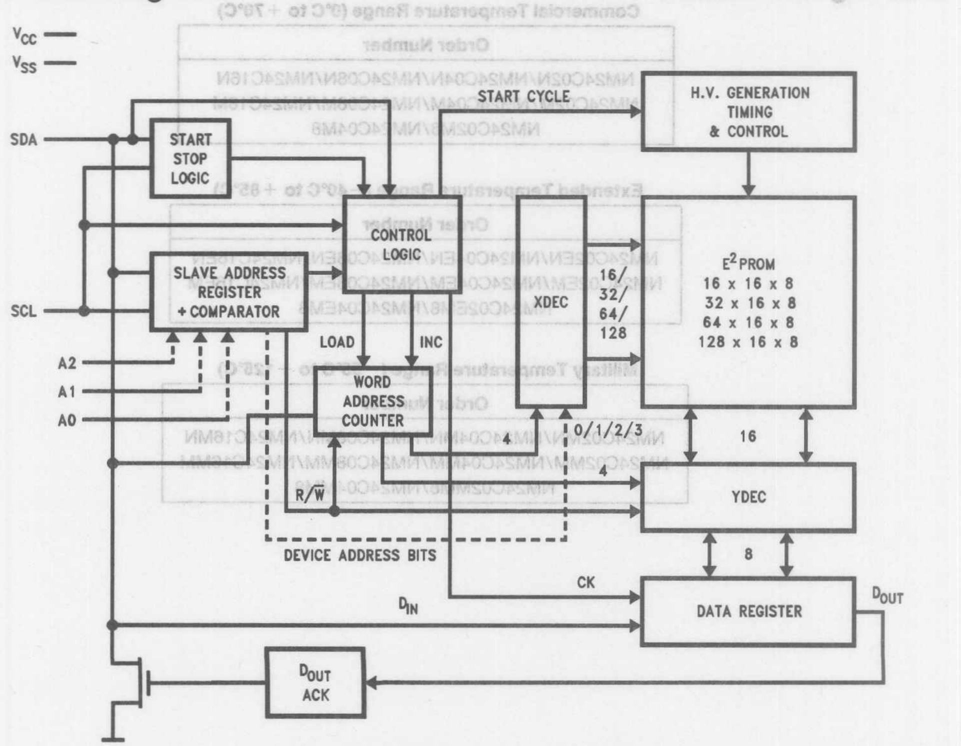
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

National EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Low Power CMOS
  - — 2 mA active current typical
  - — 60 μA standby current typical
- 2-wire I²C serial interface
  - — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP or 14 pin SO package

Functional Diagram



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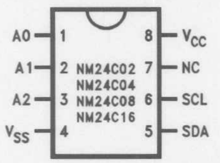
Connection Diagrams

Dual-In-Line Package (N)



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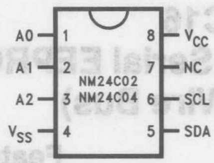
Top View

See NS Package Number N08E (N)

SO Package (M8)



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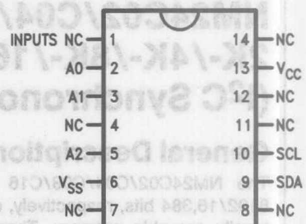
Top View

See NS Package Number M08A (M8)

SO Package (M)



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Top View

See NS Package Number M14B (M)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Connection
V_{CC}	+5V

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C02N/NM24C04N/NM24C08N/NM24C16N NM24C02M/NM24C04M/NM24C08M/NM24C16M NM24C02M8/NM24C04M8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C02EN/NM24C04EN/NM24C08EN/NM24C16EN NM24C02EM/NM24C04EM/NM24C08EM/NM24C16EM NM24C02EM8/NM24C04EM8

Military Temperature Range (−55°C to +125°C)

Order Number
NM24C02MN/NM24C04MN/NM24C08MN/NM24C16MN NM24C02MM/NM24C04MM/NM24C08MM/NM24C16MM NM24C02MM8/NM24C04MM8

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

NM24C02M/C04M/C08M/C16M (Mil. Temperature)	−55°C to +125°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

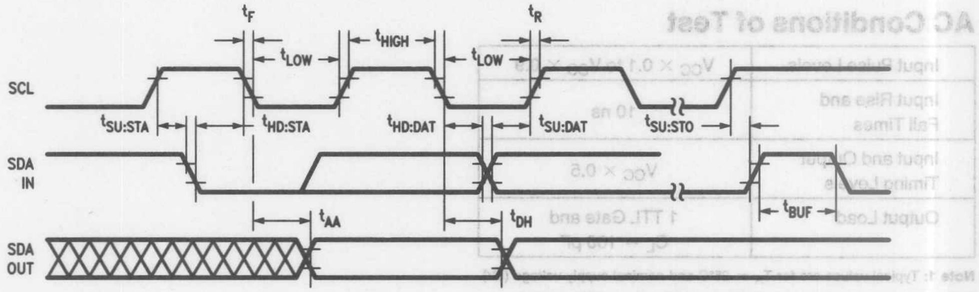
Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

t_{SCL}	SCL Clock Frequency			
t_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data in Hold Time	0		µs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMS on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

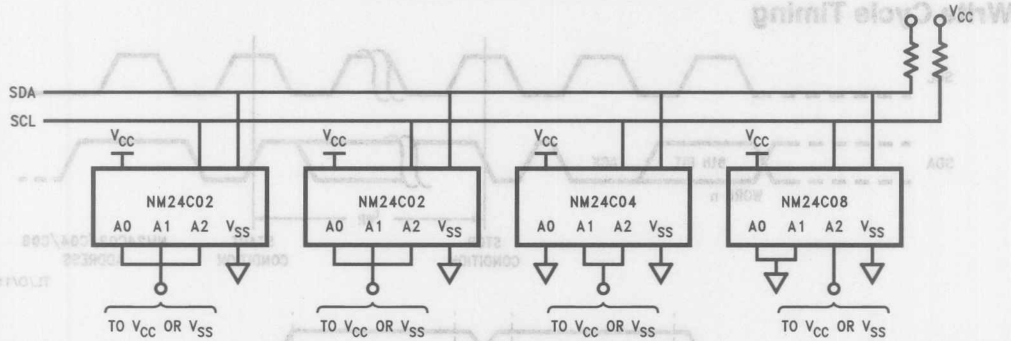
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (Tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any I²C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 16K (Maximum Size) of Memory on 2-Wire Bus



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Note: The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.

Note: The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.

Note: It is recommended that the total line capacitance be less than 400 pF.

Note: Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C02	DA	DA	DA	2048 Bits	1
NM24C04	V_{SS}	DA	DA	4096 Bits	2
NM24C08	V_{SS}	V_{SS}	DA	8192 Bits	4
NM24C16	V_{SS}	V_{SS}	V_{SS}	16,384 Bits	8

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24Cxx device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C02	ADR	ADR	ADR	$2^3 = 8$ (8) x (2K) = 16K
NM24C04	X	ADR	ADR	$2^2 = 4$ (4) x (4K) = 16K
NM24C08	X	X	ADR	$2^1 = 2$ (2) x (8K) = 16K
NM24C16	X	X	X	$2^0 = 1$ (1) x (16K) = 16K

ADR: Denotes an active pin used for device addressing
X: Not used for addressing (Must be tied to Ground/V_{SS})

Device Operation

The NM24Cxx supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24Cxx will be considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

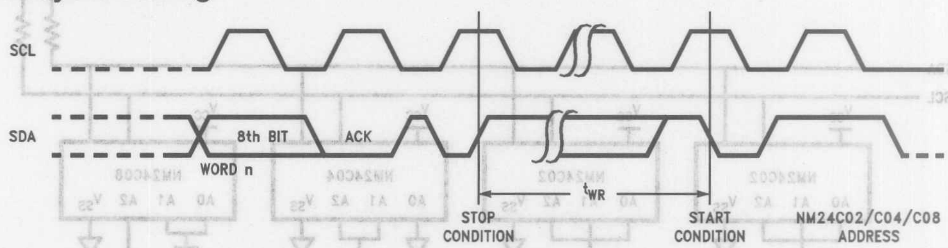
START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24Cxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

Write Cycle Timing



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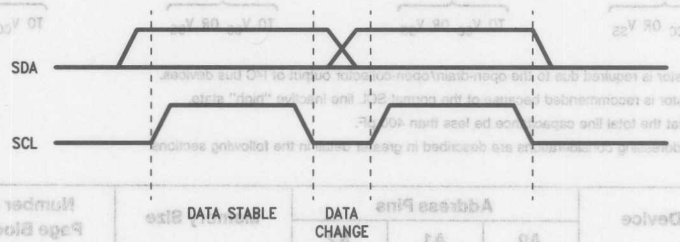

TL/D/11099-6

FIGURE 1. Data Validity

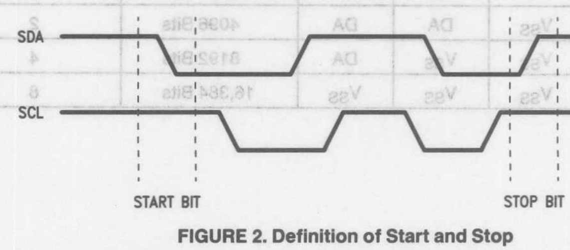

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FIGURE 2. Definition of Start and Stop

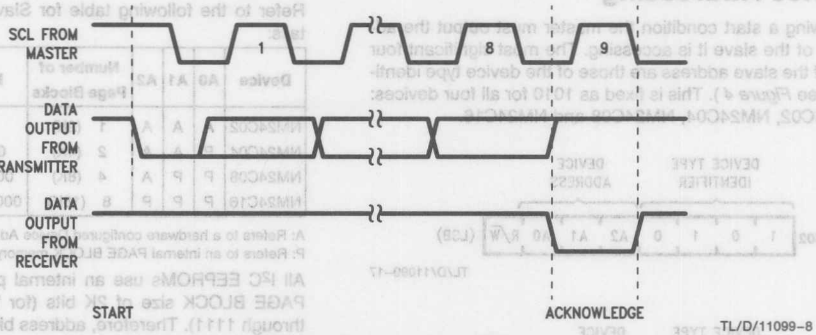


FIGURE 3. Acknowledge Response from Receiver

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24Cxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24Cxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24Cxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

2

bits of the slave address are those of the device type identifier (see *Figure 4*). This is fixed as 1010 for all four devices: NM24C02, NM24C04, NM24C08 and NM24C16.

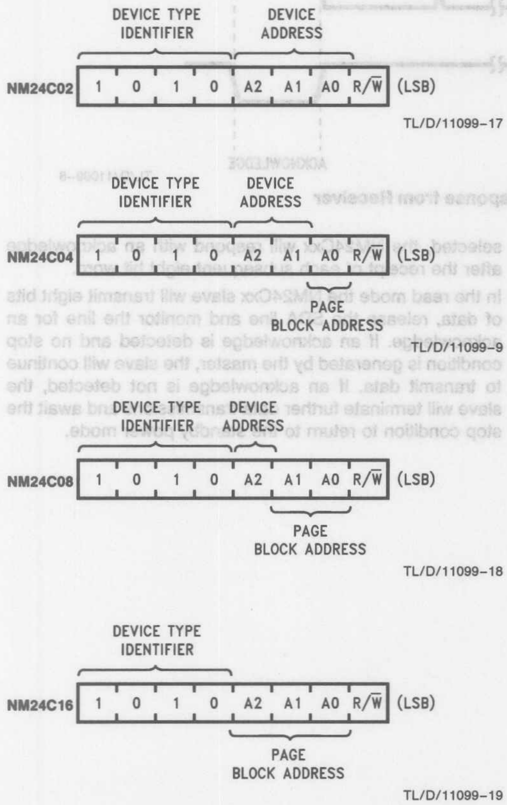


FIGURE 4. Slave Addresses

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C02	A	A	A	1 (2K)	(NONE)
NM24C04	P	A	A	2 (4K)	0 1
NM24C08	P	P	A	4 (8K)	00 01 10 11
NM24C16	P	P	P	8 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin
P: Refers to an internal PAGE BLOCK memory segment

All I^2C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed, and a "0" initiates the write mode.

A simple review: After the NM24C02/C04/C08/C16 recognizes the start condition, the devices interfaced to the I^2C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24Cxx responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

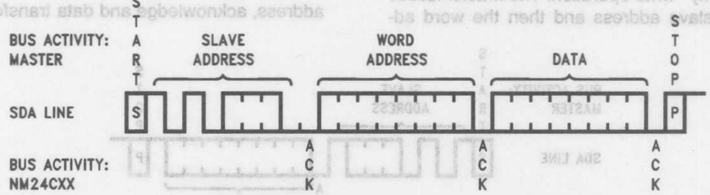
PAGE WRITE

The NM24Cxx is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24Cxx will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation the NM24Cxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24Cxx is still busy with the write operation no ACK will be returned. If the NM24Cxx has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.



TL/D/11099–10

FIGURE 5. Byte Write

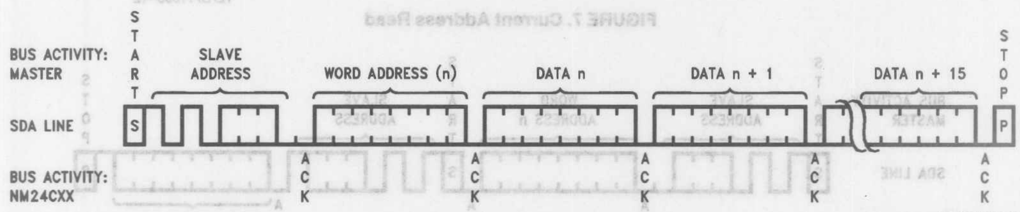


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FIGURE 6. Page Write

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24Cxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24Cxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24Cxx discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24Cxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24Cxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24Cxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24Cxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

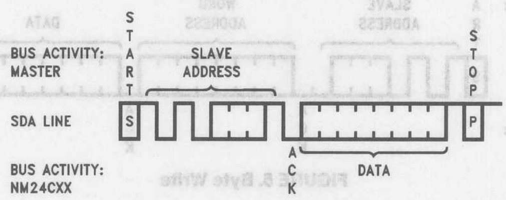

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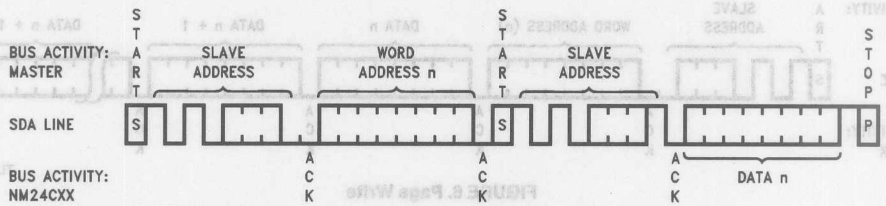
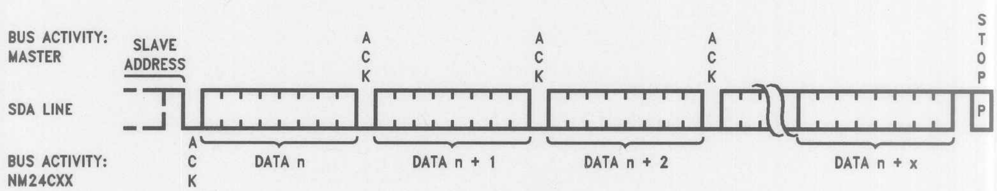
FIGURE 7. Current Address Read



TL/D/11099–13

FIGURE 8. Random Read



TL/D/11099–14

FIGURE 9. Sequential Read

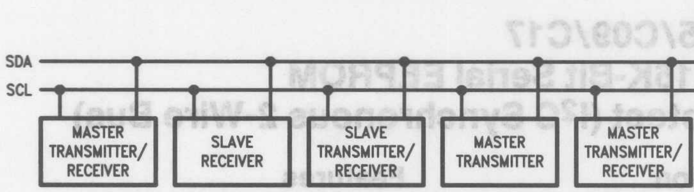


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FIGURE 10. Typical System Configuration

Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7 kΩ)

NM24C03/C05/C09/C17 2K-/4K-/8K-/16K-Bit Serial EEPROM with Write Protect (I^2C Synchronous 2-Wire Bus)

General Description

The NM24C03/C05/C09/C17 devices are 2048/4096/8192/16,834 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I^2C 2-wire protocol, and are designed to minimize device pin count and simplify PC board layout requirements.

The upper half of the memory can be disabled (Write Protected) by connecting the WP pin to V_{CC}. This section of memory then becomes unalterable unless WP is switched to V_{SS}.

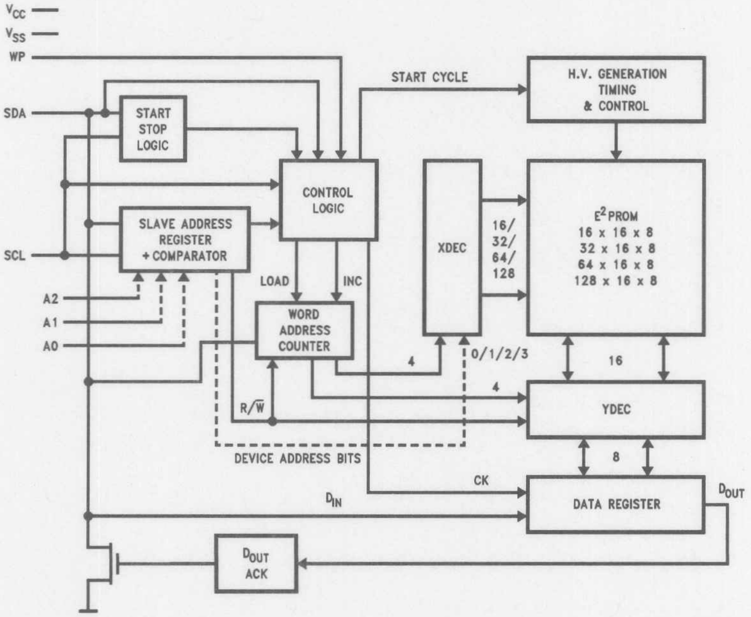
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

National EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption.

Features

- Hardwire write protect for upper block
- Low Power CMOS
  - — 2 mA active current typical
  - — 60 μA standby current typical
- 2-wire I^2C serial interface
  - — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP or 14 pin SO package

Functional Diagram



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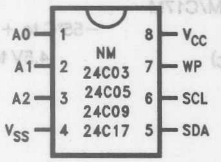
Connection Diagrams

Dual-In-Line Package (N) and (M8)



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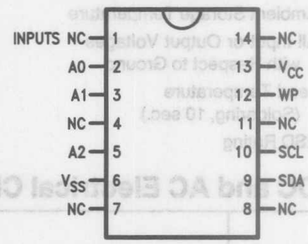
Top View

See NS Package Number N08E (N) or M08A (M8)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
V_{CC}	+5V
WP	Write Protect
NC	No Connection

SO Package (M)



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Top View

See NS Package Number M14B

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C03N/NM24C05N/NM24C09N/NM24C17N
NM24C03M8/NM24C05M8/NM24C09M/NM24C17M

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C03EN/NM24C05EN/NM24C09EN/NM24C17EN
NM24C03EM8/NM24C05EM8/NM24C09EM/NM24C17EM

Military Temperature Range (−55°C to +125°C)

Order Number
NM24C03MN/NM24C05MN/NM24C09MN/NM24C17MN
NM24C03MM8/NM24C05MM8/NM24C09MM/NM24C17MM

Note: For 14-lead SO package availability for the NM24C03/05 devices, check with your NSC sales representative.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM24C03/C05/C09/C17	0°C to +70°C
NM24C03E/C05E/C09E/C17E	−40°C to +85°C
NM24C03M/C05M/C09M/C17M (Mil. Temp.)	−55°C to +125°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits Min	Limits Typ. (Note 1)	Limits Max	Units
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A_0, A_1, A_2, SCL, WP)	V_{IN} = 0V	6	pF

A.C. Conditions of Test

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

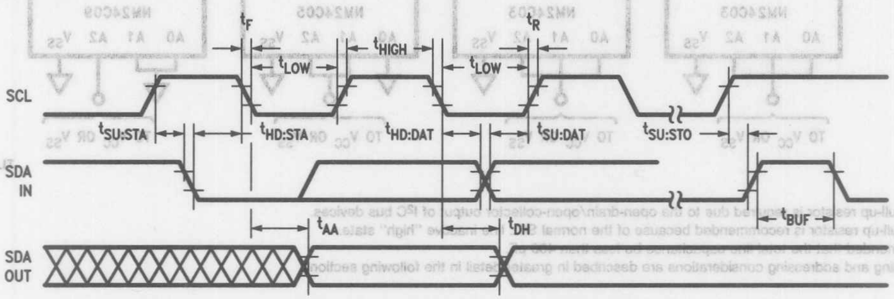
Note 2: This parameter is periodically sampled and not 100% tested.

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data in Hold Time	0		µs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24Cxx bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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BACKGROUND INFORMATION (I^2C Bus)

As mentioned, the I^2C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In additon, since the I^2C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMs on the I^2C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

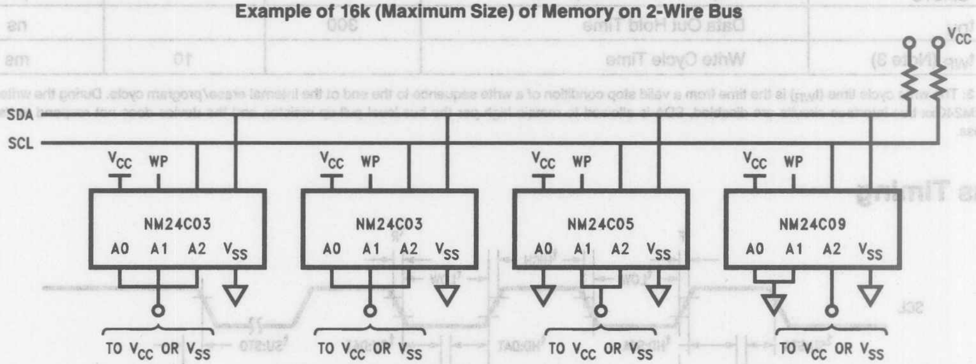
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string)

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits
MASTER	Any I^2C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 16k (Maximum Size) of Memory on 2-Wire Bus



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Note:

The SDA pull-up resistor is required due to the open-drain/open-collector output of I^2C bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.
It is recommended that the total line capacitance be less than 400 pF.
Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C03	DA	DA	DA	2048 Bits	1
NM24C05	V_{SS}	DA	DA	4096 Bits	2
NM24C09	V_{SS}	V_{SS}	DA	8192 Bits	4
NM24C17	V_{SS}	V_{SS}	V_{SS}	16,384 Bits	8

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24Cxx device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C03	ADR	ADR	ADR	$2^3 = 8$ (8) × (2K) = 16K
NM24C05	X	ADR	ADR	$2^2 = 4$ (4) × (4K) = 16K
NM24C09	X	X	ADR	$2^1 = 2$ (2) × (8K) = 16K
NM24C17	X	X	X	$2^0 = 1$ (1) × (16K) = 16K

ADR: Denotes an active pin used for device addressing

X: Not used for addressing (must be tied to Ground/V_{SS})

WP WRITE PROTECTION

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible.

If tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C03/C05/C09/C17 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24Cxx is considered a slave in all applications.

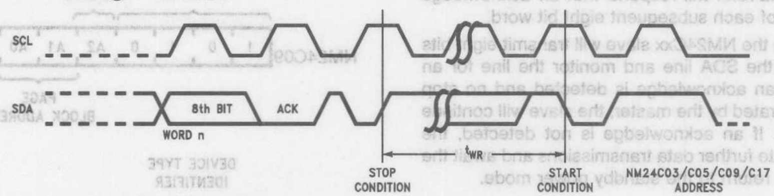
CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

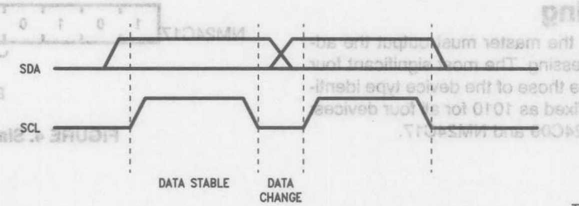
START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24Cxx continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Write Cycle Timing

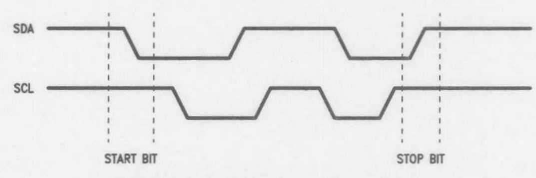


TL/D/11100-5



TL/D/11100-6

FIGURE 1. Data Validity



TL/D/11100-7

FIGURE 2. Definition of Start and Stop

2

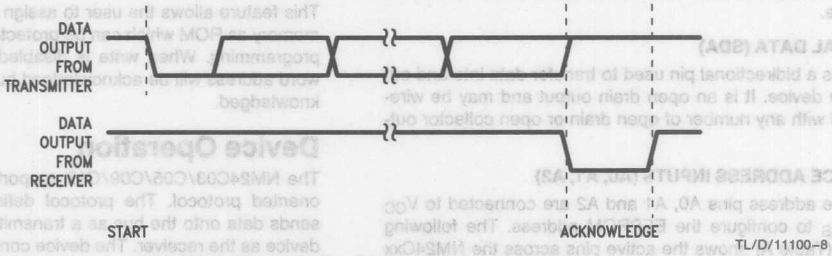


FIGURE 3. Acknowledge Response from Receiver

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24Cxx to place the device in the standby power mode.

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24Cxx device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24Cxx will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24Cxx slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier, (see *Figure 4*). This is fixed as 1010 for all four devices: NM24C03, NM24C05, NM24C09 and NM24C17.

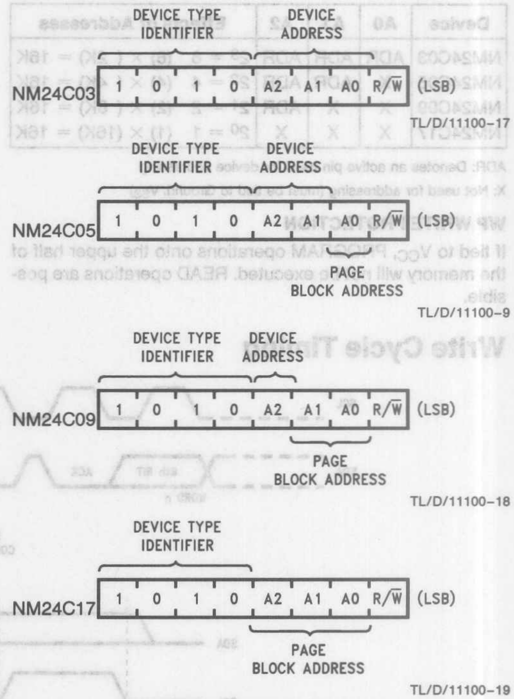


FIGURE 4. Slave Addresses

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C03	A	A	A	1 (2K)	(None)
NM24C05	P	A	A	2 (4K)	0 1
NM24C09	P	P	A	4 (8K)	00 01 10 11
NM24C17	P	P	P	1 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin
P: Refers to an internal PAGE BLOCK memory segment

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

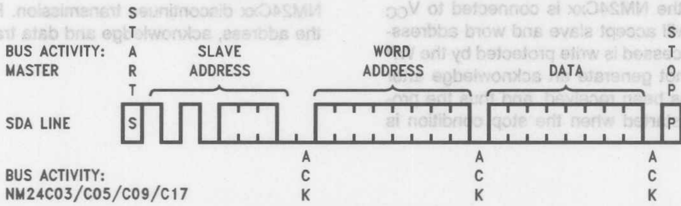
The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed and a "0" initiates the write mode.

A simple review: After the NM24C03/C05/C09/C17 recognizes the start condition, the devices interfaced to the I²C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24Cxx responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.



TL/D/11100-10

FIGURE 5. Byte Write

2

Write Operations (Continued)

PAGE WRITE

The NM24Cxx is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24Cxx will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation, the NM24Cxx initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24Cxx is still busy with the write operation, no ACK will be returned. If the NM24Cxx has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the NM24Cxx is connected to V_{CC} (+5V). The NM24Cxx will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24Cxx will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Read Operations

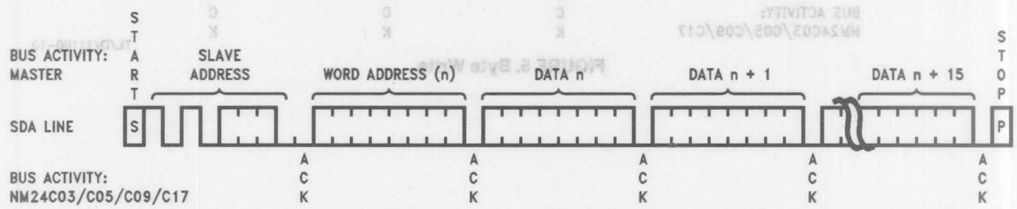
Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24Cxx contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24Cxx issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24Cxx discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24Cxx and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24Cxx discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.



TL/D/11100-11

FIGURE 6. Page Write

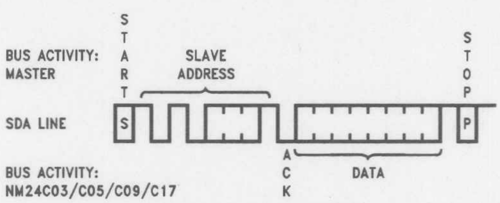


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FIGURE 7. Current Address Read

Read Operations (Continued)

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24Cxx continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24Cxx continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

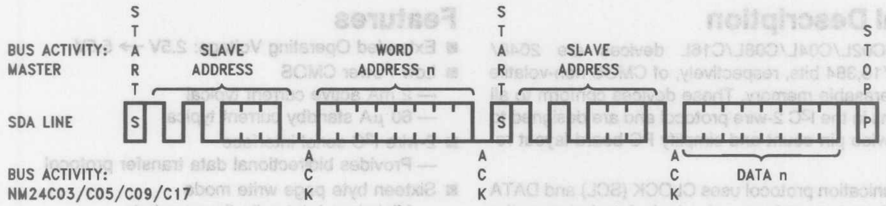

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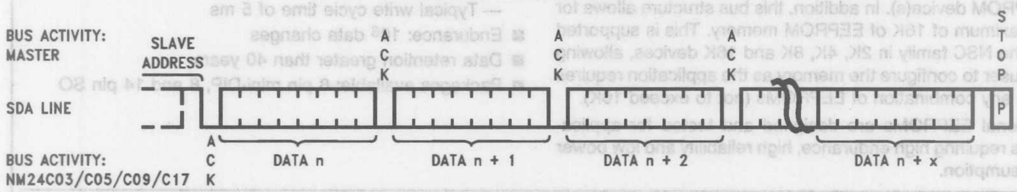
FIGURE 8. Random Read



TL/D/11100–14

FIGURE 9. Sequential Read

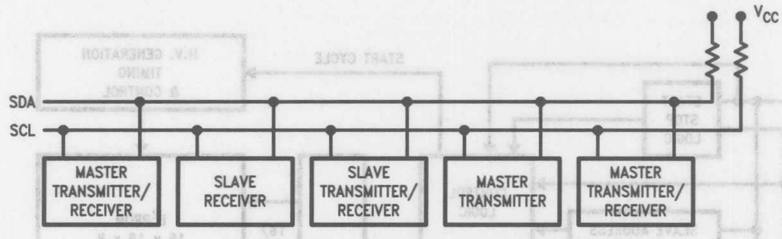


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FIGURE 10. Typical System Configuration

National Semiconductor

NM24C02L/C04L/C08L/C16L 2K-/4K-/8K-/16K-Bit Serial EEPROM (I^2C Synchronous 2-Wire Bus)

General Description

The NM24C02L/C04L/C08L/C16L devices are 2048/4096/8192/16,384 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I^2C 2-wire protocol and are designed to minimize device pin count and simplify PC board layout requirements.

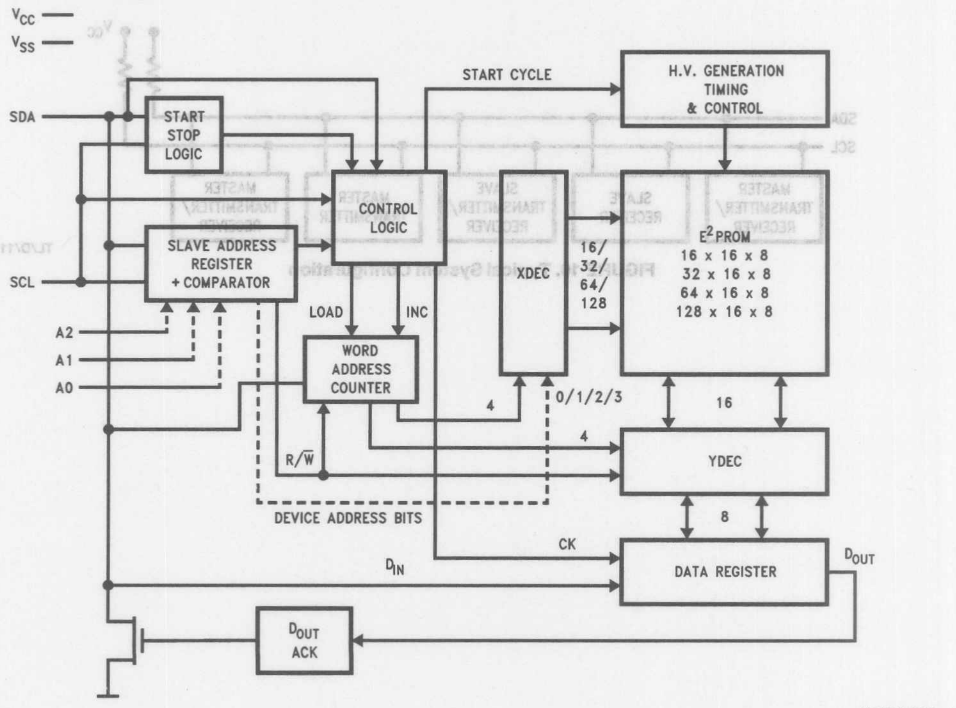
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

National EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

Features

- Extended Operating Voltage: 2.5V → 5.5V
- Low Power CMOS
  - — 2 mA active current typical
  - — 60 μA standby current typical
- 2-wire I^2C serial interface
  - — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP, 8 and 14 pin SO

Functional Diagram



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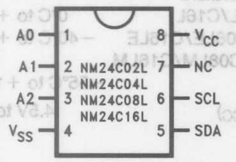
Connection Diagrams

Dual-In-Line Package (N)



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Top View

See NS Package Number N08E (N)

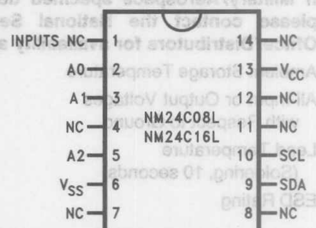
SO Package (M8)

TL/D/11738-3

Top View

See NS Package Number M08A (M8)

SO Package (M)



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Top View

See NS Package Number M14B (M)

Pin Names

A0, A1, A2	Device Address Inputs
V_{SS}	Ground
SDA	Data I/O
SCL	Clock Input
NC	No Connection (Float, GND, or V_{CC})
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C02LN/NM24C04LN/NM24C08LN/NM24C16LN NM24C02LM8/NM24C04LM8/NM24C08LM/NM24C16LM

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C02LEN/NM24C04LEN/NM24C08LEN/NM24C16LEN NM24C02LEM8/NM24C04LEM8/NM24C08LEM/NM24C16LEM

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	$-65°C$ to $+150°C$
All Input or Output Voltages with Respect to Ground	$+6.5V$ to $-0.3V$
Lead Temperature (Soldering, 10 seconds)	$+300°C$
ESD Rating	2000V min

NM24C02L/C04L/C08L/C16L	$0°C$ to $+70°C$
NM24C02LE/C04LE/C08LE/C16LE	$-40°C$ to $+85°C$
NM24C02LM/C04LM/C08LM/C16LM (Mil. Temperature)	$-55°C$ to $+125°C$
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ unless otherwise specified

Symbol	Parameter	Test Conditions	Limits Min	Limits Typ (Note 1)	Limits Max	Units
I_{CCA}	Active Power Supply Current	$f_{SCL} = 100$ kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		-0.3		$V_{CC} \times 0.3$	V
V_{IH}	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 3$ mA			0.4	V

Capacitance $T_A = 25°C$, $f = 1.0$ MHz, $V_{CC} = 5V$

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O} = 0V$	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL)	$V_{IN} = 0V$	6	pF

AC Conditions of Test

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and $C_L = 100$ pF

Note 1: Typical values are for $T_A = 25°C$ and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

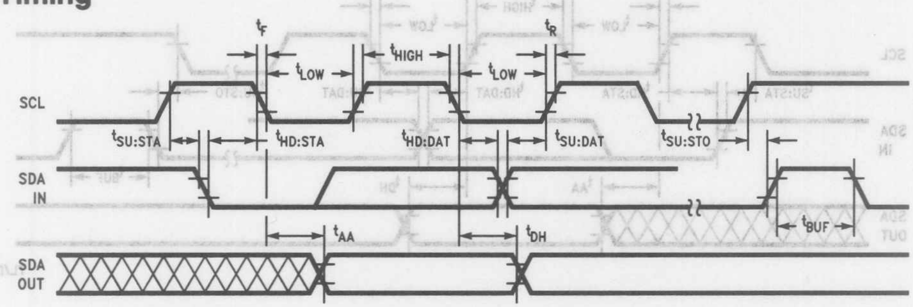
LOW VOLTAGE (2.5V $\leq V_{CC} \leq$ 4.5V) SPECIFICATIONS

Read and Write Cycle Limits

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.5		μs
t_{LOW}	Clock Low Period	6.7		μs
t_{HIGH}	Clock High Period	4.5		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	500		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24CxxL bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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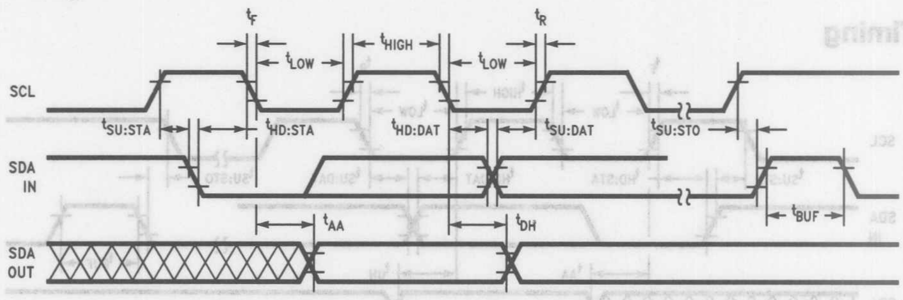
Read and Write Cycle Limits (4.5V ≤ V_{CC} ≤ 5.5V)

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data in Hold Time	0		μs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the NM24CxxL bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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As mentioned, the I²C bus allows synchronous bidirectional communication between transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In addition, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMS on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

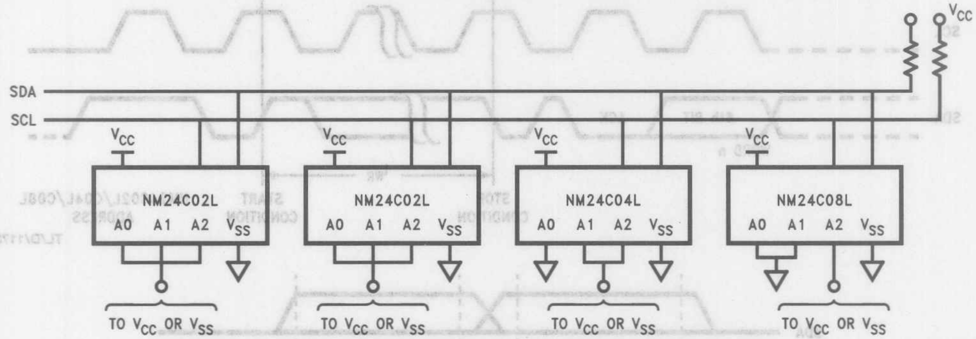
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (Tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE ADDRESS]—[PAGE BLOCK ADDRESS]—[BYTE ADDRESS]

WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits.
MASTER	Any I²C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 16K (Maximum Size) of Memory on 2-Wire Bus



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Note: The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.

Note: The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.

Note: It is recommended that the total line capacitance be less than 400 pF.

Note: Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C02L	DA	DA	DA	2048 Bits	1
NM24C04L	V_{SS}	DA	DA	4096 Bits	2
NM24C08L	V_{SS}	V_{SS}	DA	8192 Bits	4
NM24C16L	V_{SS}	V_{SS}	V_{SS}	16,384 Bits	8

DA: Device Address

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24CxxL device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses	
NM24C02L	ADR	ADR	ADR	$2^3 = 8$	(8) x (2K) = 16K
NM24C04L	X	ADR	ADR	$2^2 = 4$	(4) x (4K) = 16K
NM24C08L	X	X	ADR	$2^1 = 2$	(2) x (8K) = 16K
NM24C16L	X	X	X	$2^0 = 1$	(1) x (16K) = 16K

ADR: Denotes an active pin used for device addressing
X: Not used for addressing (Must be tied to Ground/V_{SS})

the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24CxxL will be considered a slave in all applications.

CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

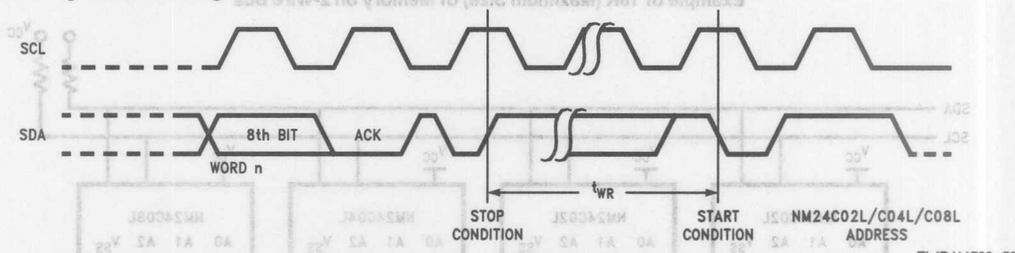
START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24CxxL continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24CxxL to place the device in the standby power mode.

Write Cycle Timing



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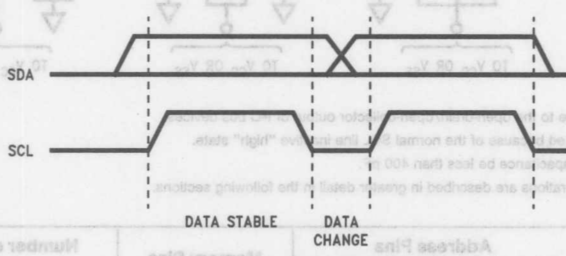

TL/D/11738-9

FIGURE 1. Data Validity

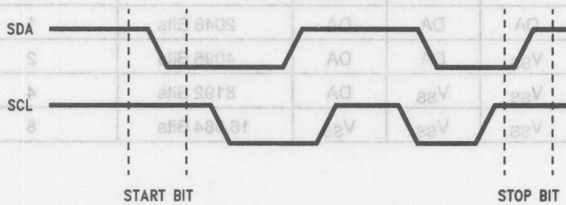

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FIGURE 2. Definition of Start and Stop

Device Operation (Continued)

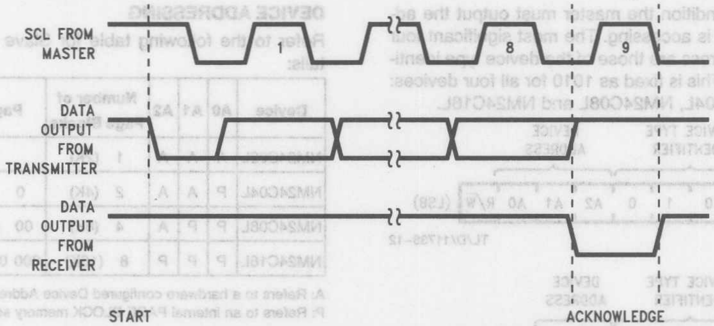

FIGURE 3. Acknowledge Response from Receiver

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24CxxL device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24CxxL will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24CxxL slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier (see *Figure 4*). This is fixed as 1010 for all four devices: NM24C02L, NM24C04L, NM24C08L and NM24C16L.

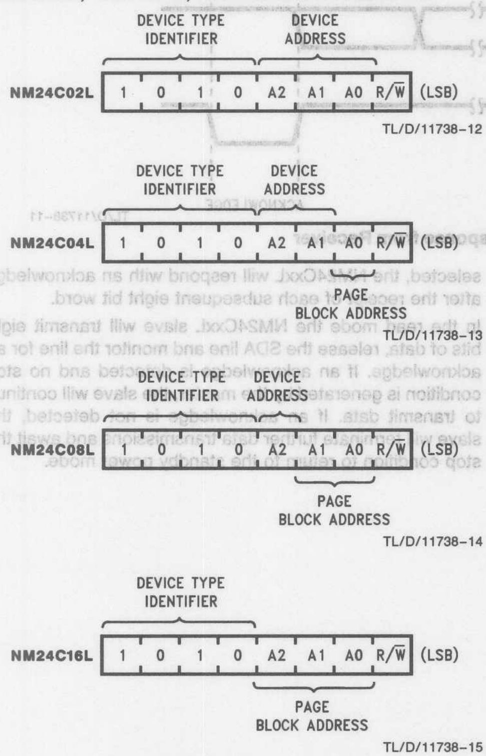

FIGURE 4. Slave Addresses

DEVICE ADDRESSING

Refer to the following table for Slave Addresss string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C02L	A	A	A	1 (2K)	(NONE)
NM24C04L	P	A	A	2 (4K)	0 1
NM24C08L	P	P	A	4 (8K)	00 01 10 11
NM24C16L	P	P	P	8 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin
P: Refers to an internal PAGE BLOCK memory segment

All I²C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed, and a "0" initiates the write mode.

A simple review: After the NM24C02L/C04L/C08L/C16L recognizes the start condition, the devices interfaced to the I²C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24CxxL responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24CxxL begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24CxxL inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

PAGE WRITE

The NM24CxxL is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24CxxL will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation the NM24CxxL initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24CxxL is still busy with the write operation no ACK will be returned. If the NM24CxxL has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

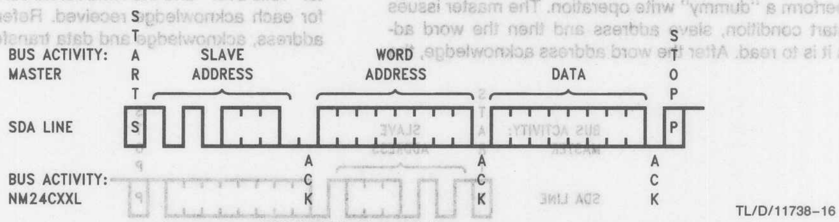

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FIGURE 5. Byte Write

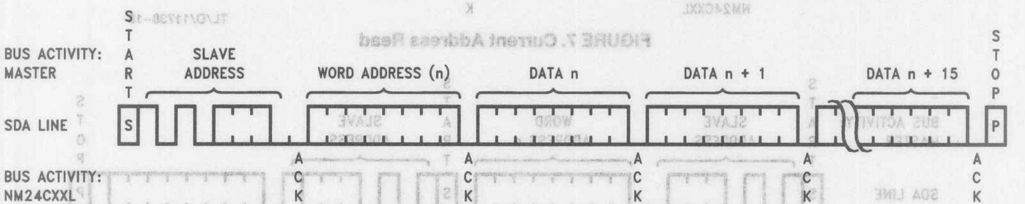

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FIGURE 6. Page Write

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24CxxL contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24CxxL issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24CxxL discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24CxxL and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24CxxL discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24CxxL continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24CxxL continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

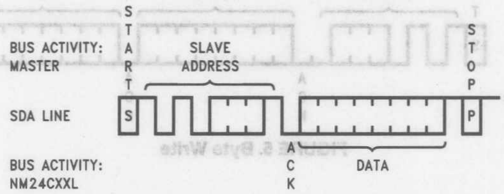


FIGURE 7. Current Address Read

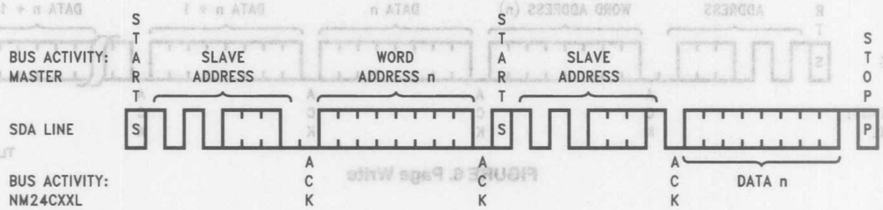


FIGURE 8. Random Read

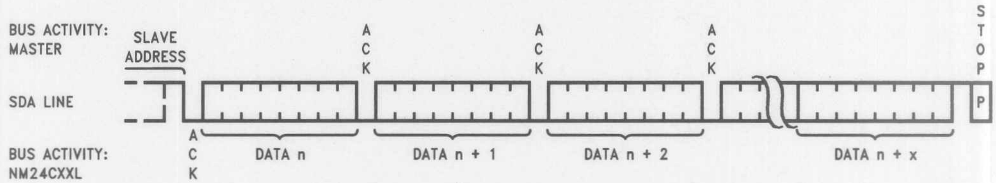


FIGURE 9. Sequential Read

2

Read Operations (Continued)

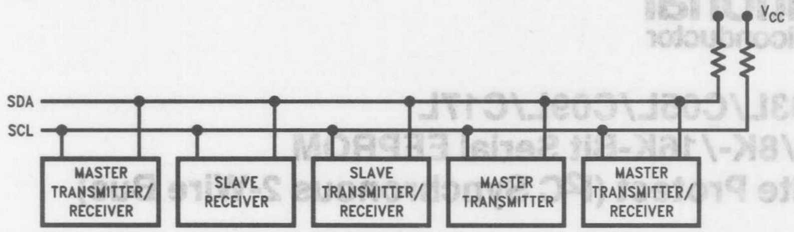


FIGURE 10. Typical System Configuration

Note: Due to open drain configuration of SDA, a bus-level pull-up resistor is called for, (typical value = 4.7 kΩ)

NM24C03L/C05L/C09L/C17L 2K-/4K-/8K-/16K-Bit Serial EEPROM with Write Protect (I²C Synchronous 2-Wire Bus)

General Description

The NM24C03L/C05L/C09L/C17L devices are 2048/4096/8192/16,834 bits, respectively, of CMOS non-volatile electrically erasable memory. These devices conform to all specifications in the I²C 2-wire protocol, and are designed to minimize device pin count and simplify PC board layout requirements.

The upper half of the memory can be disabled (Write Protected) by connecting the WP pin to V_{CC}. This section of memory then becomes ROM.

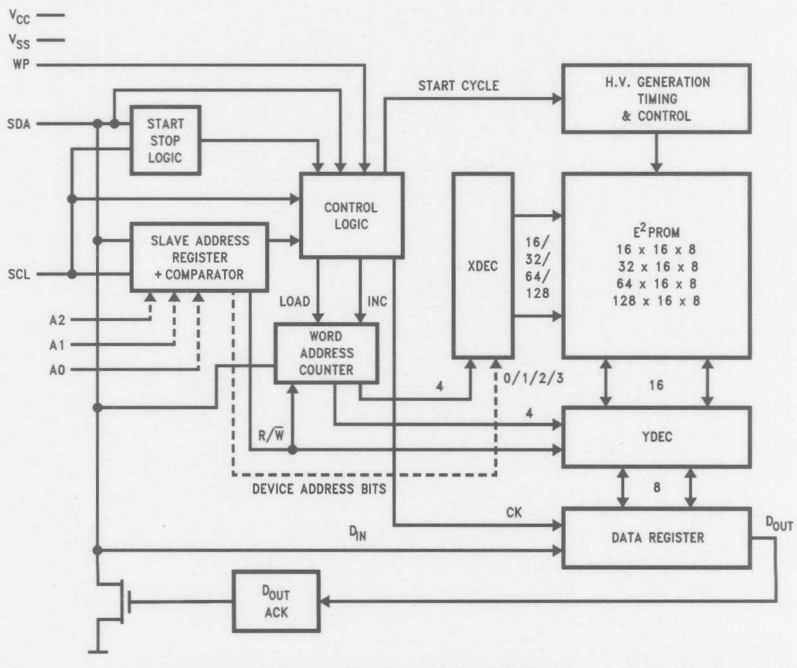
This communication protocol uses CLOCK (SCL) and DATA I/O (SDA) lines to synchronously clock data between the master (for example a microprocessor) and the slave EEPROM device(s). In addition, this bus structure allows for a maximum of 16K of EEPROM memory. This is supported by the NSC family in 2K, 4K, 8K and 16K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).

National EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption.

Features

- Extended Operating Voltage: 2.5V–5.5V
- Hardwire write protect for upper block
- Low Power CMOS
  - — 2 mA active current typical
  - — 60 μA standby current typical
- 2-wire I²C serial interface
  - — Provides bidirectional data transfer protocol
- Sixteen byte page write mode
  - — Minimizes total write time per byte
- Self timed write cycle
  - — Typical write cycle time of 5 ms
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8 pin mini-DIP, 8 and 14 pin SO

Functional Diagram



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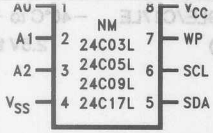
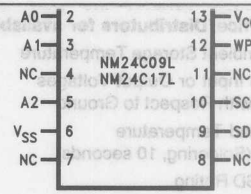


TL/D/11739-2

Top View

See NS Package Number N08E (N) and M08A (M8)

VSS	Ground
SDA	Data I/O
SCL	Clock Input
V_{CC}	Power Supply
WP	Write Protect
NC	No Connection



TL/D/11739-3

Top View

See NS Package Number M14B

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM24C03LN/NM24C05LN/NM24C09LN/NM24C17LN NM24C09LM/NM24C17LM NM24C03LM8/NM24C05LM8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM24C03LEN/NM24C05LEN/NM24C09LEN/NM24C17LEN NM24C09LEM/NM24C17LEM NM24C03LEM8/NM24C05LEM8

LOW VOLTAGE (2.5V ≤ V_{CC} < 5.5V) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 seconds)	+300°C
ESD Rating	2000V min

Operating Conditions

Ambient Operating Temperature	
NM24C03L/C05L/C09L/C17L	0°C to +70°C
NM24C03LE/C05LE/C09LE/C17LE	−40°C to +85°C
Positive Power Supply (V_{CC})	2.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.5V to 4.5V (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits Min	Limits Typ (Note 1)	Limits Max	Units
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		V_{CC} × 0.3	V
V_{IH}	Input High Voltage		V_{CC} × 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A0, A1, A2, SCL, WP)	V_{IN} = 0V	6	pF

AC Conditions of Test

Input Pulse Levels	V_{CC} × 0.1 to V_{CC} × 0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} × 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

Note 2: This parameter is periodically sampled and not 100% tested.

STANDARD VOLTAGE (4.5V ≤ V_{CC} ≤ 5.5V) SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM24C03L/C05L/C09L/C17L	0°C to +70°C
NM24C03LE/C05LE/C09LE/C17LE	−40°C to +85°C
NM24C03LM/C05LM/C09LM/C17LM (Mil. Temp.)	−55°C to +125°C
Positive Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ. (Note 1)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz		2.0	3.0	mA
I_{SB}	Standby Current	V_{IN} = GND or V_{CC}		60	100	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	10	μA
V_{IL}	Input Low Voltage		−0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Capacitance T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max	Units
$C_{I/O}$ (Note 2)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN} (Note 2)	Input Capacitance (A_0, A_1, A_2, SCL, WP)	V_{IN} = 0V	6	pF

A.C. Conditions of Test

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} x 0.5
Output Load	1 TTL Gate and C_L = 100 pF

Note 1: Typical values are for T_A = 25°C and nominal supply voltage (5V).

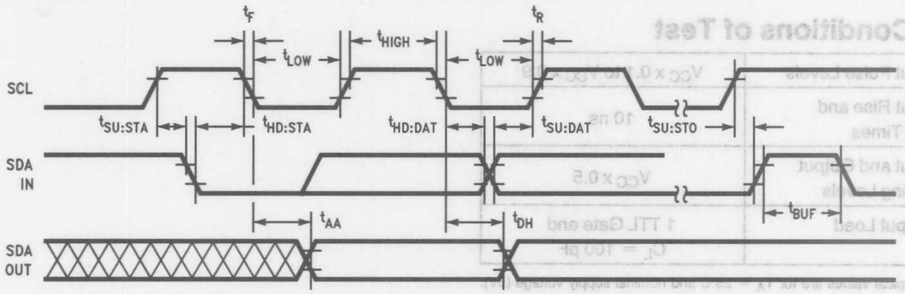
Note 2: This parameter is periodically sampled and not 100% tested.

2

t_{SCL}	SCL Clock Frequency		80	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	7.0	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	6.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.5		µs
t_{LOW}	Clock Low Period	6.7		µs
t_{HIGH}	Clock High Period	4.5		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	6.7		µs
$t_{HD:DAT}$	Data in Hold Time	0		µs
$t_{SU:DAT}$	Data in Setup Time	500		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	6.7		µs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		15	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24CxxL bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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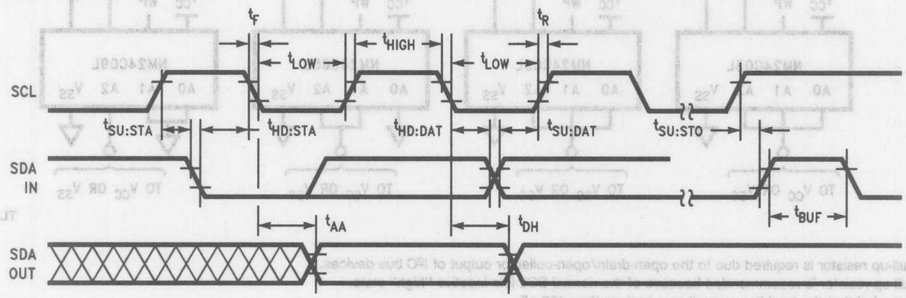
Read and Write Cycle Limits (4.5V ≤ V_{CC} ≤ 5.5V)

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency		100	kHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data in Hold Time	0		µs
$t_{SU:DAT}$	Data in Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns
t_{WR} (Note 3)	Write Cycle Time		10	ms

Note 3: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end ot the internal erase/program cycle. During the write cycle, the NM24CxxL bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Bus Timing



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2

Bus Timing (Continued)

BACKGROUND INFORMATION (I²C Bus)

As mentioned, the I²C bus allows synchronous bidirectional communication between Transmitter/Receiver using the SCL (clock) and SDA (Data I/O) lines. All communication must be started with a valid START condition, concluded with a STOP condition and acknowledged by the Receiver with an ACKNOWLEDGE condition.

In additon, since the I²C bus is designed to support other devices such as RAM, EPROM, etc., the device type identifier string must follow the START condition. For EEPROMs, this 4-bit string is 1010.

As shown below, the EEPROMs on the I²C bus may be configured in any manner required, providing the total memory addressed does not exceed 16K (16,834 bits). EEPROM memory addressing is controlled by two methods:

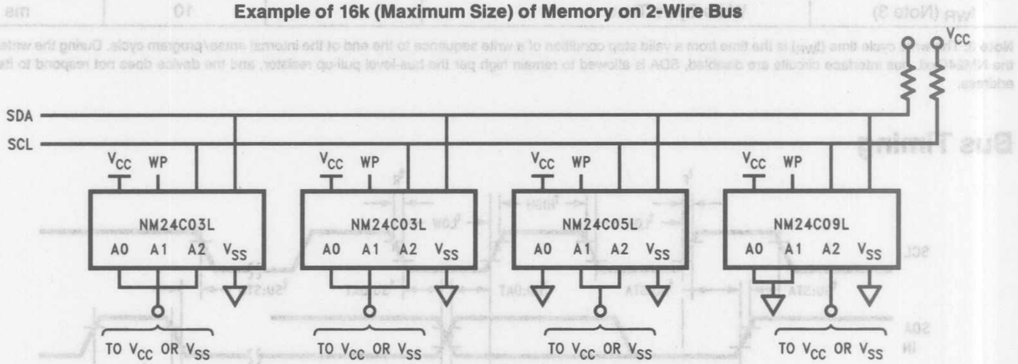
- Hardware configuring the A0, A1 and A2 pins (Device Address pins) with pull-up or pull-down resistors. ALL UNUSED PINS MUST BE GROUNDED (tied to V_{SS}).
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the Slave Address string)

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]-[DEVICE ADDRESS]-[PAGE BLOCK ADDRESS]-[BYTE ADDRESS]

DEFINITIONS	
WORD	8 bits (byte) of data.
PAGE	16 sequential addresses (one byte each) that may be programmed during a "Page Write" programming cycle.
PAGE BLOCK	2,048 (2K) bits organized into 16 pages of addressable memory. (8 bits) x (16 bytes) x (16 pages) = 2,048 bits.
MASTER	Any I²C device CONTROLLING the transfer of data (such as a microprocessor).
SLAVE	Device being controlled (EEPROMs are always considered Slaves).
TRANSMITTER	Device currently SENDING data on the bus (may be either a Master OR Slave).
RECEIVER	Device currently receiving data on the bus (Master or Slave).

Example of 16k (Maximum Size) of Memory on 2-Wire Bus



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Note:

The SDA pull-up resistor is required due to the open-drain/open-collector output of I²C bus devices.
The SCL pull-up resistor is recommended because of the normal SCL line inactive "high" state.
It is recommended that the total line capacitance be less than 400 pF.
Specific timing and addressing considerations are described in greater detail in the following sections.

Device	Address Pins			Memory Size	Number of Page Blocks
	A0	A1	A2		
NM24C03L	DA	DA	DA	2048 Bits	1
NM24C05L	V_{SS}	DA	DA	4096 Bits	2
NM24C09L	V_{SS}	V_{SS}	DA	8192 Bits	4
NM24C17L	V_{SS}	V_{SS}	V_{SS}	16,384 Bits	8

DA: Device Address

Pin Descriptions

SERIAL CLOCK (SCL)

The SCL input is used to clock all data into and out of the device.

SERIAL DATA (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

DEVICE ADDRESS INPUTS (A0, A1, A2)

Device address pins A0, A1 and A2 are connected to V_{CC} or V_{SS} to configure the EEPROM address. The following table (Table A) shows the active pins across the NM24CxxL device family.

TABLE A

Device	A0	A1	A2	Effects of Addresses
NM24C03L	ADR	ADR	ADR	$2^3 = 8$ (8) × (2K) = 16K
NM24C05L	X	ADR	ADR	$2^2 = 4$ (4) × (4K) = 16K
NM24C09L	X	X	ADR	$2^1 = 2$ (2) × (8K) = 16K
NM24C17L	X	X	X	$2^0 = 1$ (1) × (16K) = 16K

ADR: Denotes an active pin used for device addressing

X: Not used for addressing (must be tied to Ground/V_{SS})

WP WRITE PROTECTION

If tied to V_{CC}, PROGRAM operations onto the upper half of the memory will not be executed. READ operations are possible.

If tied to V_{SS}, normal memory operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the upper half of the memory as ROM which can be protected against accidental programming. When write is disabled, slave address and word address will be acknowledged but data will not be acknowledged.

Device Operation

The NM24C03L/C05L/C09L/C17L supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the NM24CxxL is considered a slave in all applications.

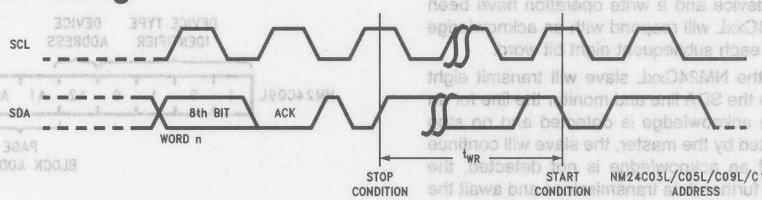
CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to *Figures 1* and *2*.

START CONDITION

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The NM24CxxL continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Write Cycle Timing



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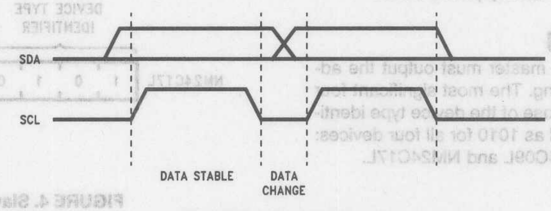

TL/D/11739-8

FIGURE 1. Data Validity

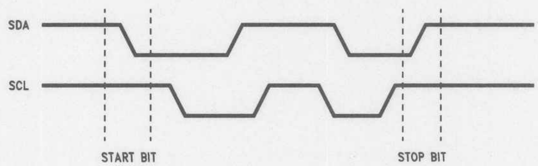

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FIGURE 2. Definition of Start and Stop

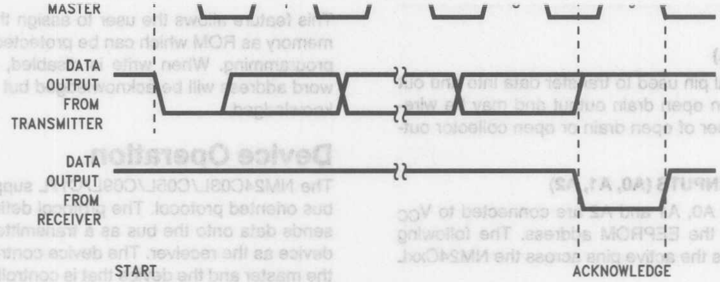

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FIGURE 3. Acknowledge Response from Receiver

STOP CONDITION

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the NM24CxxL to place the device in the standby power mode.

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to *Figure 3*.

The NM24CxxL device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the NM24CxxL will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the NM24CxxL slave will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are those of the device type identifier, (see *Figure 4*). This is fixed as 1010 for all four devices: NM24C03L, NM24C05L, NM24C09L and NM24C17L.

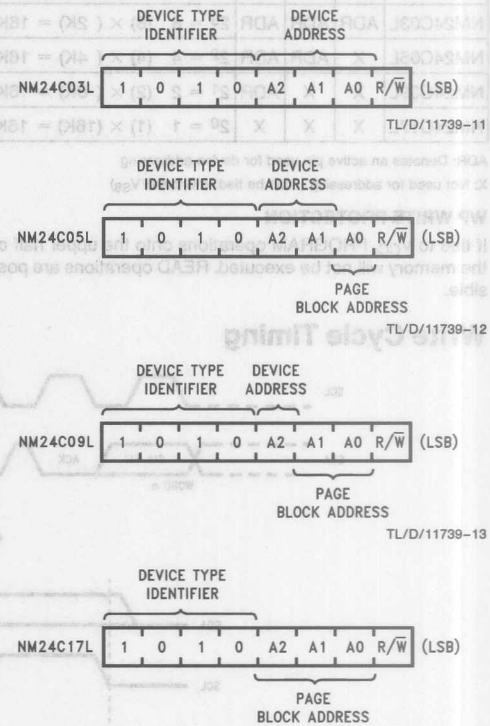

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FIGURE 4. Slave Addresses

Device Addressing (Continued)

Refer to the following table for Slave Address string details:

Device	A0	A1	A2	Number of Page Blocks	Page Block Addresses
NM24C03L	A	A	A	1 (2K)	(None)
NM24C05L	P	A	A	2 (4K)	0 1
NM24C09L	P	P	A	4 (8K)	00 01 10 11
NM24C17L	P	P	P	1 (16K)	000 001 010 011 ... 111

A: Refers to a hardware configured Device Address pin

P: Refers to an internal PAGE BLOCK memory segment

All I^{2}C EEPROMs use an internal protocol that defines a PAGE BLOCK size of 2K bits (for Word addresses 0000 through 1111). Therefore, address bits A0, A1 or A2 (if designated "P") are used to access a PAGE BLOCK in conjunction with the Word address used to access any individual data byte (Word).

The last bit of the slave address defines whether a write or read condition is requested by the master. A "1" indicates that a read operation is to be executed and a "0" initiates the write mode.

A simple review: After the NM24C03L/C05L/C09L/C17L recognizes the start condition, the devices interfaced to the I^{2}C bus wait for a slave address to be transmitted over the SDA line. If the transmitted slave address matches an address of one of the devices, the designated slave pulls the line LOW with an acknowledge signal and awaits further transmissions.

Write Operations

BYTE WRITE

For a write operation a second address field is required which is a word address that is comprised of eight bits and provides access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the NM24CxxL responds with an acknowledge and waits for the next eight bits of data, again, responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the NM24CxxL begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24CxxL inputs are disabled, and the device will not respond to any requests from the master. Refer to *Figure 5* for the address, acknowledge and data transfer sequence.

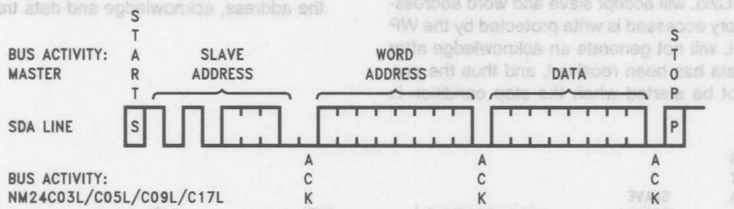

FIGURE 5. Byte Write

Write Operations (Continued)

PAGE WRITE

The NM24CxxL is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data word is tranferred, the master can transmit up to fifteen more words. After the receipt of each word, the NM24CxxL will respond with an acknowledge.

After the receipt of each word, the internal address counter increments to the next address and the next SDA data is accepted. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to *Figure 6* for the address, acknowledge and data transfer sequence.

ACKNOWLEDGE POLLING

Once the stop condition is issued to indicate the end of the host's write operation, the NM24CxxL initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the NM24CxxL is still busy with the write operation, no ACK will be returned. If the NM24CxxL has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

Programming of the upper half of the memory will not take place if the WP pin of the NM24CxxL is connected to V_{CC} (+5V). The NM24CxxL will accept slave and word addresses; but if the memory accessed is write protected by the WP pin, the NM24CxxL will not generate an acknowledge after the first byte of data has been received, and thus the program cycle will not be started when the stop condition is asserted.

Read Operations

Read operations are initiated in the same manner as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

CURRENT ADDRESS READ

Internally the NM24CxxL contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the NM24CxxL issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition, and therefore the NM24CxxL discontinues tranmission. Refer to *Figure 7* for the sequence of address, acknowledge and data transfer.

RANDOM READ

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues a start condition, slave address and then the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the NM24CxxL and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition, and therefore the NM24CxxL discontinues transmission. Refer to *Figure 8* for the address, acknowledge and data transfer sequence.

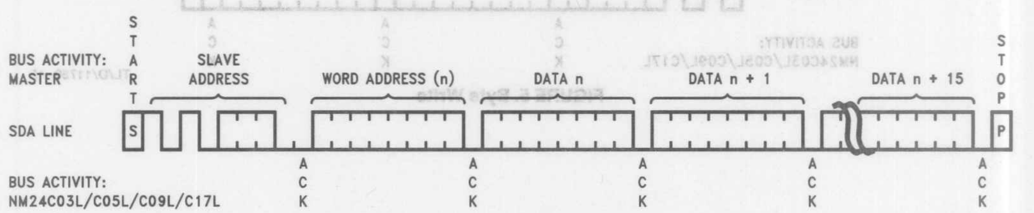

FIGURE 6. Page Write

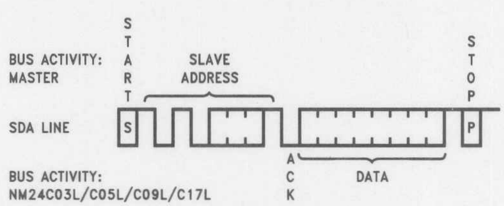

FIGURE 7. Current Address Read

Read Operations (Continued)

SEQUENTIAL READ

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted in the same manner as the other read modes; however, the master now responds with an acknowledge, indicating it requires additional data. The NM24CxxL continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge or by generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n + 1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" and the NM24CxxL continues to output data for each acknowledge received. Refer to *Figure 9* for the address, acknowledge and data transfer sequence.

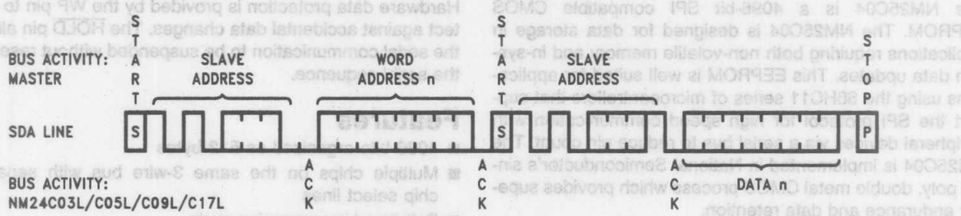

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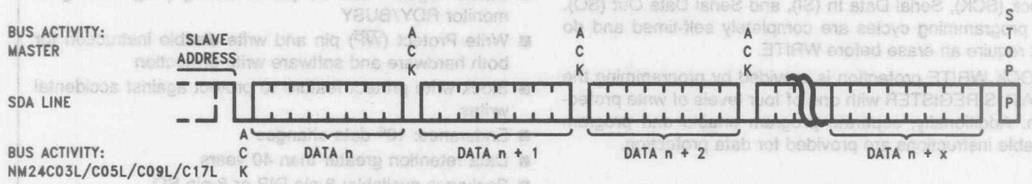
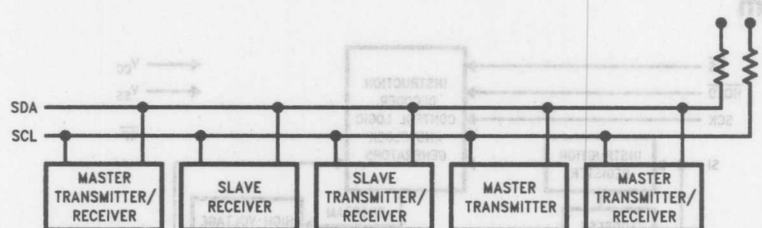
FIGURE 8. Random Read



TL/D/11739–19

FIGURE 9. Sequential Read



TL/D/11739–20

FIGURE 10. Typical System Configuration

National Semiconductor

NM25C04 4096-Bit Serial Interface CMOS EEPROM (Serial Peripheral Interface (SPI™) Synchronous Bus)

General Description

The NM25C04 is a 4096-bit SPI compatible CMOS EEPROM. The NM25C04 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI protocol for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C04 is implemented in National Semiconductor's single poly, double metal CMOS process which provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Serial Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

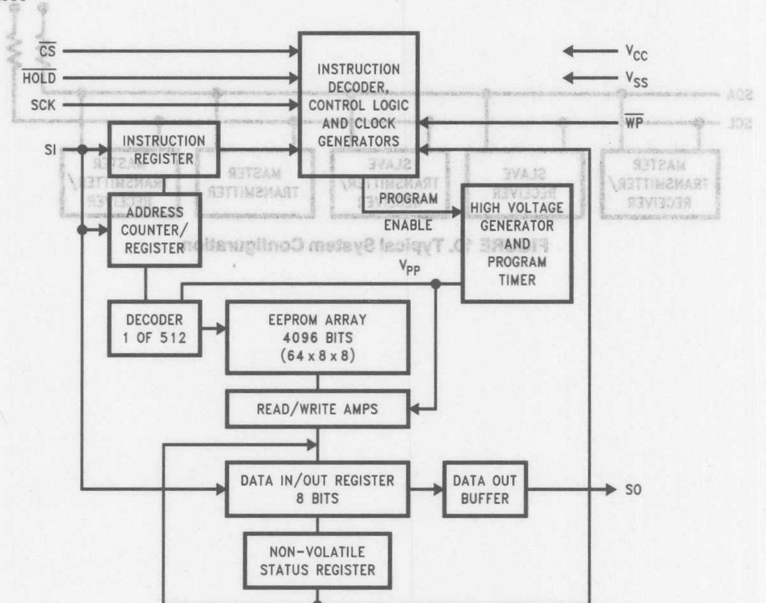
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate program enable and program disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against accidental data changes. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 4096 bits organized as 512 bytes
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor RDY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP or 8-pin SO

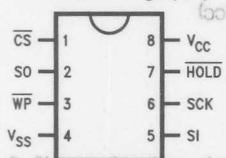
Block Diagram



TL/D/11364-1

Connection Diagram

Dual-In-Line Package (N) and SO Package (M8)



TL/D/11364-2

Top View

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Input
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM25C04N NM25C04M8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM25C04EN NM25C04EM8

Military Temperature Range (−55°C to +125°C)

Order Number
NM25C04MN NM25C04MM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C04	−0°C to +70°C
NM25C04E	−40°C to +85°C
NM25C04M	−55°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$ (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC}	Operating Current	NM25C04	$\overline{CS} = V_{IL}$		3	mA
		NM25C04E			3	mA
		NM25C04M			3	mA
I_{CCSB}	Standby Current	NM25C04	$\overline{CS} = V_{CC}$		150	μA
		NM25C04E			150	μA
		NM25C04M			150	μA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC}	−1	1	μA
I_{OL}	Output Leakage	NM25C04	V_{OUT} = 0V to V_{CC}	−1	1	μA
		NM25C04E		−1	+1	μA
		NM25C04M		−1	+1	μA
V_{IL}	Input Low Voltage			−0.3	0.3 * V_{CC}	V
V_{IH}	Input High Voltage			0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	NM25C04	I_{OL} = 1.6 mA		0.4	V
		NM25C04E			0.4	V
		NM25C04M			0.4	V
V_{OH}	Output High Voltage		I_{OH} = 0.8 mA	V_{CC} − 0.8		V
f_{OP}	SCK Frequency	NM25C04			2.1	MHz
		NM25C04E			1	MHz
		NM25C04M			1	MHz
t_{RI}	Input Rise Time				2.0	μs
t_{FI}	Input Fall Time				2.0	μs
t_{CLH}	Clock High Time	NM25C04	Note 2	190		ns
		NM25C04E		410		ns
		NM25C04M		410		ns
t_{CLL}	Clock Low Time	NM25C04	Note 2	190		ns
		NM25C04E		410		ns
		NM25C04M		410		ns
t_{CSH}	Min $\overline{CS}$ High Time	NMC25C04	Note 3	240		ns
		NM25C04E		500		ns
		NM25C04M		500		ns
t_{CSS}	$\overline{CS}$ Setup Time	NM25C04		240		ns
		NM25C04E		500		ns
		NM25C04M		500		ns
t_{DIS}	Data Setup Time	NM25C04		100		ns
		NM25C04E		100		ns
		NM25C04M		100		ns

		NM25C04E		90		ns
		NM25C04M		90		ns
t_{CSN}	$\overline{CS}$ Hold Time	NM25C04		240		ns
		NM25C04E		500		ns
		NM25C04M		500		ns
t_{DIN}	Data Hold Time			100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			90		ns
t_{PD}	Output Delay	NM25C04	$C_L = 200$ pF		240	ns
		NM25C04E			360	ns
		NM25C04M			360	ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z	NM25C04			100	ns
		NM25C04E			500	ns
		NM25C04M			500	ns
t_{DF}	Output Disable Time	NM25C04	$C_L = 200$ pF		240	ns
		NM25C04E			500	ns
		NM25C04M			500	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z	NM25C04			100	ns
		NM25C04E			500	ns
		NM25C04M			500	ns
t_{WP}	Write Cycle Time		1–4 Bytes		5	ms

Capacitance (Note 4)

$T_A = 25°C$, f = 1 MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	$C_L = 200$ pF
Input Pulse Levels	0.8V to 3.5V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SCK frequency specification specifies a minimum clock period of 476 ns; therefore, in an SCK clock cycle $t_{CLH} + t_{CLL}$ must be greater than or equal to 476 ns. For example, if $t_{CLL} = 190$ ns, then the minimum $t_{CLH} = 286$ ns in order to meet the SCK freqency specification.

Note 3: $\overline{CS}$ must be brought high for a minimum of 240 ns (t_{CSH}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

2

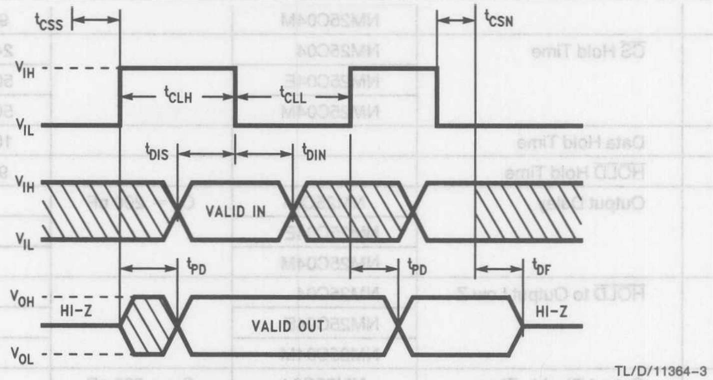


FIGURE 1. Timing Diagram

Note: When connected to the SPI port of a 68HC11 microcontroller, the NM25C04 accepts only a clock phase of 1 and a clock parity of 0.

Clock Phase 1: $\overline{CS}$ is held LOW during all serial communications and is held HIGH only between instructions.

Clock Polarity 0: Clock data IN on negative clock edge and clock data OUT on positive clock edge.

SPI Serial Interface

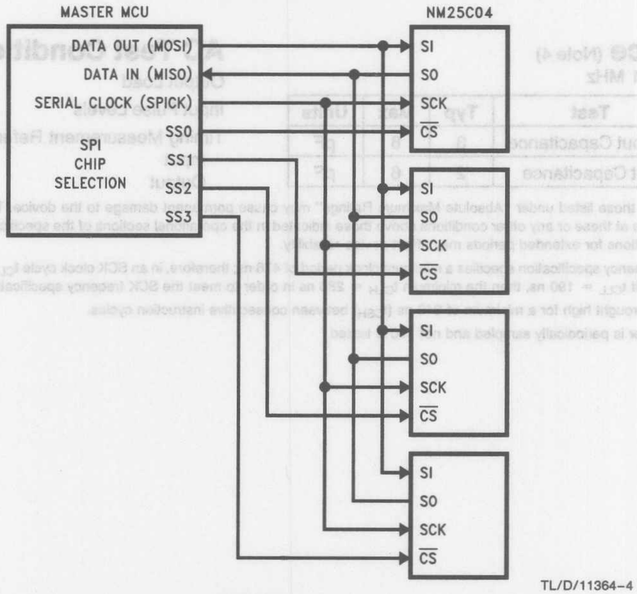


FIGURE 2

Lexicon

This lexicon describes terms used in this serial interface description.

MASTER: The device that generates the serial clock is designated as the master. The NM25C04 can never function as a master.

SLAVE: The NM25C04 always operates as a slave as the serial clock pin is always an input.

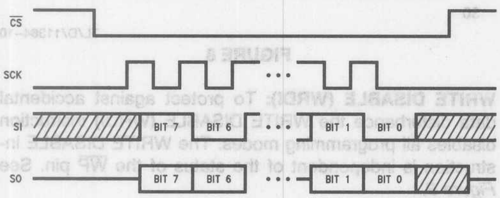
TRANSMITTER/RECEIVER: The NM25C04 has separate pins for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the op-code that defines the operation to be performed. In the READ and WRITE instructions the op-code also contains address bit A8.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C04 accepts only a clock phase of 1 and a clock polarity of 0. The SPI protocol for this device defines the bytes transmitted on the SI and SO data lines for proper chip operation. See *Figure 3*.



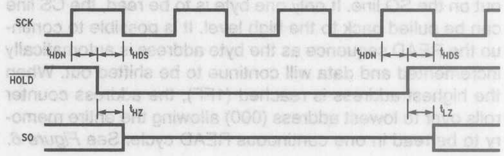
TL/D/11364–5

FIGURE 3

Phase 1: $\overline{CS}$ is held LOW during all serial communications and is held HIGH only between instructions.

Polarity 0: Clock data IN on negative SCK edge and clock data OUT on positive SCK edge.

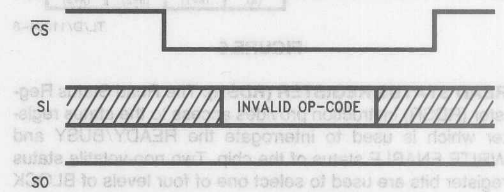
HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is high. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is high. Pins SI, SCK, and SO are at a high impedance state during HOLD. See *Figure 4*.



TL/D/11364–6

FIGURE 4. $\overline{HOLD}$ Timing

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C04, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge re-initializes the serial communication. See *Figure 5*.



TL/D/11364–7

FIGURE 5

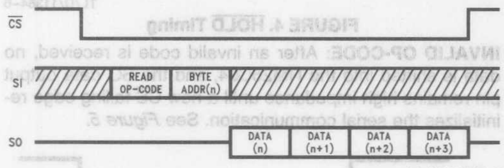
TABLE 1

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array

Note: "A" represents MSB address bit A8.

READ SEQUENCE: (One or More Bytes)

Reading the memory via the SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached (1FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See *Figure 6*.



TL/D/11364-8

FIGURE 6

READ STATUS REGISTER (RDSR): The Read Status Register (RDSR) instruction provides access to the status register which is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

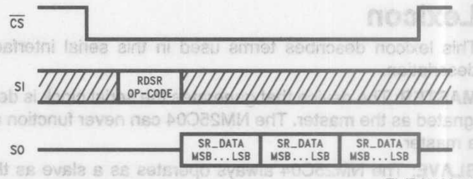
TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	BP1	BP0	WEN	$\overline{RDY}$

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s. See *Figure 7*.

TABLE 3. Block Write Protection Levels

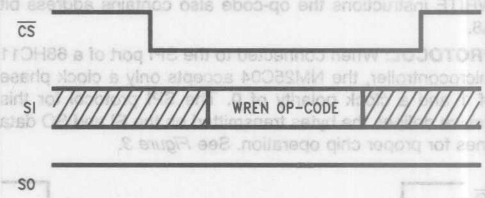
Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1	0	1	180–1FF
2	1	0	100–1FF
3	1	1	000–1FF



TL/D/11364-9

FIGURE 7

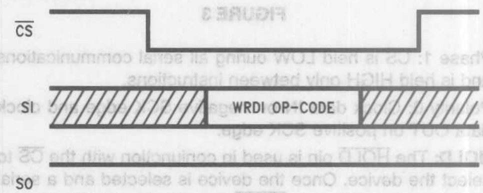
WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. Additionally the $\overline{WP}$ pin must be held high during a WRITE ENABLE instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction or forcing the $\overline{WP}$ pin low will also return the device to the write disable state. See *Figure 8*.



TL/D/11364-10

FIGURE 8

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. The WRITE DISABLE instruction is independent of the status of the $\overline{WP}$ pin. See *Figure 9*.



TL/D/11364-11

FIGURE 9

WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

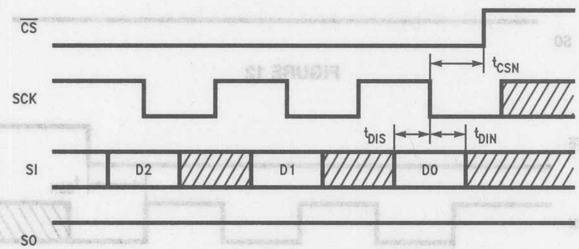
A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) and the corresponding data (D7–D0) to be programmed. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See *Figure 10.* The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER

struction is enabled.

The NM25C04 is capable of a four byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than four bytes of data, the address counter will "roll over", and the previously loaded data will be reloaded.

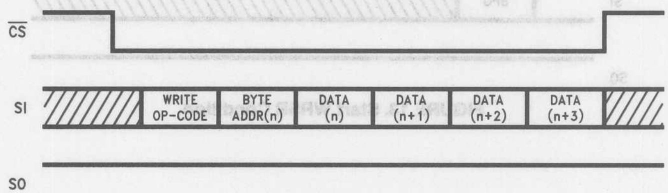
At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the $\overline{WP}$ pin is forced low or the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when $\overline{CS}$ is forced high. A new $\overline{CS}$ falling edge is required to re-initialize the serial communication. See *Figure 11.*



TL/D/11364–13

FIGURE 10. Start WRITE Condition



TL/D/11364–12

FIGURE 11

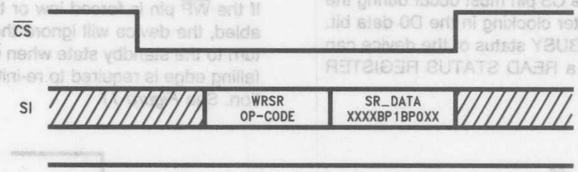
2

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). As in the WRITE mode the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed (see *Figure 12*). Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the $\overline{CS}$ pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the last don't care bit. See *Figure 13*.

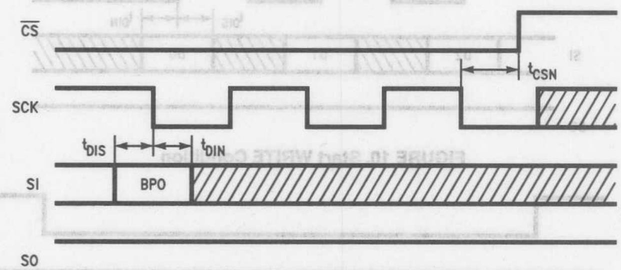
The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRSR cycle the device is automatically returned to the write disable state.



TL/D/11364-14

FIGURE 12



TL/D/11364-15

FIGURE 13. Start WRSR Condition

National Semiconductor

NM25C04L 4096-Bit Serial Interface CMOS EEPROM (Serial Peripheral Interface (SPI™) Synchronous Bus)

General Description

The NM25C04L is a 4096-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C04L is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C04L is implemented in National Semiconductor's single poly, double metal CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{\text{CS}}$), Clock (SCK), Data In (SI), and Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

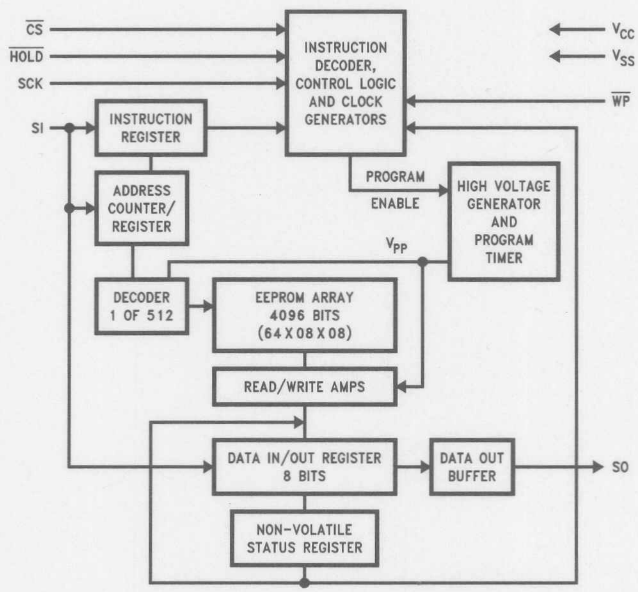
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate program enable and program disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{\text{WP}}$ pin to protect against accidental data changes. The $\overline{\text{HOLD}}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 4096 bits organized as 512 bytes
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 4 bytes at a time
- Status register can be polled during programming to monitor RDY/BUSY
- Write Protect ($\overline{\text{WP}}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 10^6 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP or 8-pin SO

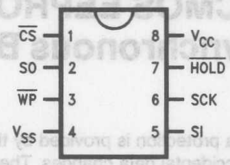
Block Diagram



TL/D/11729–1

Connection Diagram

Dual-In-Line Package (N) and SO Package (M8)



TL/D/11729-2

Top View

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Input
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to +70°C)

Order Number
NM25C04LN NM25C04LM8

Extended Temperature Range (−40°C to +85°C)

Order Number
NM25C04LEN NM25C04LEM8

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C04L	−0°C to +70°C
NM25C04LE	−40°C to +85°C
Power Supply (V_{CC})	
Read Mode	2.0V to 5.5V
All Other Modes	2.5V to 5.5V

DC and AC Electrical Characteristics $4.5V \le V_{CC} \le 5.5V$ (unless otherwise specified)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC}	Operating Current	NM25C04L	$\overline{CS} = V_{IL}$		3	mA
		NM25C04LE			3	mA
I_{CCSB}	Standby Current	NM25C04L	$\overline{CS} = V_{CC}$		150	μA
		NM25C04LE			150	μA
I_{IL}	Input Leakage		V_{IN} = 0V to V_{CC}	−1	1	μA
I_{OL}	Output Leakage	NM25C04L	V_{OUT} = 0V to V_{CC}	−1	1	μA
		NM25C04LE		−1	+1	μA
V_{IL}	Input Low Voltage			−0.3	0.3 * V_{CC}	V
V_{IH}	Input High Voltage			0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	NM25C04L	I_{OL} = 10μA		0.2* V_{CC}	V
		NM25C04LE			0.2* V_{CC}	V
V_{OH}	Output High Voltage		I_{OH} = 10 μA	0.8 * V_{CC}		V
f_{OP}	SCK Frequency	NM25C04L			1	MHz
		NM25C04LE			1	MHz
t_{RI}	Input Rise Time				2.0	μs
t_{FI}	Input Fall Time				2.0	μs
t_{CLH}	Clock High Time	NM25C04L	Note 2	500		ns
		NM25C04LE		500		ns
t_{CLL}	Clock Low Time	NM25C04L	Note 2	500		ns
		NM25C04LE		500		ns
t_{CSH}	Min $\overline{CS}$ High Time	NMC25C04L	Note 3	500		ns
		NM25C04LE		500		ns
t_{CSS}	$\overline{CS}$ Setup Time	NM25C04L		500		ns
		NM25C04LE		500		ns
t_{DIS}	Data Setup Time	NM25C04L		100		ns
		NM25C04LE		100		ns

2

t_{HDS}	HOLD Setup Time	NM25C04L		200		ns
		NM25C04LE		200		ns
t_{CSN}	$\overline{CS}$ Hold Time	NM25C04L		500		ns
		NM25C04LE		500		ns
t_{DIN}	Data Hold Time			100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			200		ns
t_{PD}	Output Delay	NM25C04L	$C_L = 200$ pF		500	ns
		NM25C04LE			500	ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z	NM25C04L			500	ns
		NM25C04LE			500	ns
t_{DF}	Output Disable Time	NM25C04L	$C_L = 200$ pF		500	ns
		NM25C04LE			500	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z	NM25C04L			500	ns
		NM25C04LE			500	ns
t_{WP}	Write Cycle Time		1–4 Bytes		10	ms

Capacitance (Note 4)

$T_A = 25°C$, $f = 1$ MHz

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	$I_{OL} = 10\ \mu A$, $I_{OH} = 10\ \mu A$
Input Pulse Levels	0.3V and 1.8V
Timing Measurement Reference Level	
Input	0.4V and 1.6V
Output	0.8V and 1.6V

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The SCK frequency specification specifies a minimum clock period of 1000 ns; therefore, in an SCK clock cycle $t_{CLH} + t_{CLL}$ must be greater than or equal to 1000 ns. For example, if $t_{CLL} = 410$ ns, then the minimum $t_{CLH} = 550$ ns in order to meet the SCK freqency specification.

Note 3: $\overline{CS}$ must be brought high for a minimum of 500 ns (t_{CSH}) between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

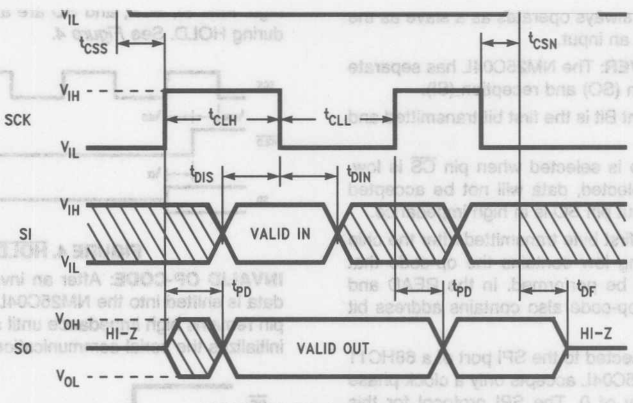


FIGURE 1. Timing Diagram

Note: When connected to the SPI port of a 68HC11 microcontroller, the NM25C04L accepts only a clock phase of 1 and a clock parity of 0.

Clock Phase 1: $\overline{CS}$ is held LOW during all serial communications and is held HIGH only between instructions.

Clock Polarity 0: Clock data IN on negative clock edge and clock data OUT on positive clock edge.

SPI Serial Interface

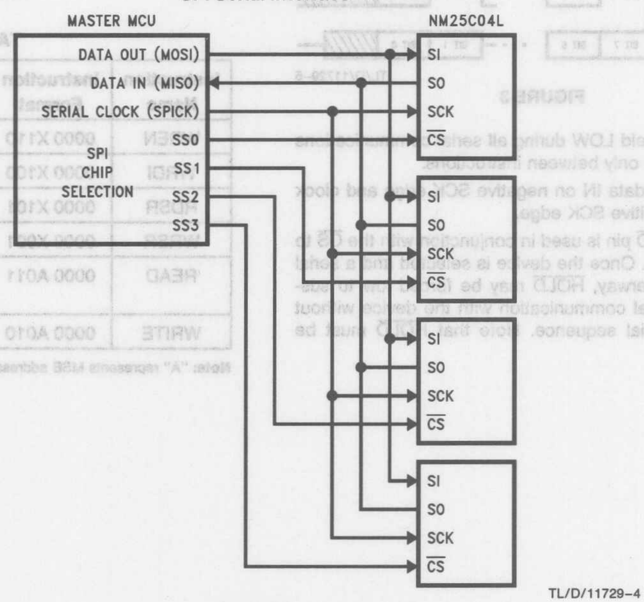


FIGURE 2

Functional Description

MASTER: The device that generates the serial clock is designated as the master. The NM25C04L can never function as a master.

SLAVE: The NM25C04L always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C04L has separate pins for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{\text{CS}}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{\text{CS}}$ going low contains the op-code that defines the operation to be performed. In the READ and WRITE instructions the op-code also contains address bit A8.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C04L accepts only a clock phase of 1 and a clock polarity of 0. The SPI protocol for this device defines the bytes transmitted on the SI and SO data lines for proper chip operation. See *Figure 3*.

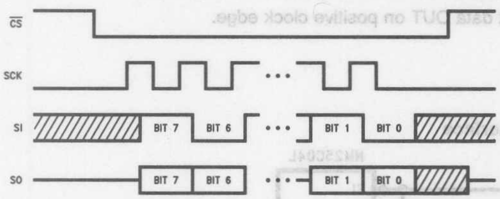


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FIGURE 3

Phase 1: $\overline{\text{CS}}$ is held LOW during all serial communications and is held HIGH only between instructions.

Polarity 0: Clock data IN on negative SCK edge and clock data OUT on positive SCK edge.

HOLD: The $\overline{\text{HOLD}}$ pin is used in conjunction with the $\overline{\text{CS}}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{\text{HOLD}}$ must be brought low while the SCK pin is high. The device must remain selected during this sequence. To resume serial communication $\overline{\text{HOLD}}$ is brought high while the SCK pin is high. Pins SI, SCK, and SO are at a high impedance state during HOLD. See *Figure 4*.

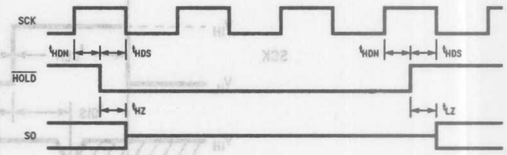

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FIGURE 4. $\overline{\text{HOLD}}$ Timing

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C04L, and the SO data output pin remains high impedance until a new $\overline{\text{CS}}$ falling edge re-initializes the serial communication. See *Figure 5*.

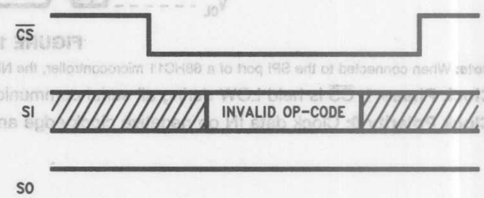

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FIGURE 5

TABLE 1

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 A011	Read Data from Memory Array
WRITE	0000 A010	Write Data to Memory Array

Note: "A" represents MSB address bit A8.

READ SEQUENCE: (One or More Bytes)

Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) to be read. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached (1FF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See *Figure 6*.

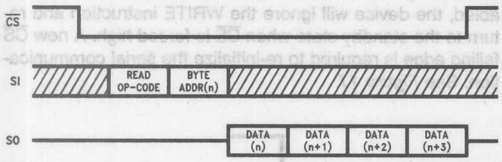

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FIGURE 6

READ STATUS REGISTER (RDSR): The Read Status Register (RDSR) instruction provides access to the status register which is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	1	1	BP1	BP0	WEN	$\overline{RDY}$

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. Note that if a RDSR instruction is executed during a programming cycle only the $\overline{RDY}$ bit is valid. All other bits are 1s. See *Figure 7*.

TABLE 3. Block Write Protection Levels

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1	0	1	180–1FF
2	1	0	100–1FF
3	1	1	000–1FF

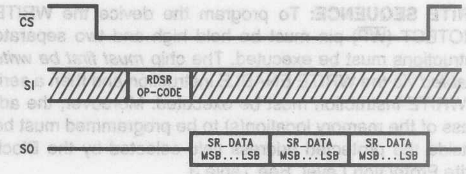

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FIGURE 7

WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. Additionally the $\overline{WP}$ pin must be held high during a WRITE ENABLE instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRDI) instruction or forcing the $\overline{WP}$ pin low will also return the device to the write disable state. See *Figure 8*.

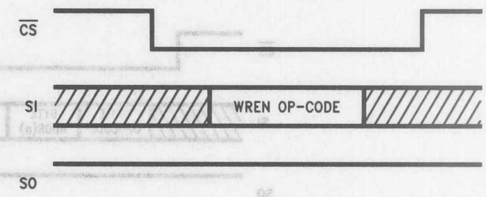

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FIGURE 8

WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. The WRITE DISABLE instruction is independent of the status of the $\overline{WP}$ pin. See *Figure 9*.

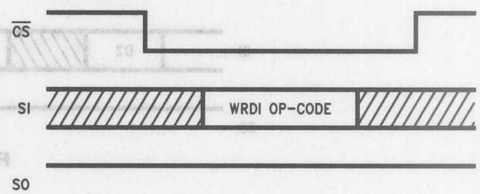

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FIGURE 9

WRITE SEQUENCE: To program the device the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip *must first be write enabled* via the WRITE ENABLE instruction and then a serial WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A serial WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code (which includes A8) is transmitted on the SI line followed by the byte address (A7–A0) and the corresponding data (D7–D0) to be programmed. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See *Figure 10*. The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C04L is capable of a four byte PAGE WRITE operation. After receipt of each byte of data the two low order address bits are internally incremented by one. The seven high order bits of the address will remain constant. If the master should transmit more than four bytes of data, the address counter will "roll over", and the previously loaded data will be reloaded.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the $\overline{WP}$ pin is forced low or the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when $\overline{CS}$ is forced high. A new $\overline{CS}$ falling edge is required to re-initialize the serial communication. See *Figure 11*.

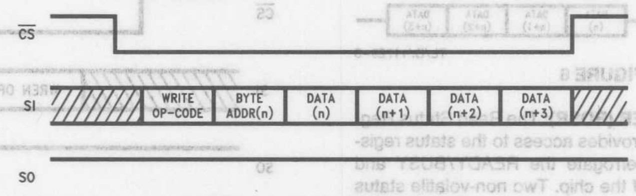

FIGURE 10. Start WRITE Condition

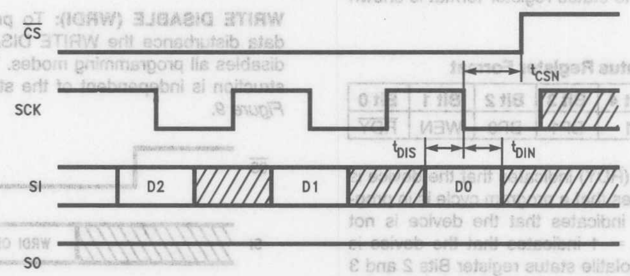

FIGURE 11

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). As in the WRITE mode the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a serial WRSR instruction must be executed.

The serial WRSR command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed (see *Figure 12*). Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the $\overline{CS}$ pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the last don't care bit. See *Figure 13*.

The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRSR cycle the device is automatically returned to the write disable state.

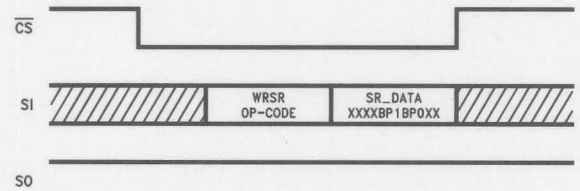

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FIGURE 12

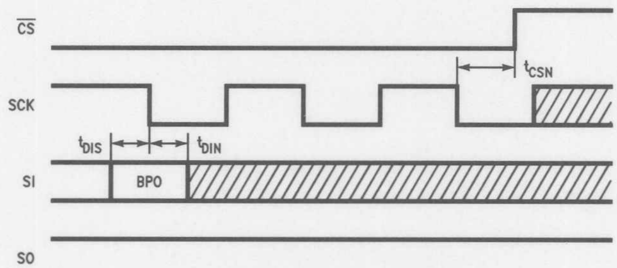

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FIGURE 13. Start WRSR Condition

2

Section 3
CMOS EPROMs

Section 3 Contents

National Semiconductor

CMOS EPROM Selection Guide Standard Products

General Description

National Semiconductor's family of high performance CMOS EPROMs offer the following shared features: pin compatibility with byte-wide JEDEC EPROMs; "Don't Care" feature during read operations; high speed operation with high performance CPUs such as the 80186, 68020, 80386; single chip solutions for the code storage requirements of 100% firmware based equipment.

This family of EPROMs are available in densities from 16k-bit to 4 Mbit and a variety of packages including CerDIP, PLCC, OTP and TSOP.

Features

- High performance CMOS
  — 90 ns access time
- Fast programming
- EPI processing
  — Latch-up immunity
  — ESD protection
- Compatible with JEDEC EPROM configurations
- Simplified upgrade path
  — V_{PP} and PGM are "Don't Care" during normal read operation
- Single 5V power supply

Available Product

	Packages	Temperature Ranges	Speed
NMC27C16B	Q	C, E	150 ns, 200 ns
NMC27C32B	Q	C, E	200 ns
NMC27C64	Q, N	C, E, M*	150 ns, 200 ns
NM27C128	Q, N	C, E	200 ns, 250 ns
NM27C256	Q, V, N	C, E	100 ns, 150 ns, 200 ns
NM27C512	Q, V, N	C, E	90 ns, 150 ns, 200 ns
NM27C010	Q, V, N, T	C, E	90 ns, 150 ns, 200 ns
NM27C210	Q, V	C, E	120 ns, 150 ns, 200 ns
NM27C020	Q, T	C, E	150 ns, 200 ns
NM27C040	Q	C, E	120 ns, 170 ns, 200 ns

*N package available only in commercial temperature range (0°C to +70°C).

Note: All products will operate at speeds slower than those listed.

NM 27 C 512 Q E 120

- NM — National Memory
- 27 — EPROM
- C — CMOS
- 512 — Size
  512 = 512k-bit
- Q — Package
  Q = Ceramic DIP
  N = OTP DIP
  V = PLCC
  T = TSOP
- E — Operating Temperature Range
  Blank = 0°C to +70°C
  E = −40°C to +85°C
- 120 — Access Time (speed)
  120 = 120 ns

National Semiconductor

NMC27C16B 16,384-Bit (2048 x 8) CMOS EPROM

General Description

The NMC27C16B is a high performance 16K UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

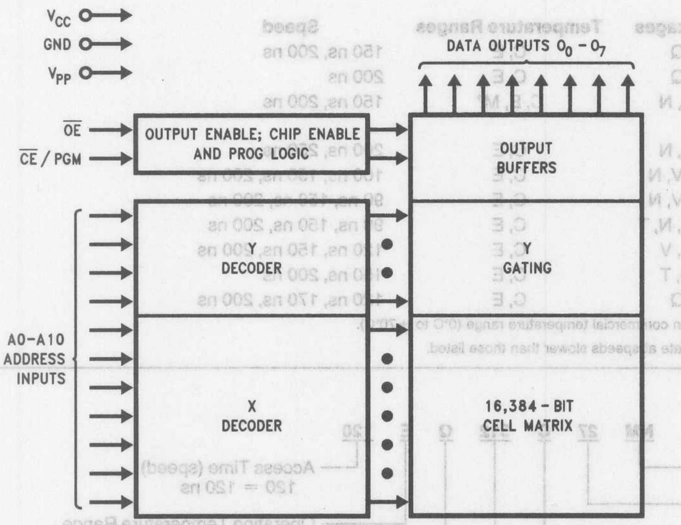
The NMC27C16B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Low CMOS power consumption
  Active power: 55 mW max
  Standby power: 0.55 mW max
- Extended temperature range available, −40°C to +85°C
- Fast and reliable programming (100 μs for most bytes)
- TTL compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming equipment
- High current CMOS level output drivers
- Upgrade for NMOS 2716

Block Diagram



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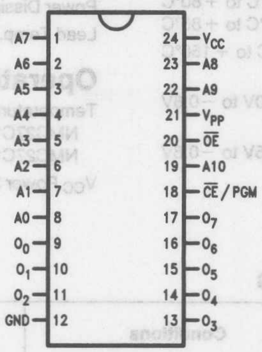
Pin Names

A0–A10	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
PGM	Program
NC	No Connect

V_{PP}	V_{PP}	V_{PP}	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
GND	GND	GND	GND

Dual-In-Line Package



	V_{CC}	V_{CC}	V_{CC}
	$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
A11	A11	A11	A11
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3

TL/D/9180-2

Top View

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16B pins.

Order Number NMC27C16BQ
See NS Package Number J24AQ

Commercial Temp. Range (0°C to 70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQ150	150
NMC27C16BQ200	200

Extended Temp. Range (−40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C16BQE150	150
NMC27C16BQE200	200

3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	
Commercial Parts	$-10°C$ to $+80°C$
Extended Temp. Parts	$-40°C$ to $+85°C$
Storage Temperature	$-65°C$ to $+150°C$
V_{CC} Supply with Respect to Ground	$+7.0V$ to $-0.6V$
All Input Voltages except A9 with Respect to Ground (Note 10)	$+6.5V$ to $-0.6V$
All Output Voltages with Respect to Ground (Note 10)	$V_{CC}+1.0V$ to $GND-0.6V$
V_{PP} Supply and A9 Voltage with Respect to Ground	$+14.0V$ to $-0.6V$
Power Dissipation	1.0W
Lead Temp. (Soldering, 10 sec.)	300°C

Operating Conditions (Note 8)

Temperature Range	
NMC27C16BQ150, 200	$0°C$ to $+70°C$
NMC27C16BQE150, 200	$-40°C$ to $+85°C$
V_{CC} Power Supply	$+5V \pm 10\%$

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 11)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.1	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.1	1	μA
I_{CC1} (Note 3)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL} I/O = 0 mA		5	20	mA
I_{CC2} (Note 3)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = 5.5V$			10	μA
V_{IL}	Input Low Voltage		-0.2		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -400$ mA	2.4			V
V_{OL2}	Output Low Voltage	$I_{OL} = 10\ \mu A$			0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = -10\ \mu A$	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C16BQ				Units
			Q150, QE150		Q200, QE200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{OE} = \overline{OE} = V_{IL}$	0		0		ns

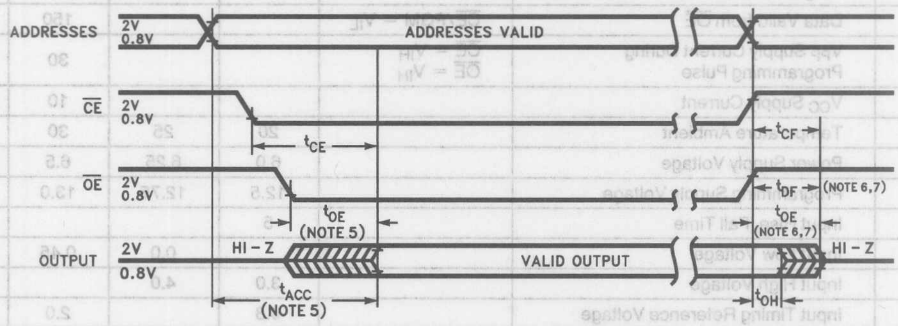
Capacitance $T_A = +25°C$, f = 1 MHz (Note 4)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load (Note 12)	1 TTL Gate and $C_L = 100$ pF	Timing Measurement Reference Level	
Input Rise and Fall Times	≤ 5 ns	Inputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V	Outputs	0.8V and 2V

AC Waveforms (Notes 2 & 9)



TL/D/9180–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. $I_{CC1} \leq$ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: This parameter is only sampled and is not 100% tested.

Note 5: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 6: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 7: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 8: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 9: The outputs must be restricted to $V_{CC} + 1.0V$ to avoid latch-up and device damage.

Note 10: Inputs and outputs can undershoot to $-2.0V$ for 20 ns maximum.

Note 11: Typical values are for $T_A = 25°C$ and nominal supply voltages.

Note 12: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = 400$ μA.
C_L: 100 pF inlcudes fixture capacitance.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/PGM = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		3.0	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

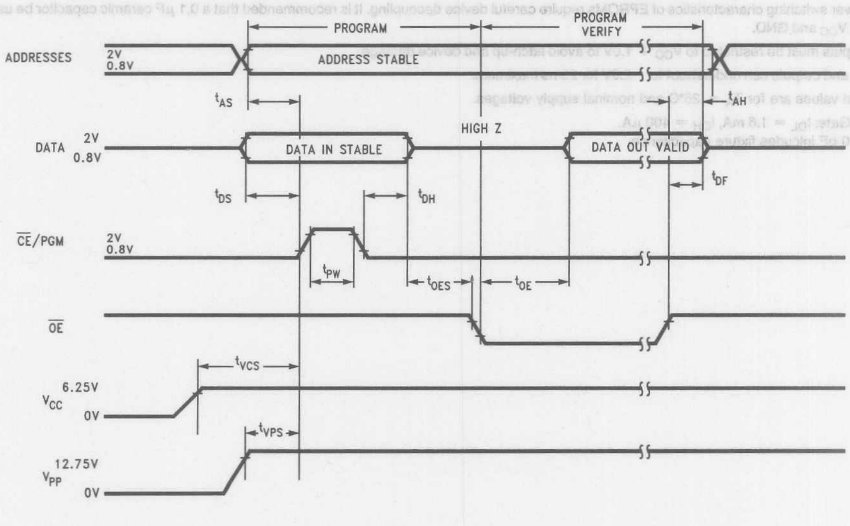
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

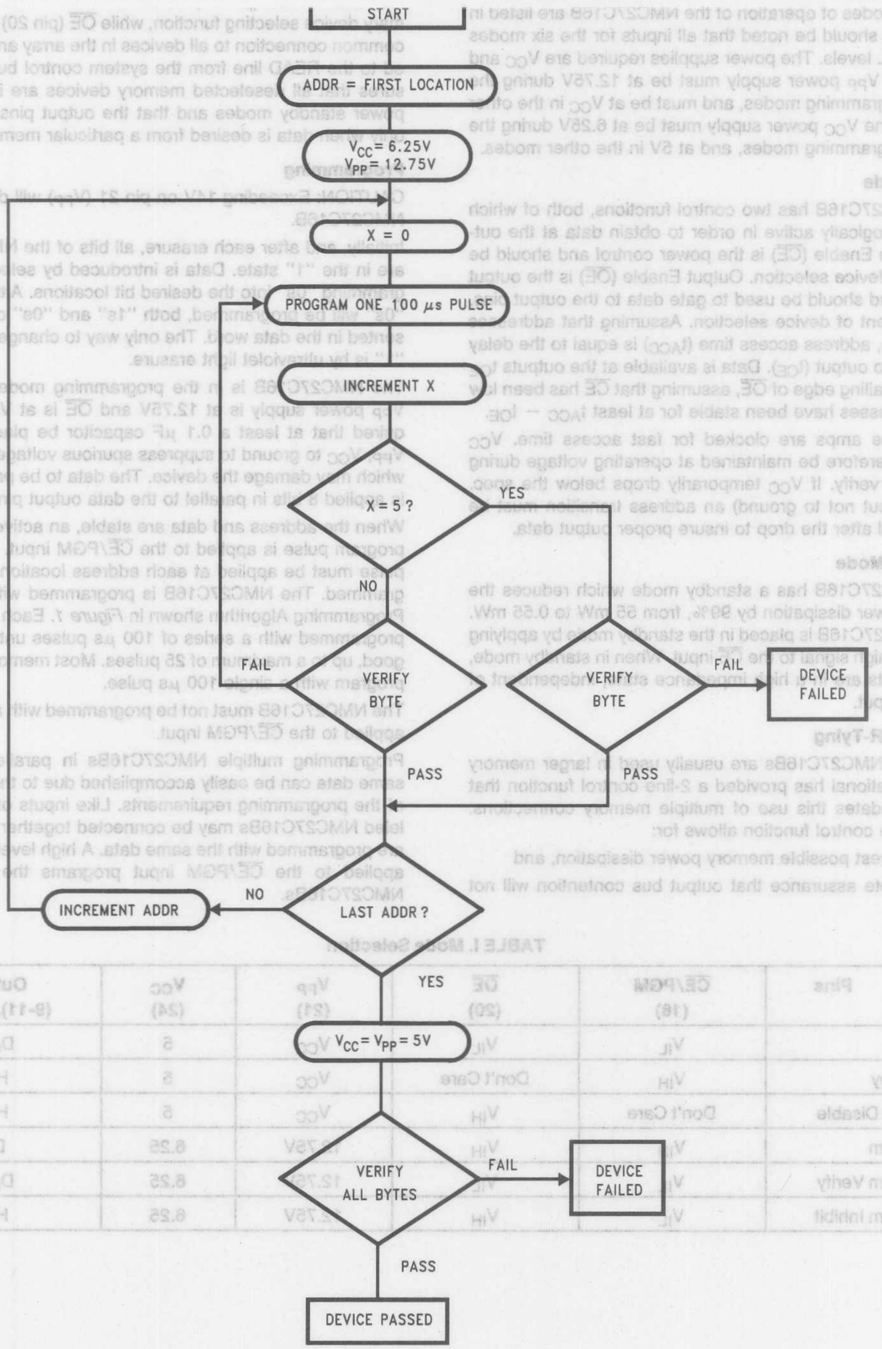
Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max Limit Parameters are Design parameters, not Tested or guaranteed.

Programming Waveforms



TL/D/9180–4



TL/D/9180–5

FIGURE 1

Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at V_{CC} in the other modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other modes.

Read Mode

The NMC27C16B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C16B has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C16B is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output OR-Tying

Because NMC27C16Bs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

mary device selecting function, while $\overline{\text{OE}}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 21 (V_{PP}) will damage the NMC27C16B.

Initially, and after each erasure, all bits of the NMC27C16B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16B is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{\text{OE}}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins.

When the address and data are stable, an active high, TTL program pulse is applied to the $\overline{\text{CE}}$/PGM input. A program pulse must be applied at each address location to be programmed. The NMC27C16B is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The NMC27C16B must not be programmed with a DC signal applied to the $\overline{\text{CE}}$/PGM input.

Programming multiple NMC27C16Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16Bs may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{\text{CE}}$/PGM input programs the paralleled NMC27C16Bs.

TABLE I. Mode Selection

Pins / Mode	$\overline{\text{CE}}$/PGM (18)	$\overline{\text{OE}}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11), (13-17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{CC}	5	Hi-Z
Program	V_{IH}	V_{IH}	12.75V	6.25	D_{IN}
Program Verify	V_{IL}	V_{IL}	12.75V	6.25	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	12.75V	6.25	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C16Bs in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM all like inputs (including $\overline{OE}$) of the parallel NMC27C16Bs may be common. A TTL high level program pulse applied to an NMC27C16B's $\overline{CE}$/PGM input with V_{PP} at 12.75V will program that NMC27C16B. A TTL low level $\overline{CE}$/PGM input inhibits the other NMC27C16Bs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. Except during programming and program verify, V_{PP} must be at V_{CC}.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C16B has a manufacturer's identification code to aid in programming. The code, shown in Table III, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C16B is, "8F80", where "8F" designates that it is made by National Semiconductor, and "80" designates a 16k part.

The code is accessed by applying 12.0V $\pm$0.5V to address pin A9. Addresses A1–A8, A10, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C $\pm$5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C16B window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a mimimum of 15 W-sec/cm^2.

The NMC27C16B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table II shows the minimum NMC27C16B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Minimum NMC27C16B Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

TABLE III. Manufacturer's Identification Code

Pins	A_0 (8)	O_7 (17)	O_6 (16)	O_5 (15)	O_4 (14)	O_3 (13)	O_2 (11)	O_1 (10)	O_0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	0	0	0	0	0	0	0	80

National Semiconductor

NMC27C32B 32,768-Bit (4096 x 8) CMOS EPROM

General Description

The NMC27C32B is a 32k UV erasable and electrically re-programmable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C32B is designed to operate with a single +5V power supply with ±10% tolerance.

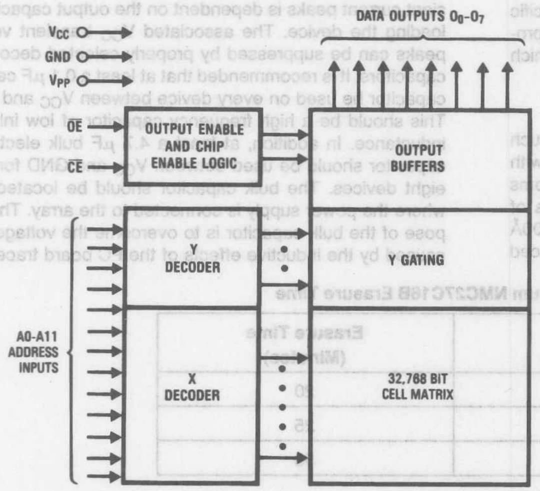
The NMC27C32B is packaged in a 24-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

This EPROM is fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- Low CMOS power consumption
  - Active Power: 55 mW Max
  - Standby Power: 0.55 mW Max
- Extended temperature range, −40°C to +85°C
- Fast and reliable programming
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming
- High current CMOS level output drivers
- Compatible with NMOS 2732

Block Diagram



TL/D/8827-1

Pin Names

A0–A11	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{PP}	Programming Voltage
O_0–O_7	Outputs
V_{CC}	Power Supply
GND	Ground

NMC27C32B
Dual-In-Line Package

27256	27128	2764	2716	NMC27C32B	Pin	Pin	NMC27C32B	2716	2764	27128	27256
V_{PP}	V_{PP}	V_{PP}							V_{CC}	V_{CC}	V_{CC}
A12	A12	A12							$\overline{PGM}$	$\overline{PGM}$	A14
A7	A7	A7	A7	A7	1	24	V_{CC}	V_{CC}	NC	A13	A13
A6	A6	A6	A6	A6	2	23	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	3	22	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	4	21	A11	V_{PP}	A11	A11	A11
A3	A3	A3	A3	A3	5	20	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A2	A2	A2	A2	A2	6	19	A10	A10	A10	A10	A10
A1	A1	A1	A1	A1	7	18	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
A0	A0	A0	A0	A0	8	17	O_7	O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	O_0	9	16	O_6	O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	O_1	10	15	O_5	O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	O_2	11	14	O_4	O_4	O_4	O_4	O_4
GND	GND	GND	GND	GND	12	13	O_3	O_3	O_3	O_3	O_3

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Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32B pins.

Order Number NMC27C32BQ
See NS Package Number J24AQ

Commercial Temp Range (0°C to +70°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQ150	150
NMC27C32BQ200	200
NMC27C32BQ250	250

Extended Temp Range (−40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C32BQE200	200

3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	−40°C to +85°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 and $\overline{OE}/V_{PP}$ with Respect to Ground (Note 9)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 9)	V_{CC}+1.0V to GND−0.6V
$\overline{OE}/V_{PP}$ Supply and A9 Voltage with Respect to Ground	+14.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions (Note 6)

Temperature Range	
NMC27C32BQ150, 200, 250	0°C to +70°C
NMC27C32BQE200	−40°C to +85°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND		0.01	1	μA
I_{PP}	$\overline{OE}/V_{PP}$ Load Current	$\overline{OE}/V_{PP} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
V_{IL}	Input Low Voltage		−0.2		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = −10 μA	V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C32B						Units
			Q150		Q200, QE200		Q250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	50	0	60	0	70	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$	0	50	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		ns

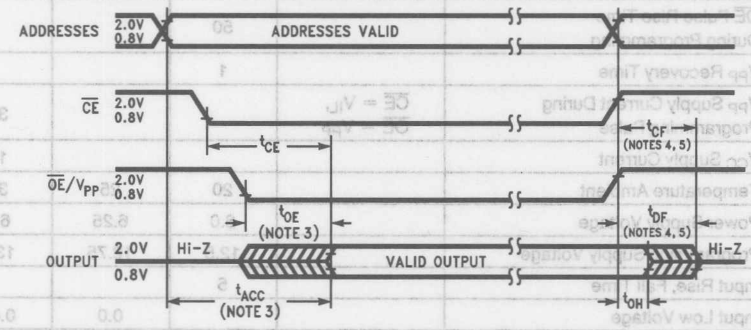
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	16	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Note 7)



TL/D/8827-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

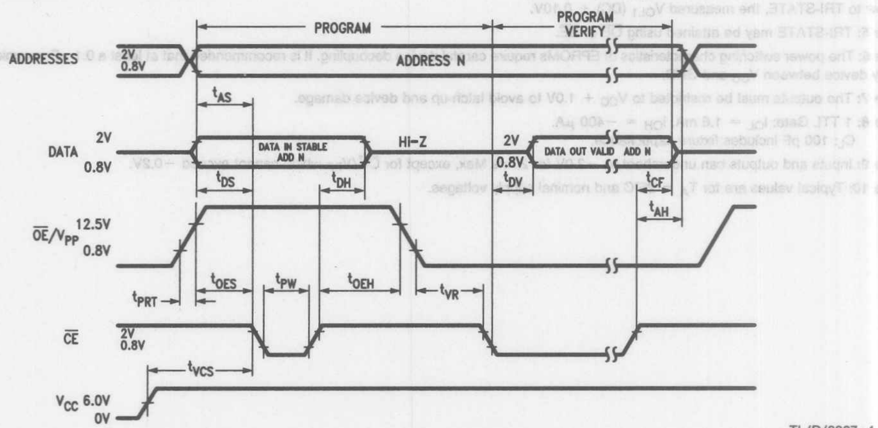
Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max, except for $\overline{OE}/V_{PP}$ which cannot exceed −0.2V.

Note 10: Typical values are for $T_A = 25°C$ and nominal supply voltages.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms



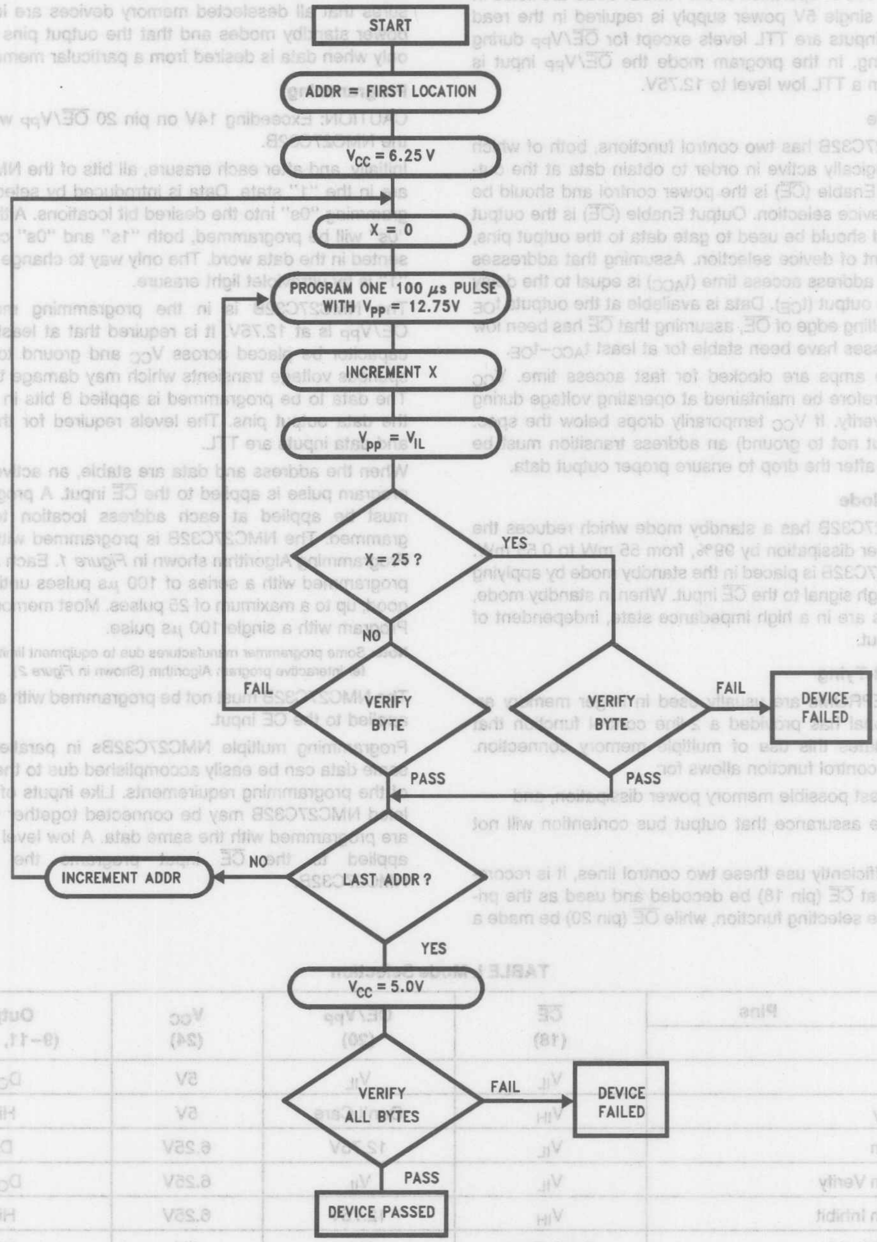
TL/D/8827-4

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.



TL/D/8827–5

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C32B are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NMC27C32B has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NMC27C32B has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C32B is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMs are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a. The lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 20 $\overline{OE}/V_{PP}$ will damage the NMC27C32B.

Initially, and after each erasure, all bits of the NMC27C32B are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C32B is in the programming mode when $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C32B is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will Program with a single 100 μs pulse.

Note: Some programmer manufactures due to equipment limitation may offer interactive program Algorithm (Shown in *Figure 2*).

The NMC27C32B must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NMC27C32Bs in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32B may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32B.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9–11, 13–17)
Read	V_{IL}	V_{IL}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	5V	Hi-Z
Program	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	Hi-Z
Output Disable	Don't Care	V_{IH}	5V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C32B in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$) of the parallel NMC27C32B may be common. A TTL low level program pulse applied to an NMC27C32B's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NMC27C32B. A TTL high level $\overline{CE}$ input inhibits the other NMC27C32B from being programmed.

Program Verify

A verify should be performed on the programmed bit to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C32B has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C32B is, "8F01", where "8F" designates that it is made by National Semiconductor, and "01" designates a 32k part.

The code is accessed by applying 12.0V ±0.5V to address pin A9. Addresses A1–A8, A10–A11, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32B are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C32B's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32B is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC27C32B should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C32B erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (8)	O_7 (17)	O_6 (16)	O_5 (15)	O_4 (14)	O_3 (13)	O_2 (11)	O_1 (10)	O_0 (9)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	0	0	1	01

TABLE III. Minimum NMC27C32B Erasure Time

Light Intensity (μW/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

National Semiconductor

NMC27C64 65,536-Bit (8192 x 8) CMOS EPROM

General Description

The NMC27C64 is a 64K UV erasable, electrically reprogrammable and one-time programmable (OTP) CMOS EPROM ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

The NMC27C64Q is packaged in a 28-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

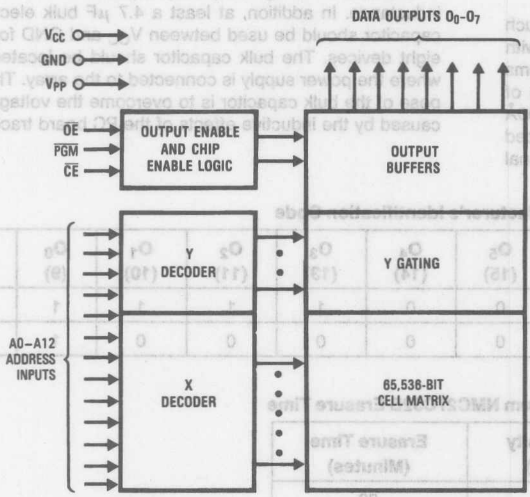
The NMC27C64N is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be one once.

This family of EPROMs are fabricated with National's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- High performance CMOS
  - — 150 ns access time
- JEDEC standard pin configuration
  - — 28-pin DIP package
  - — 32-pin chip carrier
- Drop-in replacement for 27C64 or 2764
- Manufacturers identification code

Block Diagram



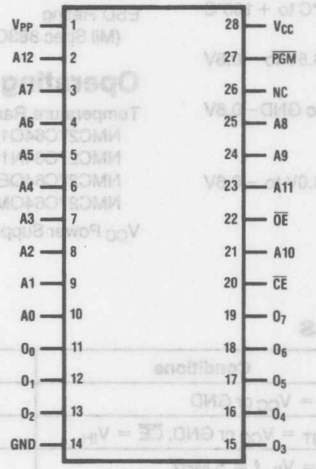
TL/D/8634-1

Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect
V_{PP}	Programming Voltage
V_{CC}	Power Supply
GND	Ground

Dual-In-Line Package

27512	27256	27128	2732	2716
A15	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND



2716	2732	27128	27256	27512
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	A14	A14
V_{CC}	V_{CC}	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}$/PGM	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/PGM	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

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Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64 pins.

Commercial Temperature Range
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64Q, N150	150
NMC27C64Q, N200	200
NMC27C64Q, N250	250

Extended Temp Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QE150	150
NMC27C64QE200	200

Military Temp Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QM200	200
NMC27C64QM250	250

3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Under Bias	$-55°C$ to $+125°C$
Storage Temperature	$-65°C$ to $+150°C$
All Input Voltages except A9 with Respect to Ground (Note 10)	$+6.5V$ to $-0.6V$
All Output Voltages with Respect to Ground (Note 10)	$V_{CC}+1.0V$ to GND$-0.6V$
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	$+14.0V$ to $-0.6V$
V_{CC} Supply Voltage with Respect to Ground	$+7.0V$ to $-0.6V$
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C64Q150, 200, 250	0°C to $+70°C$
NMC27C64N150, 200, 250	
NMC27C64QE150, 200	$-40°C$ to $+85°C$
NMC27C64QM200, M250	$-55°C$ to $+125°C$
V_{CC} Power Supply	$+5V \pm 10\%$

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC} + 1$	V
V_{OL1}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V
V_{OL2}	Output Low Voltage	$I_{OL} = 0$ μA			0.1	V
V_{OH2}	Output High Voltage	$I_{OH} = 0$ μA	$V_{CC} - 0.1$			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64Q/N						Units
			150, E150		200, E200, M200		250, M250		
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2) NMC27C64Q

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2) NMC27C64N

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	10	pF

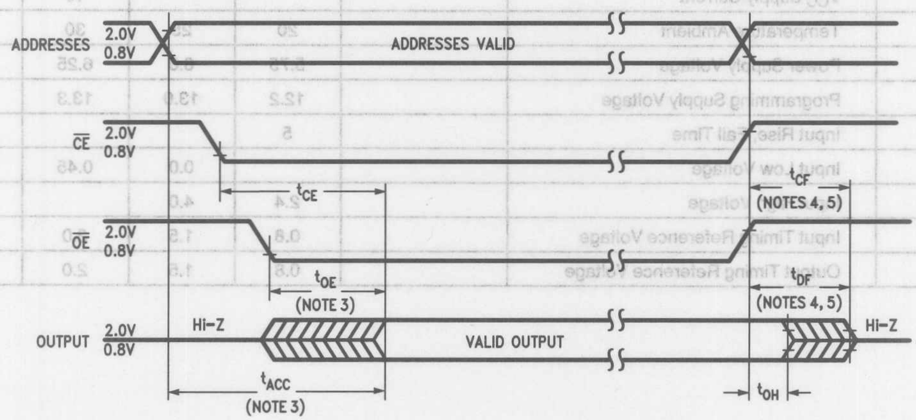
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6 & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

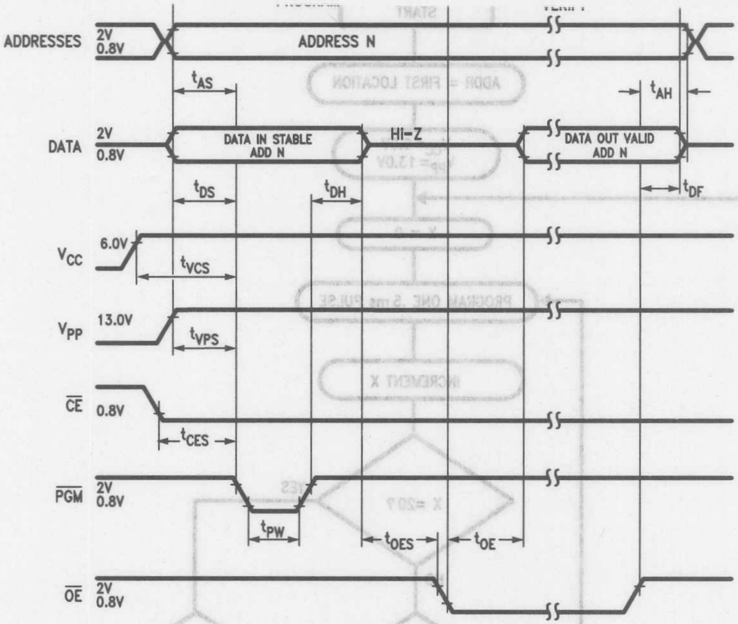
Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V



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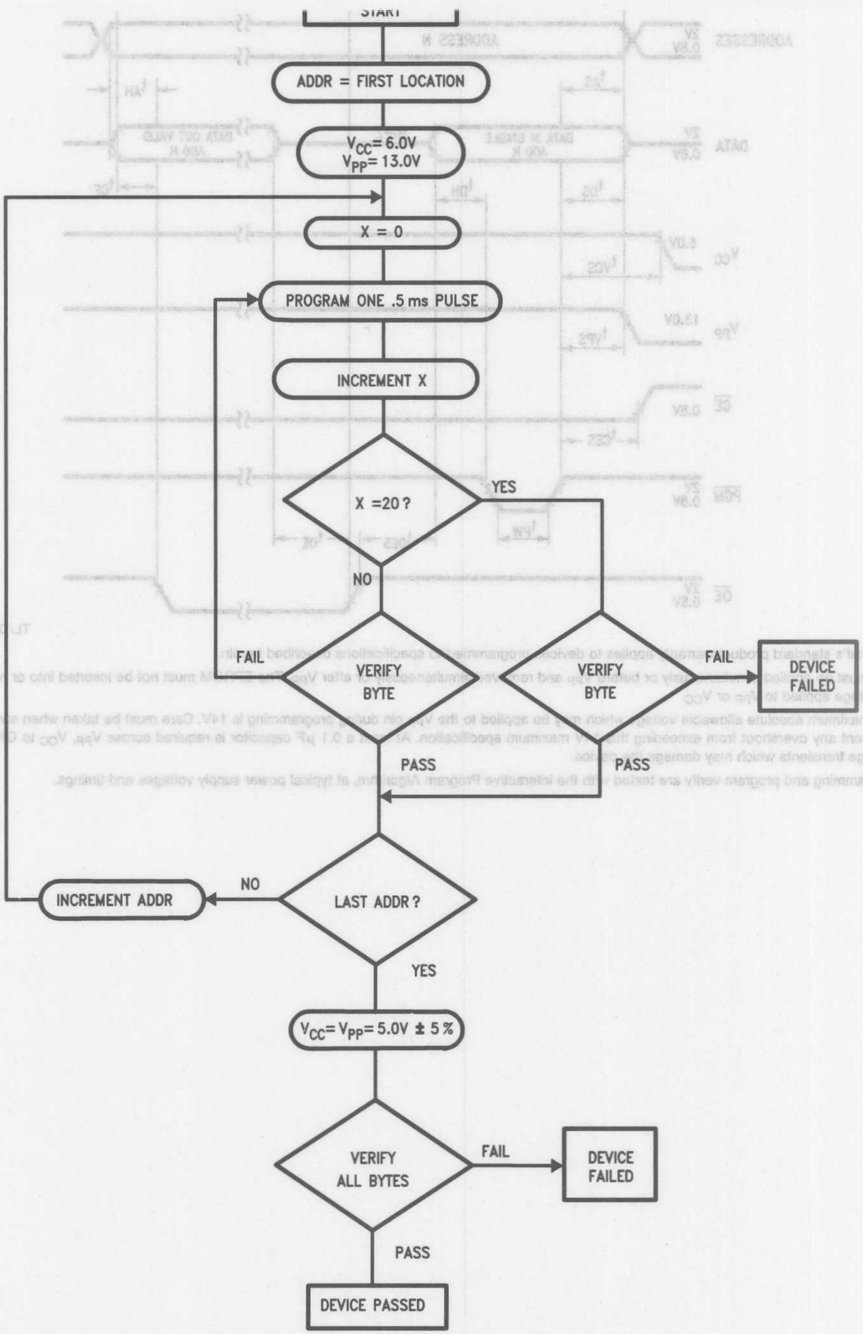
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings.

3


START
ADDR = FIRST LOCATION
V_{CC}= 6.0V
V_{PP}= 13.0V
X = 0
PROGRAM ONE .5 ms PULSE
INCREMENT X
X =20 ?
YES
NO
FAIL
VERIFY BYTE
VERIFY BYTE
FAIL
DEVICE FAILED
PASS
PASS
INCREMENT ADDR
NO
LAST ADDR ?
YES
V_{CC}= V_{PP}= 5.0V ± 5%
VERIFY ALL BYTES
FAIL
DEVICE FAILED
PASS
DEVICE PASSED

TL/D/8634–5

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64.

Initially, all bits of the NMC27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed.

The NMC27C64 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 13.0V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64 is designed to be programmed with interactive programming, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NMC27C64 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NMC27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64s. If an application requires erasing and reprogramming, the NMC27C64Q UV erasable PROM in a windowed package should be used.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}		13V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13V	6V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64 may be common. A TTL low level program pulse applied to an NMC27C64's PGM input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NMC27C64. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64 is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC27C64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C64 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of $15W\text{-}sec/cm^2$.

The NMC27C64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC27C64 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

TABLE III. Minimum NMC27C64 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

NM27C128
131,072-Bit (16K x 8) High Performance CMOS EPROM

General Description

The NM27C128 is a high performance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with National's latest CMOS split gate EPROM technology which enables it to operate at speeds as fast as 100 ns access time over the full operating range.

The NM27C128 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 100ns access time provides high speed operation with high-performance CPUs. The NM27C128 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

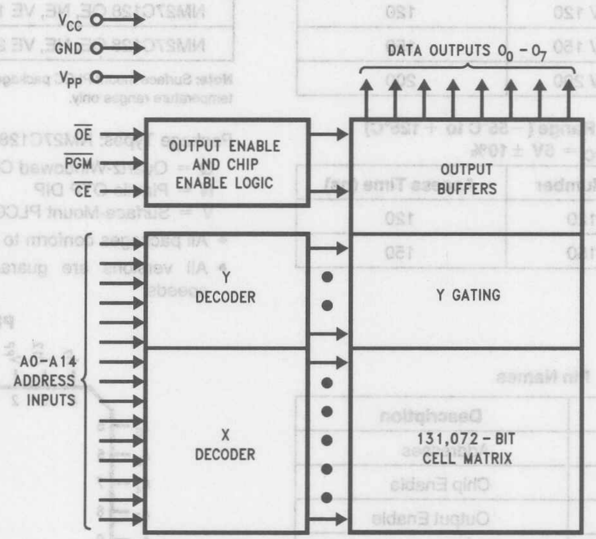
The NM27C128, is configured in the standard EPROM pin-out which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C128 is one member of a high density EPROM Family which range in densities up to 4 Mb.

Features

- High performance CMOS
  - 100 ns access time
- Fast turn-off for microprocessor compatibility
- JEDEC standard pin configuration
  - 28-pin DIP package
  - 32-pin chip carrier
- Drop-in replacement for 27C128 or 27128

Block Diagram



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Connection Diagrams

27C080	27C040	27C020	27C010	27C512	27C256
A19	V_{PP}	V_{PP}	V_{PP}		
A16	A16	A16	A16		
A15	A15	A15	A15	A15	V_{PP}
A12	A12	A12	A12	A12	A12
A7	A7	A7	A7	A7	A7
A6	A6	A6	A6	A6	A6
A5	A5	A5	A5	A5	A5
A4	A4	A4	A4	A4	A4
A3	A3	A3	A3	A3	A3
A2	A2	A2	A2	A2	A2
A1	A1	A1	A1	A1	A1
A0	A0	A0	A0	A0	A0
O0	O0	O0	O0	O0	O0
O1	O1	O1	O1	O1	O1
O2	O2	O2	O2	O2	O2
GND	GND	GND	GND	GND	GND

DIP
NM27C128

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27C256	27C512	27C010	27C020	27C040	27C080
		V_{CC}	V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A18	A18
V_{CC}	V_{CC}	XX	A17	A17	A17
A14	A14	A14	A14	A14	A14
A13	A13	A13	A13	A13	A13
A8	A8	A8	A8	A8	A8
A9	A9	A9	A9	A9	A9
A11	A11	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}/PGM$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/PGM$	$\overline{CE}/PGM$
O7	O7	O7	O7	O7	O7
O6	O6	O6	O6	O6	O6
O5	O5	O5	O5	O5	O5
O4	O4	O4	O4	O4	O4
O3	O3	O3	O3	O3	O3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C128 pins.

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C128 Q, N, V 100	100
NM27C128 Q, N, V 120	120
NM27C128 Q, N, V 150	150
NM27C128 Q, N, V 200	200

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C128 QE, NE, VE 120	120
NM27C128 QE, NE, VE 150	150
NM27C128 QE, NE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

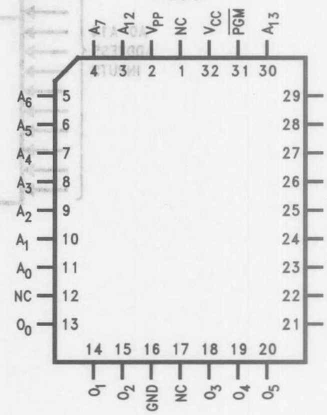
Military Temp. Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C128 QM 120	120
NM27C128 QM 150	150

Package Types: NM27C128 Q, N, V XXX
Q = Quartz-Windowed Ceramic DIP
N = Plastic OTP DIP
V = Surface-Mount PLCC

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

PLCC



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Pin Names

Symbol	Description
A0–A13	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	> 2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}
Comm'l	0°C to +70°C	+5V ±10%
Industrial	−40°C to +85°C	+5V ±10%
Military	−55°C to +125°C	+5V ±10%

Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA	3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V V_{IL} = GND ± 0.3V, V_{IH} = V_{CC} ±0.3V		100	μA
I_{SB2}	V_{CC} Standby Current (T^2L)	$\overline{CE}$ = V_{IH}		1	mA
I_{CC1}	V_{CC} Active Current, T^2L Inputs	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 5 MHz I/O = 0 mA		35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}		10	μA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	μA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

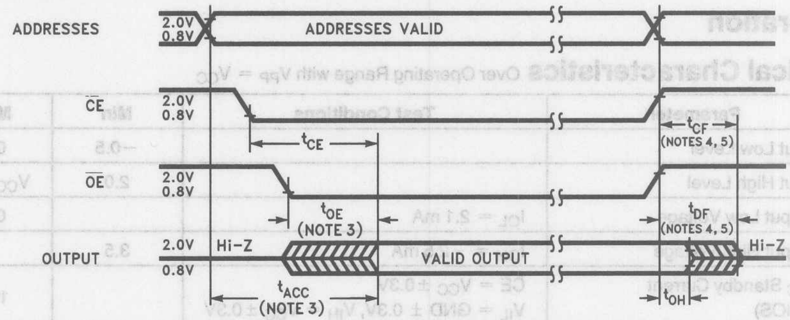
Symbol	Parameter	120		150		200		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	ns
t_{CF} (Note 2)	$\overline{CE}$ High to Output Float		30		45		55	ns
t_{DF} (Note 2)	$\overline{OE}$ High to Output Float		35		45		55	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		ns

C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	≤ 5 ns	Timing Measurement Reference Level	(Note 10)
		Inputs	0.8V and 2.0V
		Outputs	0.8V and 2.0V

AC Waveforms (Notes 6, 7 and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
$C_L = 100$ pF includes fixture capacitance.

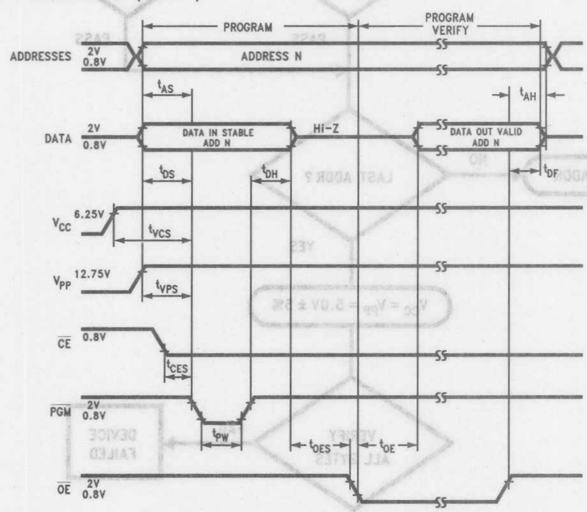
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

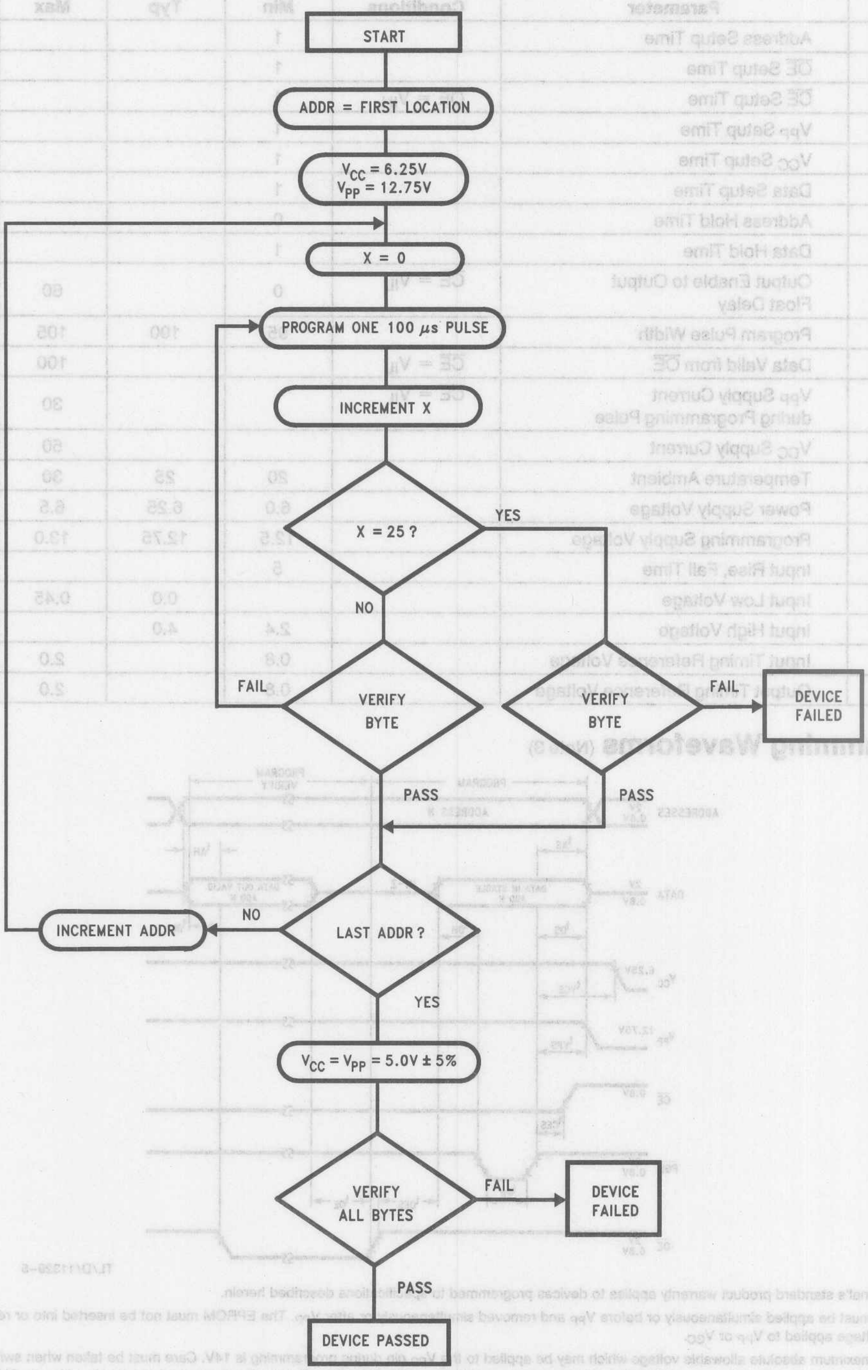
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart (Note 4)



TL/D/11329–6

FIGURE 1

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{\text{OE}}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{\text{CE}}$ be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$ be made a common connection to all devices in the array and connected to the deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V, $\overline{\text{CE}}$ is A7 V_{IL}, and $\overline{\text{OE}}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{\text{PGM}}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{\text{PGM}}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirments. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{PGM}}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{\text{CE}}$ all like inputs (including $\overline{\text{OE}}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{\text{CE}}$ input with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{\text{CE}}$ input inhibits the other EPROMs from being programmed.

verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacture and device type. The code for NM27C128 is "8F83", where "8F" designates that it is made by National Semiconductor, and "83" designates a 128K part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A13, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C to $\pm$5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wave-

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of NM27C128 listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	5.0V	D_{OUT}
Output Disable	X	V_{IH}	V_{IH}	V_{CC}	5.0V	High-Z
Standby	V_{IH}	X	X	V_{CC}	5.0V	High-Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High-Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	0	1	1	83

National Semiconductor

NM27C256
262,144-Bit (32K x 8) High Performance CMOS EPROM

General Description

The NM27C256 is a 256K Electrically Programmable Read Only Memory. It is manufactured in National's latest CMOS split gate EPROM technology which enables it to operate at speeds as fast as 120 ns access time over the full operating range.

The NM27C256 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 120 ns access time provides high speed operation with high-performance CPUs. The NM27C256 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

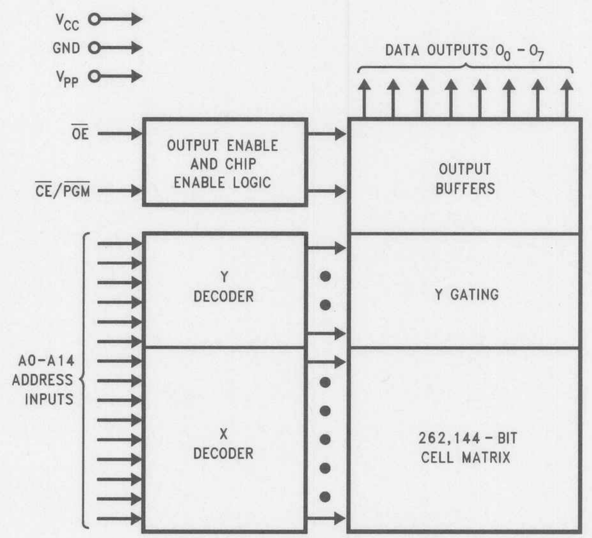
The NM27C256, is configured in the standard EPROM pin-out which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C256 is one member of a high density EPROM Family which range in densities up to 4 Mb.

Features

- High performance CMOS
  - 120 ns access time
- JEDEC standard pin configuration
  - 28-pin DIP package
  - 32-pin chip carrier
- Drop-in replacement for 27C256 or 27256
- Manufacturer's identification code

Block Diagram



TL/D/10833-1

Connection Diagrams

27C080	27C040	27C020	27C010	27C512
A19	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A16	A16	A16	A16	
A15	A15	A15	A15	A15
A12	A12	A12	A12	A12
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O0	O0	O0	O0	O0
O1	O1	O1	O1	O1
O2	O2	O2	O2	O2
GND	GND	GND	GND	GND

27C512	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/$\overline{PGM}$	XX/$\overline{PGM}$	A18	A18
V_{CC}	XX	A17	A17	A17
A14	A14	A14	A14	A14
A13	A13	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
A11	A11	A11	A11	A11
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O7	O7	O7	O7	O7
O6	O6	O6	O6	O6
O5	O5	O5	O5	O5
O4	O4	O4	O4	O4
O3	O3	O3	O3	O3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C256 pins.

Commercial Temp. Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 Q, N, V 120	120
NM27C256 Q, N, V 150	150
NM27C256 Q, N, V 200	200

Military Temp. Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 QM 150	150
NM27C256 QM 250	250

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C256 QE, NE, VE 120	120
NM27C256 QE, NE, VE 150	150
NM27C256 QE, NE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

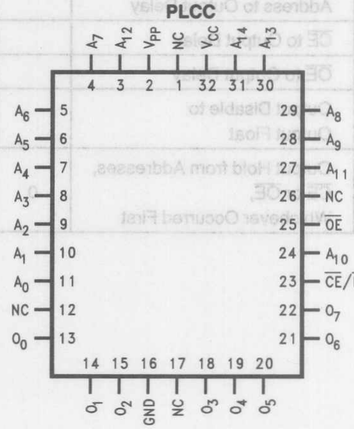
Package Types: NM27C256 Q, N, V XXX
- Q = Quartz-Windowed Ceramic DIP
- N = Plastic OTP DIP
- V = Surface-Mount PLCC

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Pin Names

Symbol	Description
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (during Read)

PLCC



Top

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Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V

Respect to Ground V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}
Comm'l	0°C to +70°C	+5V ±10%
Industrial	−40°C to +85°C	+5V ±10%
Military	−55°C to +125°C	+5V ±10%

Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA	3.5		V
I_{SB1} (Note 11)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V		100	µA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH}		1	mA
I_{CC1}	V_{CC} Active Current TTL Inputs	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}		10	µA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	µA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

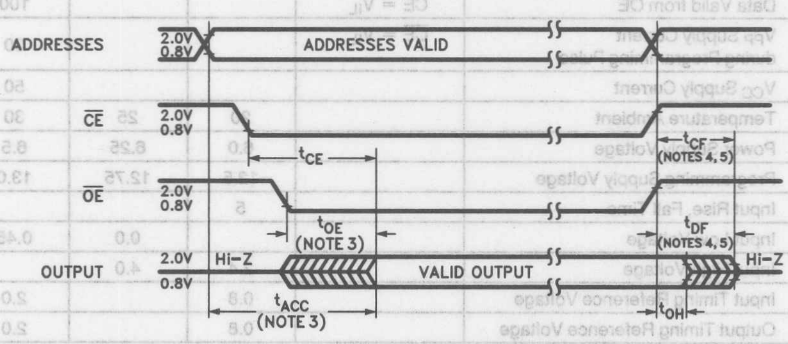
Symbol	Parameter	100		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50		50	ns
t_{DF} (Note 2)	Output Disable to Output Float		30		35		45		55	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		ns

C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Input Pulse Levels	0.45 to 2.4V
		Timing Measurement Reference Level	(Note 10)
Input Rise and Fall Times	≤ 5 ns	Inputs	0.8V and 2.0V
		Outputs	0.8V and 2.0V

AC Waveforms (Notes 6, 7 and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
$C_L = 100$ pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

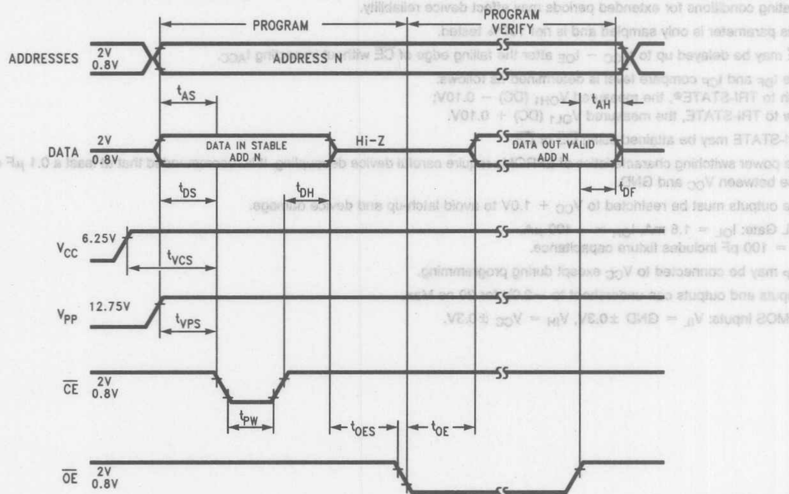
Note 11: CMOS inputs: V_{IL} = GND $\pm$0.3V, $V_{IH} = V_{CC}$ $\pm$0.3V.

3

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

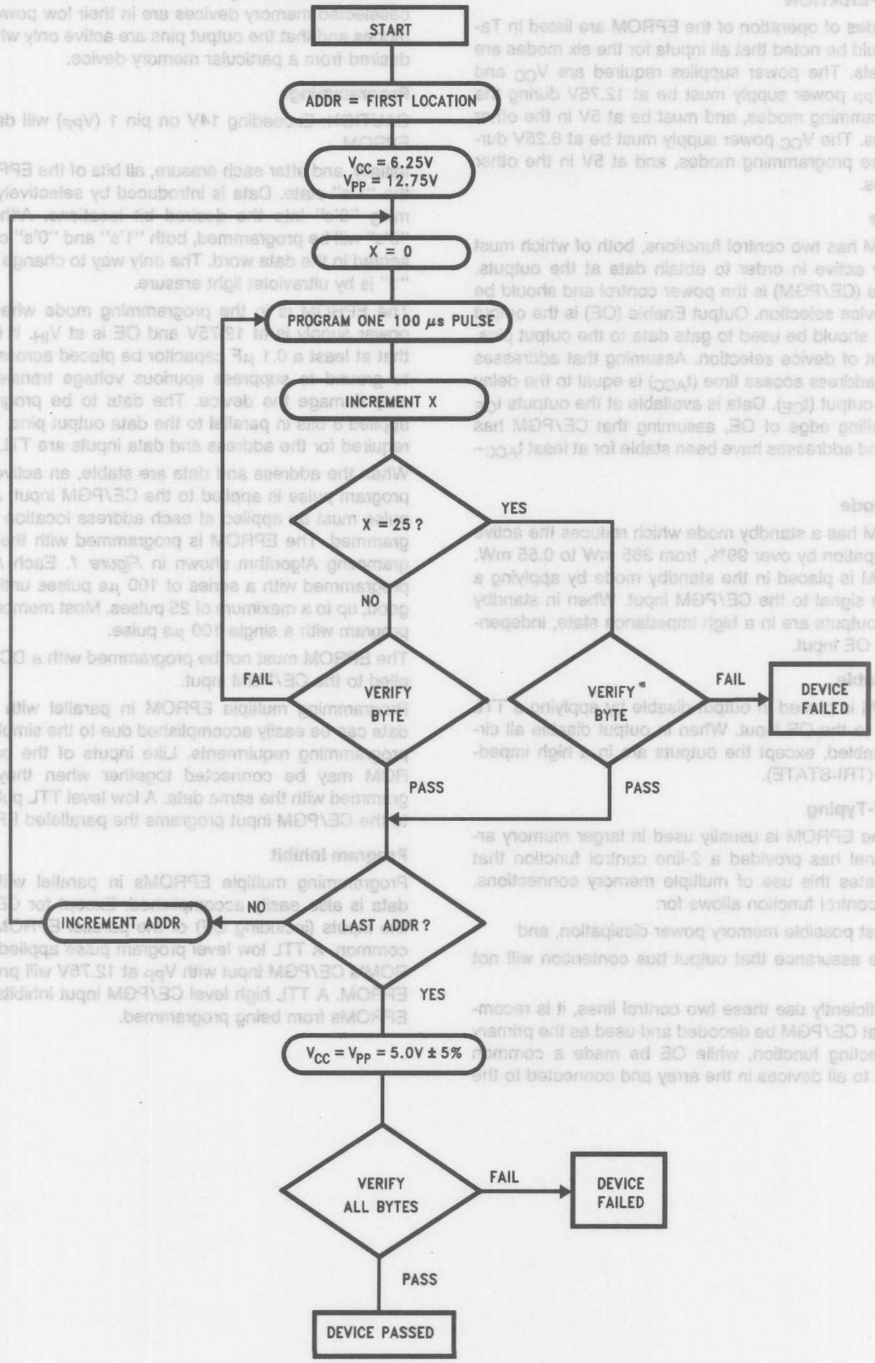
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/10833–6

FIGURE 1

at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE/PGM has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and OE is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirments. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM, all like inputs (including OE) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27C256 is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C to ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wave-

exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

3

Mode Selection

The modes of operation of NM27C256 listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Mode \ Pins	$\overline{CE}/PGM$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	V_{CC}	5.0V	High-Z
Standby	V_{IH}	X	V_{CC}	5.0V	High-Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High-Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	0	1	0	0	04

National Semiconductor

NM27C512
524,288-Bit (64K x 8) High Performance CMOS EPROM

General Description

The NM27C512 is a high performance 512K UV Erasable Electrically Programmable Read Only Memory (EPROM). It is manufactured using National's proprietary 0.8 micron CMOS AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability.

The NM27C512 provides microprocessor-based systems storage capacity for portions of operating system and application software. Its 90 ns access time provides no-wait-state operation with high-performance CPUs. The NM27C512 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

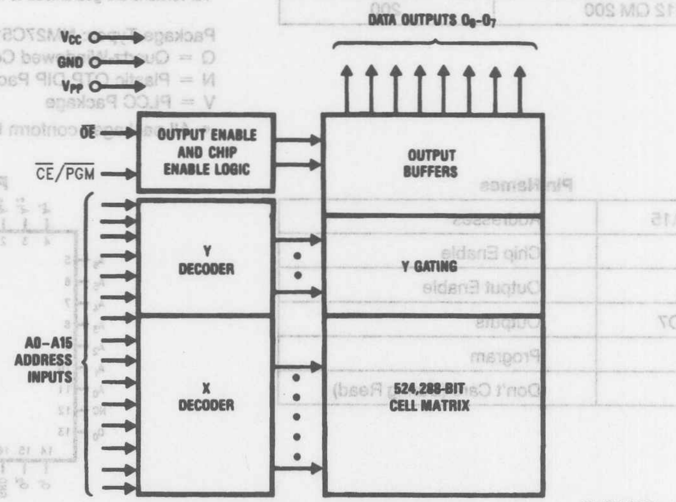
The NM27C512 is configured in the standard JEDEC EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs.

The NM27C512 is one member of a high density EPROM Family which range in densities up to 4 Megabit.

Features

- High performance CMOS
  - 90 ns access time
- Fast turn-off for microprocessor compatibility
- Manufacturers identification code
- JEDEC standard pin configuration
  - 28-pin DIP package
  - 32-pin chip carrier

Block Diagram



TL/D/10834–1

Connection Diagrams

27C080	27C040	27C020	27C010	27C256
A_{19}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	
A_{16}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

DIP
NM27C512

TL/D/10834-2

27C256	27C010	27C020	27C040	27C080
	V_{CC}	V_{CC}	V_{CC}	V_{CC}
	XX/$\overline{PGM}$	XX/$\overline{PGM}$	A_{18}	A_{18}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}/PGM$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C512 pins.

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Access Time (ns)*
NM27C512 Q, N, V 90	90
NM27C512 Q, N, V 120	120
NM27C512 Q, N, V 150	150
NM27C512 Q, N, V 200	200

Extended Temp Range (−40°C to +85°C)

Parameter/Order Number	Access Time (ns)*
NM27C512 QE, NE, VE 90	90
NM27C512 QE, NE, VE 120	120
NM27C512 QE, NE, VE 150	150
NM27C512 QE, NE, VE 200	200

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Access Time (ns)*
NM27C512 QM 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

*All versions are guaranteed to function for slower speeds.

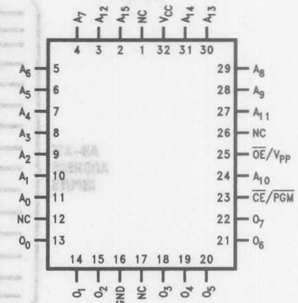
Package Types: NM27C512 Q, N, V XXX
Q = Quartz-Windowed Ceramic DIP Package
N = Plastic OTP DIP Package
V = PLCC Package

- All packages conform to the JEDEC standard.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

PLCC



TL/D/10834-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages Except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection (MIL Std. 883, Method 3015.2)	>2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Comm'l	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	08	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V			100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	f = 5 MHz		40	mA
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA C, I Temp Ranges			35	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			10	μA
V_{PP}	V_{PP} Read Voltage			V_C − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Electrical Characteristics

Symbol	Parameter	90		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		40		50		50		50	ns
t_{DF}	Output Disable to Output Float		35		25		45		55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0				ns

Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	20	25	pF

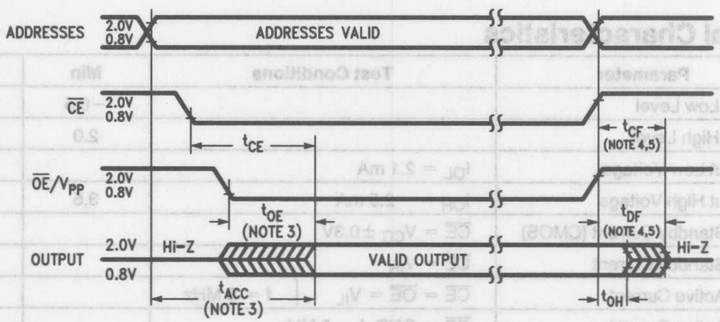
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level (Note 9)

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7)



TL/D/10834-4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

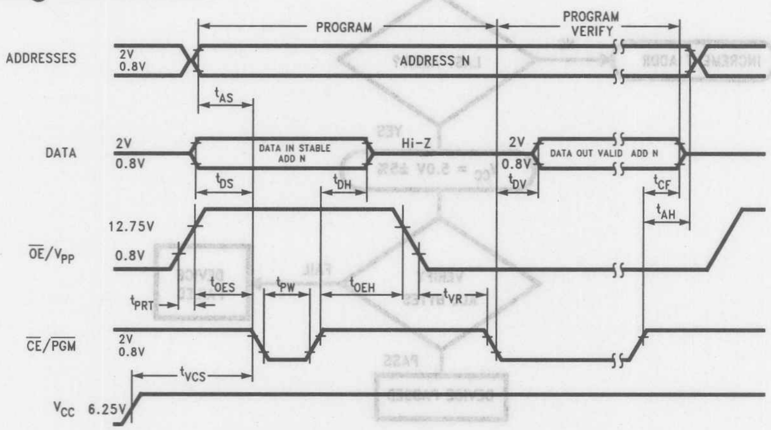
Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

t_{OES}	OE Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OEH}	$\overline{OE}$ Hold Time		1			µs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			µs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing Reference Voltage		0.8		2	V

Programming Waveforms



TL/D/10834–5

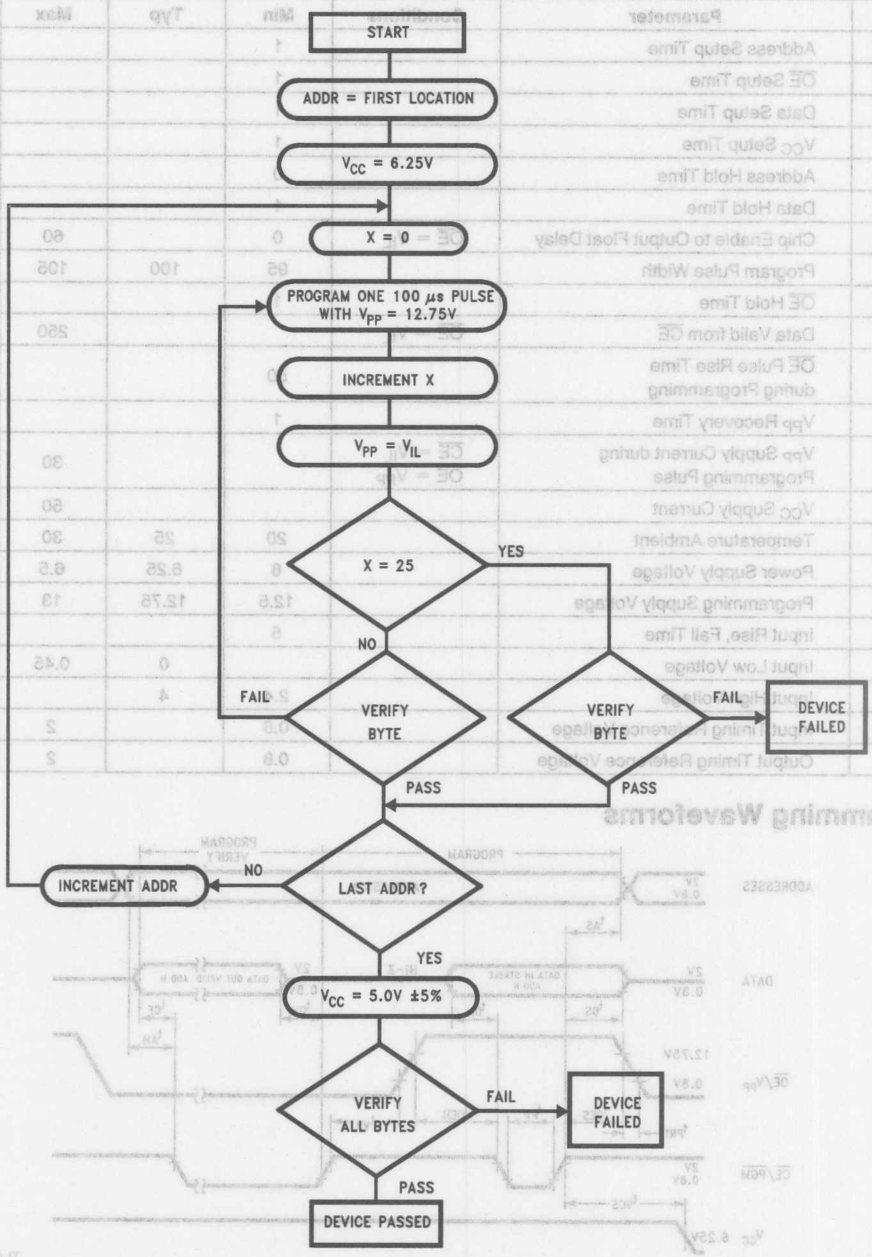
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart



TL/D/10834–6

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and OE/V_{PP}. The OE/V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE/V_{PP}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE/V_{PP} be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 (OE/V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the OE/V_{PP} is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed.

The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM all like inputs (including OE/V_{PP}) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with OE/V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with OE/V_{PP} and CE at V_{IL}. Data should be verified T_{DV} after the falling edge of CE.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27C512 is "8F85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512K part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins

Functional Description (Continued)

are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27C512 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels excepts for V_{PP} and A9 for device signature.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$/PGM	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	5.0V	High Z
Standby	V_{IH}	X	5.0V	High Z
Programming	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	0	1	85

National Semiconductor

NM27C010
1,048,576-Bit (128K x 8) High Performance CMOS EPROM

General Description

The NM27C010 is a high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 128K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature during read operations allows memory expansions from 1M to 8M bits with no printed circuit board changes.

The NM27C010 can directly replace lower density 28-pin EPROMs by adding an A16 address line and V_{CC} jumper. During the normal read operation PGM and V_{PP} are in a "Don't Care" state which allows higher order addresses, such as A17, A18, and A19 to be connected without affecting the normal read operation. This allows memory upgrades to 8M bits without hardware changes. The NM27C010 is also offered in a 32-pin plastic DIP with the same upgrade path.

The NM27C010 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 90 ns access time provides no-wait-state operation with high-performance CPUs. The NM27C010 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

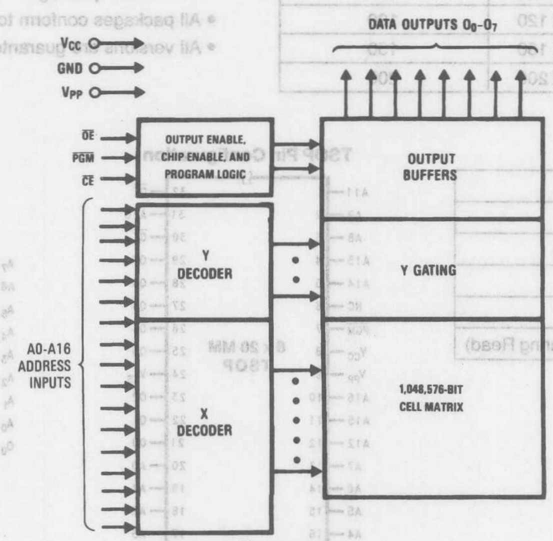
The NM27C010 is manufactured using National's advanced CMOS AMG™ EPROM technology.

The NM27C010 is one member of a high density EPROM Family which range in densities up to 4 Megabit.

Features

- High performance CMOS
  - — 90 ns access time
- Fast turn-off for microprocessor compatibility
- Simplified upgrade path
  - — V_{PP} and PGM are "Don't Care" during normal read operation
- Manufacturers identification code
- Fast programming
- JEDEC standard pin configurations
  - — 32-pin DIP package
  - — 32-pin PLCC package
  - — 32-pin TSOP package

Block Diagram



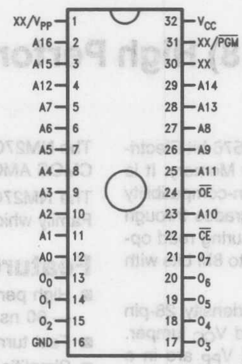
TL/D/10798-1

Connection Diagrams

DIP PIN CONFIGURATIONS

27C080	27C040	27C020	27C512	27C256
A19	XX/V_{PP}	XX/V_{PP}		
A16	A16	A16		
A15	A15	A15	A15	V_{PP}
A12	A12	A12	A12	A12
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

DIP
NM27C010



27C256	27C512	27C020	27C040	27C080
		V_{CC}	V_{CC}	V_{CC}
		XX/PGM	A18	A18
V_{CC}	V_{CC}	A17	A17	A17
A14	A14	A14	A14	A14
A13	A13	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
A11	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10	A10	A10
$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C010 pins.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C010 Q, V, N, T 90	90
NM27C010 Q, V, N, T 120	120
NM27C010 Q, V, N, T 150	150
NM27C010 Q, V, N, T 200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C010 QE, VE, NE 100	100
NM27C010 QE, VE, NE 120	120
NM27C010 QE, VE, NE 150	150
NM27C010 QE, VE, NE 200	200

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C010 QM 150	150
NM27C010 QM 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

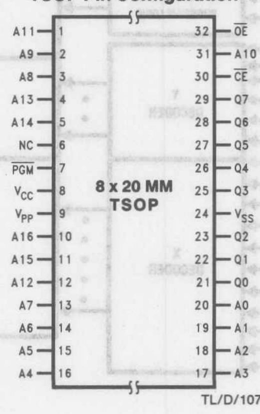
Package Types: NM27C010 Q, N, V XXX
Q = Quartz-Windowed Ceramic DIP package
V = PLCC package
N = Plastic DIP package
T = TSOP package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function at slower speeds.

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

TSOP Pin Configuration



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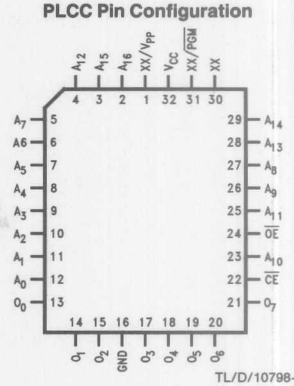
PLCC Pin Configuration



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages Except A_9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A_9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND −0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	μA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$ I/O = 0 mA	f = 5 MHz		30	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5 or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

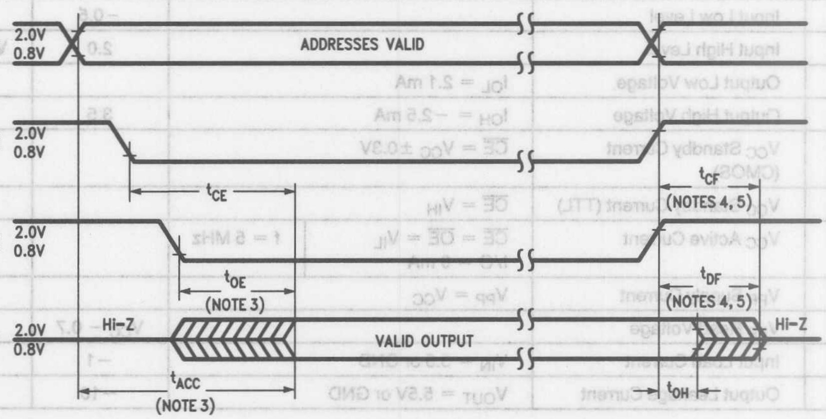
Symbol	Parameter	90		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		40		50		50		50	ns
t_{DF} (Note 2)	Output Disable to Output Float		35		35		45		55	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		ns

C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	10	15	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6, 7, & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ µA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

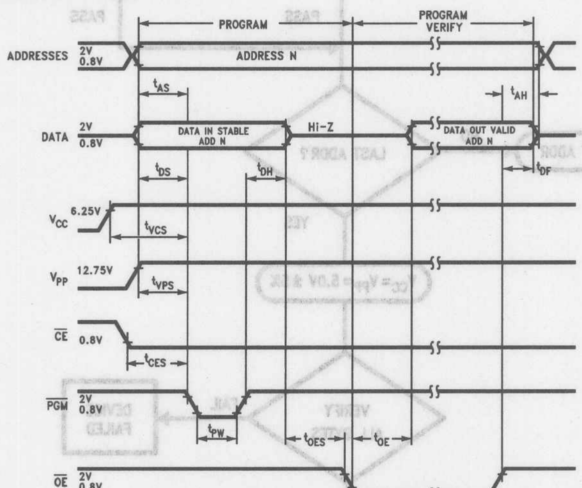
Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

3

Programming Characteristics (Notes 1, 2, 3, 4, & 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	μs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			15	mA
I_{CC}	V_{CC} Supply Current				20	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



TL/D/10798-5

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

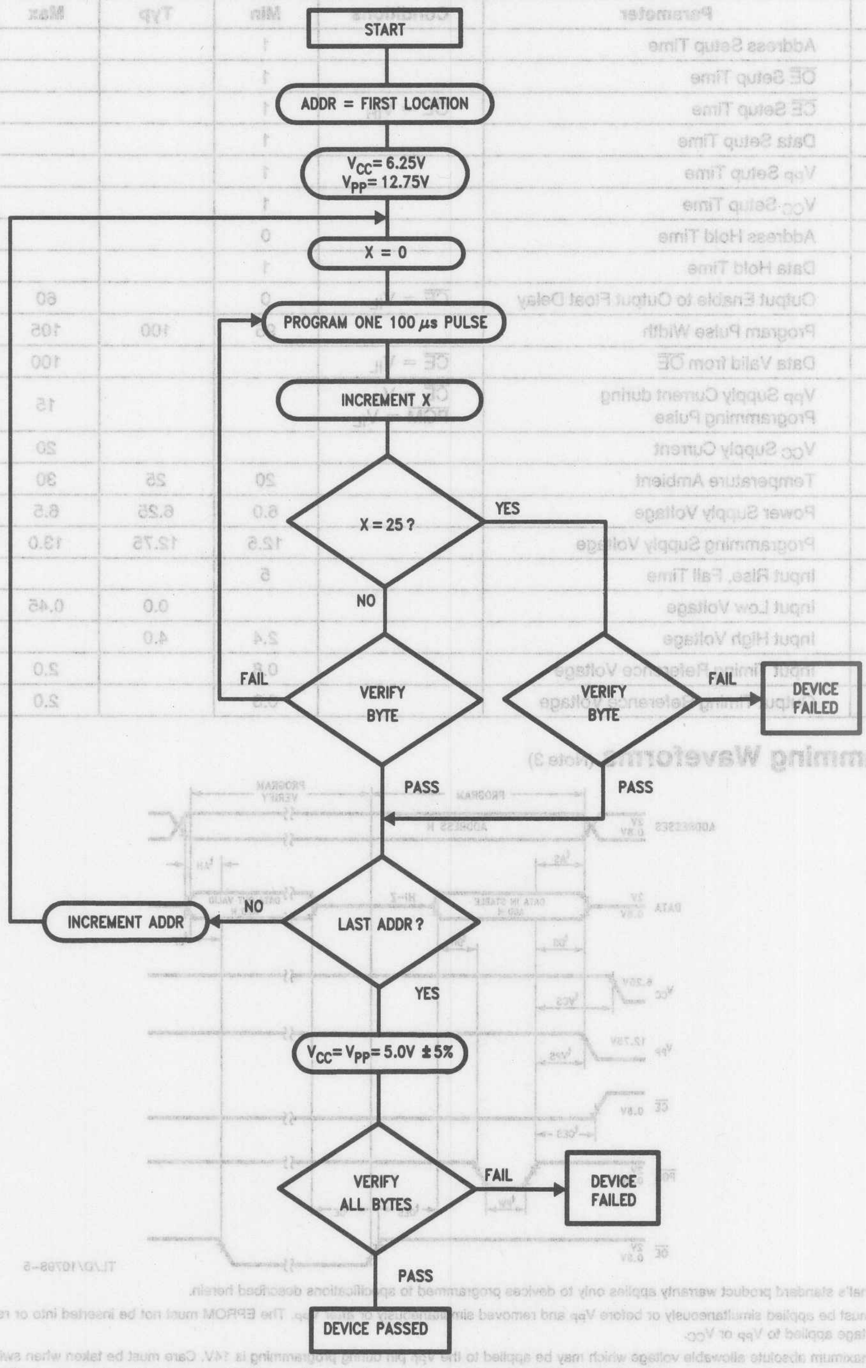
Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

3

Fast Programming Algorithm Flow Chart (Same as NMC27C010)



TL/D/10798-6

FIGURE 1

at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 165 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's indentification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27C010 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1 Megabit (128K $\times$ 8) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0–07. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

3

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp. (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27C010 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O_7 (21)	O_6 (20)	O_5 (19)	O_4 (18)	O_3 (17)	O_2 (15)	O_1 (14)	O_0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	1	0	86

National Semiconductor

NM27C210

1,048,576-Bit (64K x 16) High Performance CMOS EPROM

General Description

The NM27C210 is a high performance Electrically Programmable UV erasable ROM (EPROM). It contains 1,048,576 bits configured as 64K x 16 bit. It is offered in both erasable versions for prototyping and early production applications as well as non-erasable, plastic packaged versions that are ideal for high volume and automated assembly applications.

The NM27C210 operates from a single 5 volt ±10% supply in the read mode.

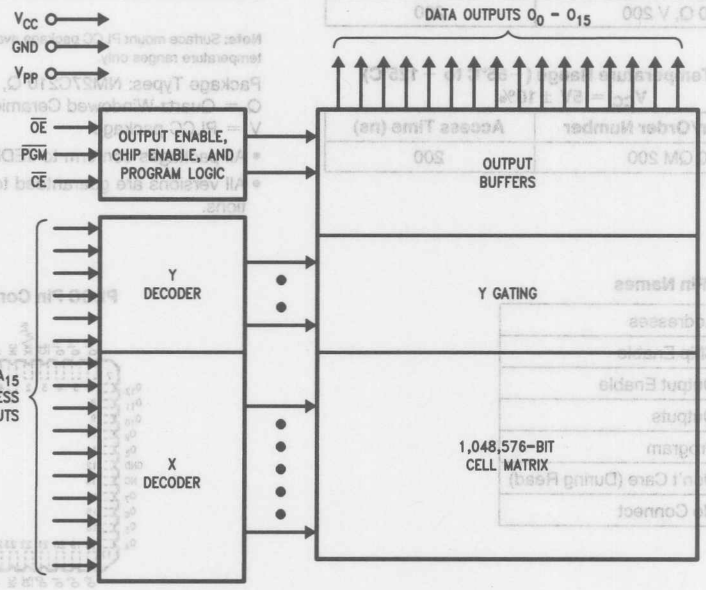
The NM27C210 is offered in both DIP and surface mount packages. The DIP package is a 40-pin dual-in-line ceramic with a quartz window to allow erasing. The surface mount package is a 44-pin PLCC that is offered in OTP.

This EPROM is manufactured using National's proprietary 0.8 micron CMOS AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability.

Features

- High performance CMOS
  - — 90 ns access time
- Fast turn-off for microprocessor compatibility
- Simplified upgrade path
  - — V_{PP} and PGM are "Don't Care" during normal read operation
- Compatible with 27210 and 27C210 EPROMs
- Manufacturer's identification code
- Fast programming
- JEDEC standard pin configuration
  - — 40-pin CDIP package
  - — 44-pin PLCC package

Block Diagram



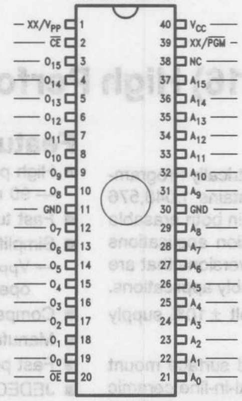
TL/D/11093–1

Connection Diagrams

DIP PIN CONFIGURATIONS

27C280	27C240	27C220
A_{18}	XX/V_{PP}	XX/V_{PP}
$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_{15}	O_{15}	O_{15}
O_{14}	O_{14}	O_{14}
O_{13}	O_{13}	O_{13}
O_{12}	O_{12}	O_{12}
O_{11}	O_{11}	O_{11}
O_{10}	O_{10}	O_{10}
O_9	O_9	O_9
O_8	O_8	O_8
GND	GND	GND
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3
O_2	O_2	O_2
O_1	O_1	O_1
O_0	O_0	O_0
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$

DIP
NM27C210



27C220	27C240	27C280
V_{CC}	V_{CC}	V_{CC}
$XX/\overline{PGM}$	A_{17}	A_{17}
A_{16}	A_{16}	A_{16}
A_{15}	A_{15}	A_{15}
A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}
A_{12}	A_{12}	A_{12}
A_{11}	A_{11}	A_{11}
A_{10}	A_{10}	A_{10}
A_9	A_9	A_9
GND	GND	GND
A_8	A_8	A_8
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C210 pins.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 Q, V 90	90
NM27C210 Q, V 120	120
NM27C210 Q, V 150	150
NM27C210 Q, V 200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 QE, VE 120	120
NM27C210 QE, VE 150	150
NM27C210 QE, VE 200	200

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C210 QM 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

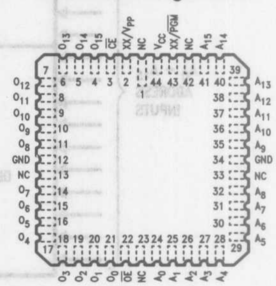
Package Types: NM27C210 Q, V XXX
Q = Quartz-Windowed Ceramic DIP package
V = PLCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
NC	No Connect

PLCC Pin Configuration



TL/D/11093-3

Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC}$ ±0.3V			100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA	f = 5 MHz		40	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
I_{LI}	Input Load Current	V_{IN} = 5.5 or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	90		120		150		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		90		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50		50	ns
t_{DF} (Note 2)	Output Disable to Output Float		30		35		45		55	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		ns

3

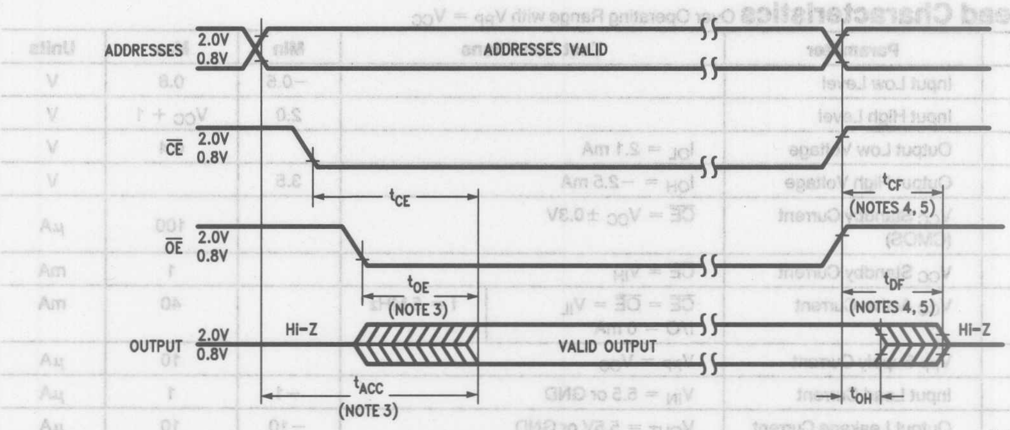
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	12	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, & 9)



TL/D/11093–4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

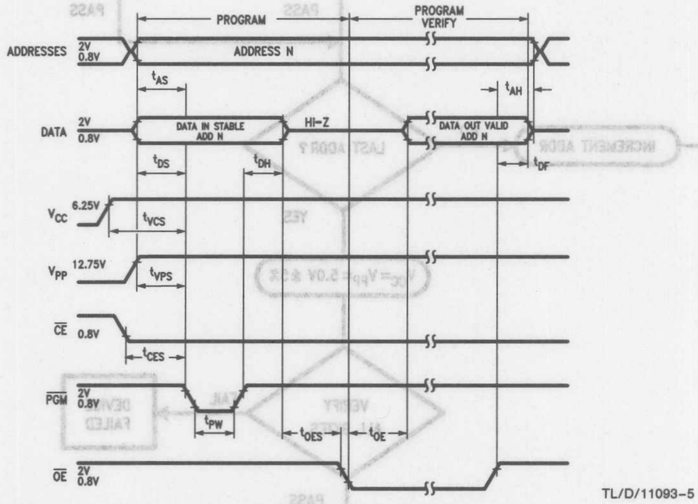
Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



TL/D/11093-5

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart

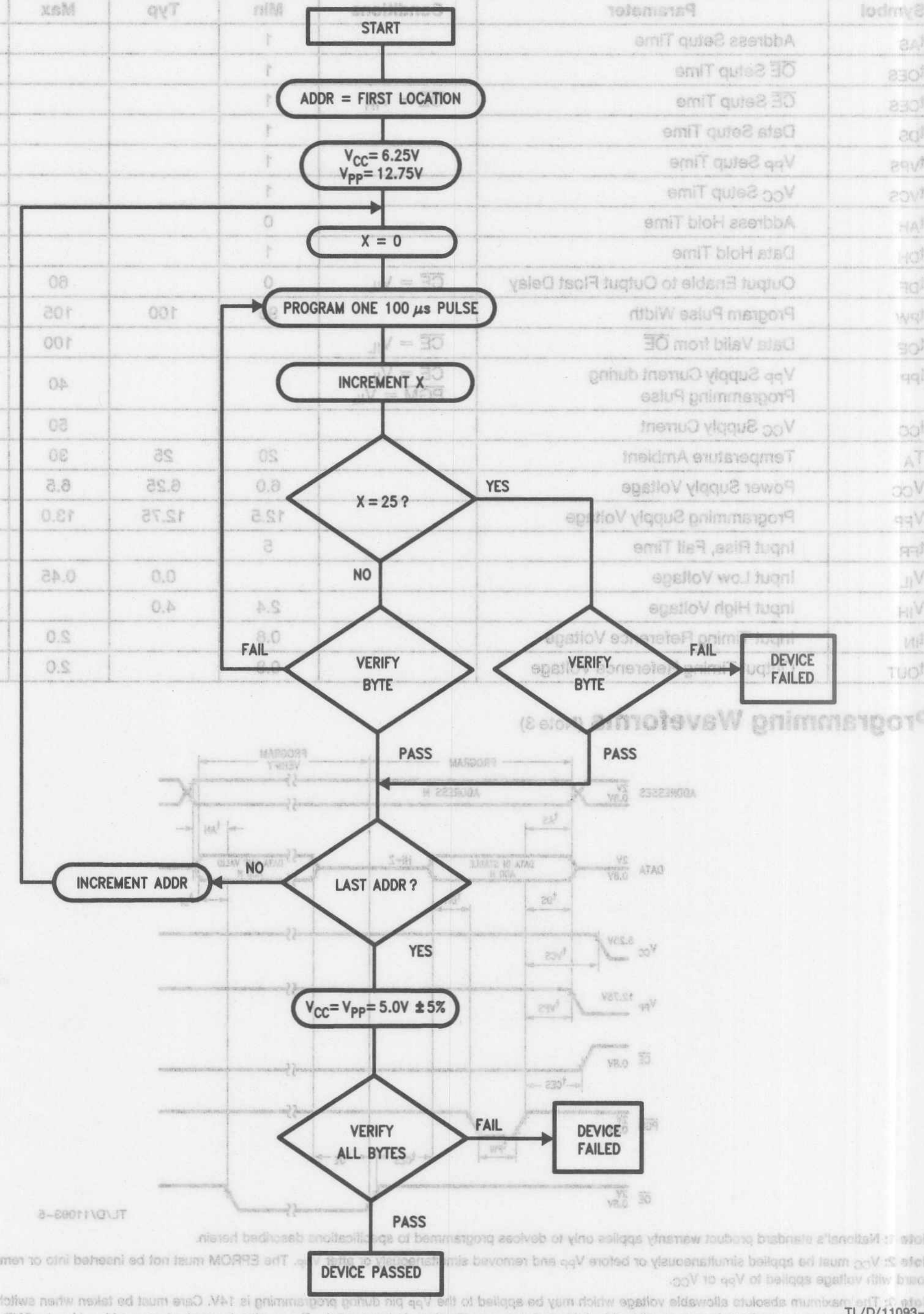


FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 275 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Functional Description (Continued)

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27C210 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A_9. Addresses A_1–A_8, A_{10}–A_{15}, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

MODE SELECTION

The modes of operation of the NM27C210 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

National Semiconductor

PRELIMINARY

NM27C020
2,097,152-Bit (256K x 8) UV Erasable CMOS EPROM

General Description

The NM27C020 is a high performance 2,097,152-bit EPROM. It is organized as 256 K-words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature during read operations enables memory expansions up to 8 Mbits with no printed circuit board changes.

The NM27C020 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 100 ns access time provides no-wait-state operation with high-performance CPUs. The NM27C020 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently-used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

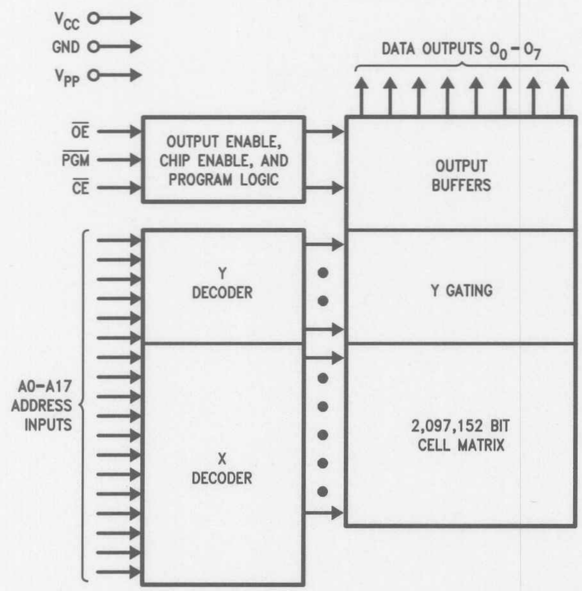
The NM27C020, is manufactured using National's advanced CMOS AMG™ EPROM technology.

The NM27C020 is one member of a high density National EPROM series which range in densities up to 4 Mb.

Features

- High performance CMOS
  - 100 ns access time
- Simplified upgrade path
  - V_{PP} and PGM are "Don't Care" during normal read operation
- JEDEC standard pin configuration
- Manufacturer's identification code
- JEDEC standard pin configuration
  - 32-pin DIP
  - 32-pin PLCC

Block Diagram



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Pin Names

Symbol	Description
A0–A17	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

Connection Diagrams

DIP Pin Configuration

8 Mbit	4 Mbit	1 Mbit	27C512	27C256	NM27C020	Pin	Pin	NM27C020	27C256	27C512	27C010	27C040	27C080
A19	XX/V_{PP}	XX/V_{PP}			XX/V_{PP}	1	32	V_{CC}			V_{CC}	V_{CC}	V_{CC}
A16	A16	A16			A16	2	31	XX/$\overline{PGM}$			XX/$\overline{PGM}$	A18	A18
A15	A15	A15	A15	V_{PP}	A15	3	30	A17	V_{CC}	V_{CC}	XX	A17	A17
A12	A12	A12	A12	A12	A12	4	29	A14	A14	A14	A14	A14	A14
A7	A7	A7	A7	A7	A7	5	28	A13	A13	A13	A13	A13	A13
A6	A6	A6	A6	A6	A6	6	27	A8	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	A5	7	26	A9	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	A4	8	25	A11	A11	A11	A11	A11	A11
A3	A3	A3	A3	A3	A3	9	24	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/V_{PP}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/V_{PP}
A2	A2	A2	A2	A2	A2	10	23	A10	A10	A10	A10	A10	A10
A1	A1	A1	A1	A1	A1	11	22	$\overline{CE}$	$\overline{CE}$/PGM	$\overline{CE}$/PGM	$\overline{CE}$	$\overline{CE}$/PGM	$\overline{CE}$/PGM
A0	A0	A0	A0	A0	A0	12	21	O_7	O_7	O_7	O_7	O_7	O_7
O_0	O_0	O_0	O_0	O_0	O_0	13	20	O_6	O_6	O_6	O_6	O_6	O_6
O_1	O_1	O_1	O_1	O_1	O_1	14	19	O_5	O_5	O_5	O_5	O_5	O_5
O_2	O_2	O_2	O_2	O_2	O_2	15	18	O_4	O_4	O_4	O_4	O_4	O_4
GND	GND	GND	GND	GND	GND	16	17	O_3	O_3	O_3	O_3	O_3	O_3

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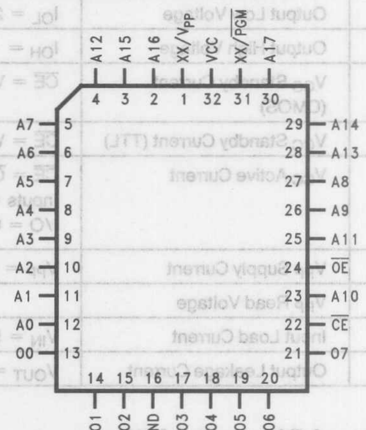
Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C020 pins.

PLCC Pin Configuration



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Commercial Temp. Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C020 Q, V 100	100
NM27C020 Q, V 120	120
NM27C020 Q, V 150	150
NM27C020 Q, V 200	200

Extended Temp. Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C020 QE, VE 100	100
NM27C020 QE, VE 150	150
NM27C020 QE, VE 200	200

Packages Types: NM27C020 Q, V
Q = Ceramic DIP
V = PLCC

Ordering Information

NM 27 C 020 Q E 150

- **National Memory** — NM
- **EPROM** — 27
- **CMOS** — C
- **Size** — 020 = 2 Mbit
- **Package** — Q = Ceramic Dip; V = PLCC
- **Operating Temperature Range** — Blank = Commercial; E = Extended
- **Access Time** — 150 = 150 ns

Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection (MIL Std. 883C, Method 3015.2)	> 2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

Operating Range

Range	Temperature	V_{CC}	Tolerance
Comm'l	0°C to +70°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%

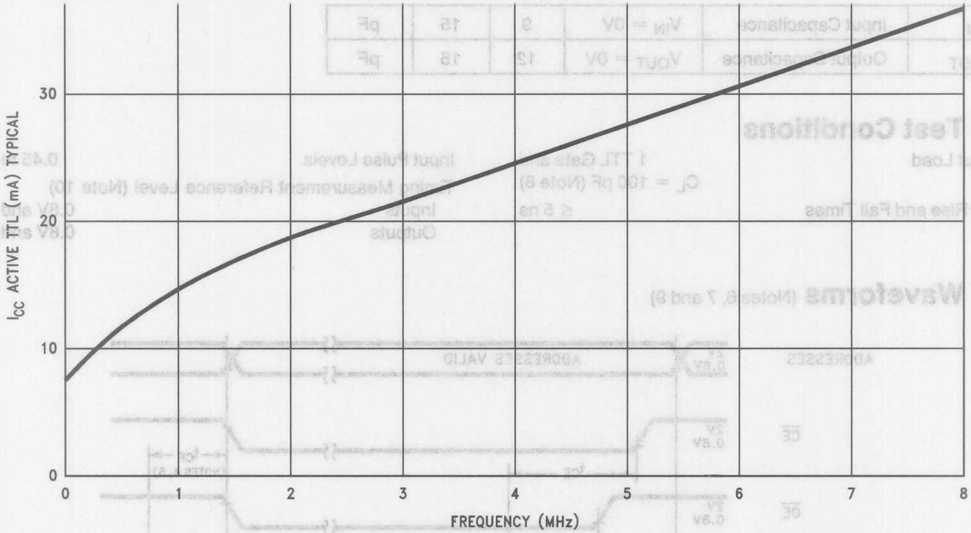
DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA		3.5		V
I_{SB1} (Note 3)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V			100	μA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}* (Note 1)	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL} Inputs = V_{IH} or V_{IL} I/O = 0 mA, f = 5 MHz	Commercial		30	mA
			Industrial		30	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	150		200		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50	ns
t_{DF} (Note 2)	Output Disable to Output Float		45		55	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		ns

* See attached I_{CC} vs Frequency Graphs.



TL/D/10835-7

FIGURE 1

I_{CC} vs Temperature

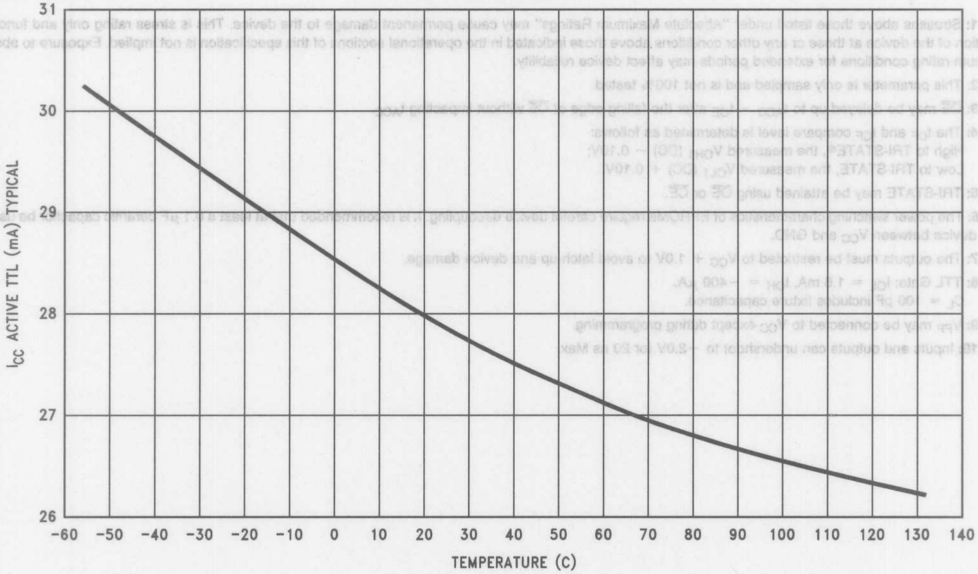


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FIGURE 2

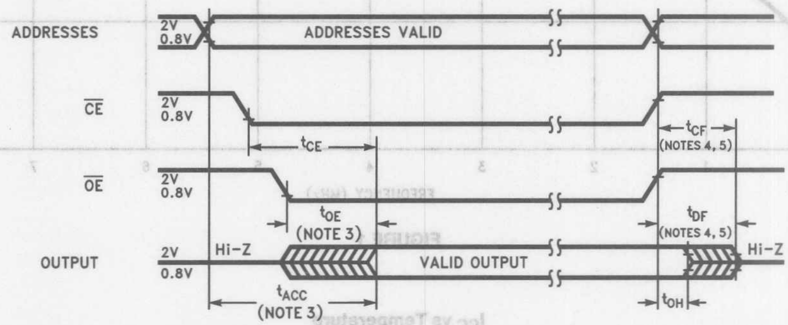
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Input Pulse Levels	0.45 to 2.4V
Input Rise and Fall Times	≤ 5 ns	Timing Measurement Reference Level (Note 10)	
		Inputs	0.8V and 2.0V
		Outputs	0.8V and 2.0V

AC Waveforms (Notes 6, 7 and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
$C_L = 100$ pF includes fixture capacitance.

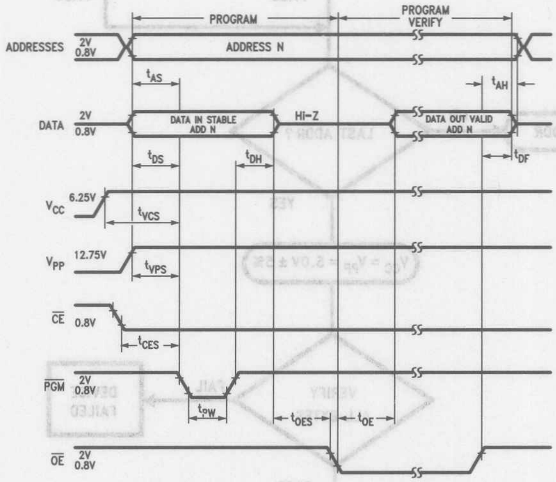
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$OE = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IL}$			15	mA
I_{CC}	V_{CC} Supply Current				20	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



TL/D/10835–5

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

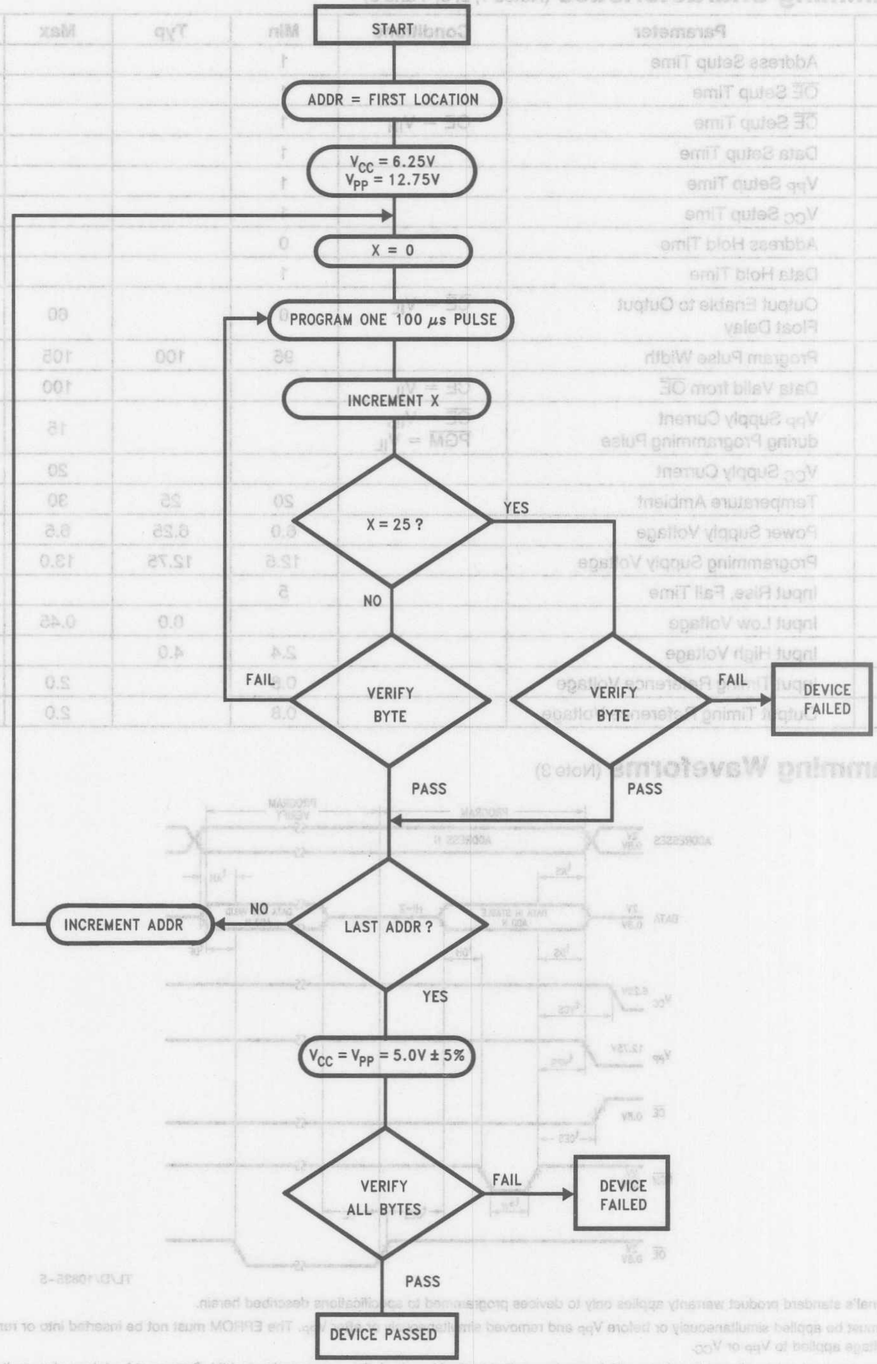
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings. The Min and Max limit parameters are design parameters, not tested or guaranteed.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/10835–6

FIGURE 3

Functional Description

DEVICE OPERATION

The six modes of operation of the device are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The part has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The device has a standby mode which reduces the active power dissipation by over 99%, from 220 mW to 0.55 mW. The device is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because the part is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a. the lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the device.

Initially, and after each erasure, all bits of the device are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The part is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

Mode Selection

The modes of operation of NM27C020 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Mode Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High-Z
Standby	V_{IH}	X	X	X	5.0V	High-Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High-Z

Note 1: X can be V_{IL} or V_{IH}.

Functional Description (Continued)

Manufacturer's Identification Code

The part has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for the NM27C020 is "8F07", where "8F" designates that it is made by National Semiconductor, and "07" designates a 2 Megabit byte-wide part.

The code is accessed by applying 12.0V $\pm$0.5V to address pin A9. All address and control pins are held at V_{IL}, except A0. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} from the device code. The code is read on the eight data pins, O0–O7. Proper code access is only guaranteed at 25°C $\pm$5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the device window to prevent unintentional erasure. Covering the window will also prevent temporary functional failures due to the generation of photo currents.

The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The device should be placed within 1 inch of the lamp tubes during erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer. The standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	0	1	1	1	07

National Semiconductor

NM27C040

4,194,304-Bit (512K x 8) High Performance CMOS EPROM

General Description

The NM27C040 is a high performance, 4,194,304-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 512K words of 8 bits each. Its pin-compatibility with byte-wide JEDEC EPROMs enables upgrades through 8 Mbit EPROMs. The "Don't Care" feature on V_{PP} during read operations allows memory expansions from 1M to 8 Mbits with no printed circuit board changes.

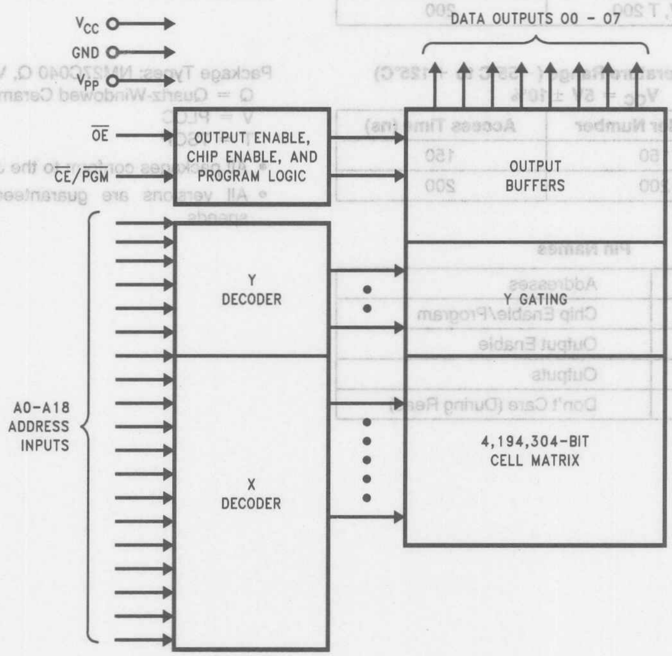
The NM27C040 provides microprocessor-based systems extensive storage capacity for large portions of operating system and application software. Its 120 ns access time provides high speed operation with high-performance CPUs. The NM27C040 offers a single chip solution for the code storage requirements of 100% firmware-based equipment. Frequently used software routines are quickly executed from EPROM storage, greatly enhancing system utility.

The NM27C040 is manufactured using National's advanced CMOS AMG™ EPROM technology.

Features

- High performance CMOS
  — 120 ns access time
- Simplified upgrade path
  — V_{PP} is a "Don't Care" during normal read operation
- Manufacturer's identification code
- JEDEC standard pin configuration
  — 32-pin DIP
  — 32-pin PLCC
  — 32-pin TSOP

Block Diagram



TL/D/10836-1

Connection Diagrams

27C080	27C020	27C010
A19	XX/V_{PP}	XX/V_{PP}
A16	A16	A16
A15	A15	A15
A12	A12	A12
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND

DIP
NM27C040

TL/D/10836–2

27C010	27C020	27C080
V_{CC}	V_{CC}	V_{CC}
XX/PGM	XX/PGM	A18
XX	A17	A17
A14	A14	A14
A13	A13	A13
A8	A8	A8
A9	A9	A9
A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE/PGM}$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C040 pin.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C040 Q, V, T 120	120
NM27C040 Q, V, T 150	150
NM27C040 Q, V, T 170	170
NM27C040 Q, V, T 200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C040 QE, VE, TE 150	150
NM27C040 QE, VE, TE 170	170
NM27C040 QE, VE, TE 200	200

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C040 QM 150	150
NM27C040 QM 200	200

Package Types: NM27C040 Q, V, T XXX
Q = Quartz-Windowed Ceramic DIP
V = PLCC
T = TSOP

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Pin Names

A0–A18	Addresses
$\overline{CE}/\overline{PGM}$	Chip Enable/Program
$\overline{OE}$	Output Enable
O0–O7	Outputs
XX	Don't Care (During Read)

Military	−55°C to +125°C	+5V	±10%

All Input Voltages except A9 with Respect to Ground: −0.6V to +7V

V_{PP} and A9 with Respect to Ground: −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground: −0.6V to +7V

ESD Protection: >2000V

All Output Voltages with Respect to Ground: V_{CC} +10V to GND −0.6V

Read Operation

DC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA	f = 5 MHz		30	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	120		150		170		200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		170		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		170		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50		50	ns
t_{DF} (Note 2)	Output Disable to Output Float		35		35		45		55	ns
t_{OH} (Note 2)	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		ns

3

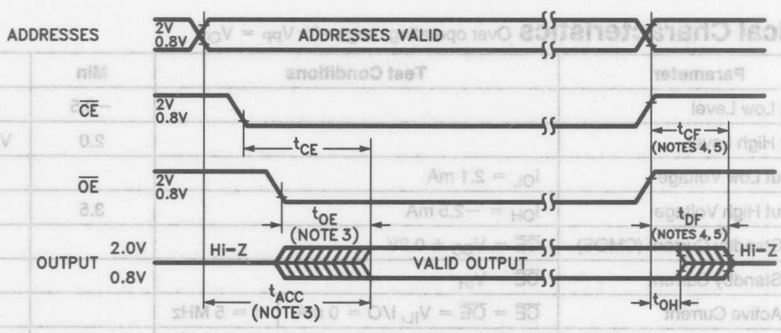
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level (Note 10)	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, and 9)



TL/D/10836-4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

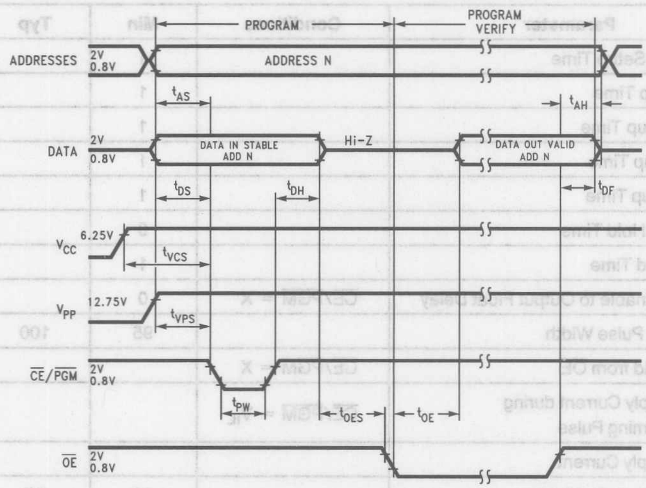
Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Waveform (Note 3)



TL/D/10836–5

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = X$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = X$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				30	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage		−0.1	0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

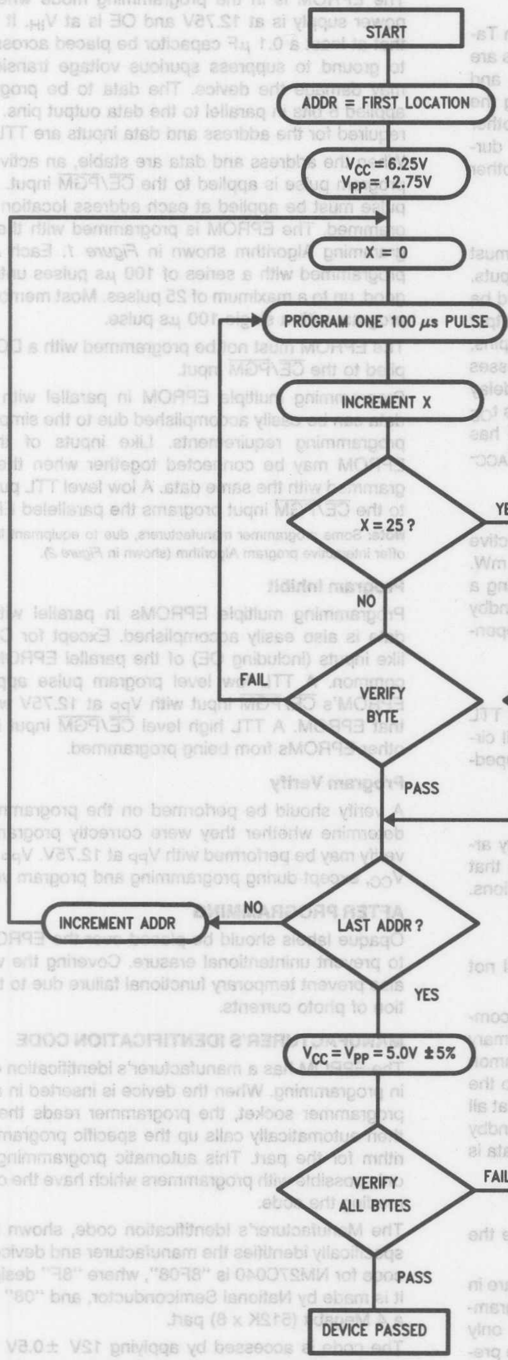
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Progam Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/10836–6

FIGURE 1

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that $\overline{CE}/\overline{PGM}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from of 65 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}/\overline{PGM}$ input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}/\overline{PGM}$ be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}/\overline{PGM}$ input programs the paralleled EPROM.

Note: Some programmer manufacturers, due to equipment limitation, may offer interactive program Algorithm (shown in *Figure 2*).

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM all like inputs (including OE) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}/\overline{PGM}$ input with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}/\overline{PGM}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27C040 is "8F08", where "8F" designates that it is made by National Semiconductor, and "08" designates a 4 Megabit (512K x 8) part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A18, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manu-

Functional Description (Continued)

facturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp. (If distance is doubled the erasure time increases by factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27C040 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	5.0V	High Z
Standby	V_{IH}	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_H

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	1	0	0	0	08

National Semiconductor

PRELIMINARY

NM27C240
4,194,304-Bit (256k x 16) High Performance CMOS EPROM

General Description

The NM27C240 is a high performance Electrically Programmable UV erasable ROM (EPROM). It contains 4,194,304 bits configured as 256k x 16 bits. It is offered in both erasable versions for prototyping and early production applications as well as non-erasable, plastic packaged versions that are ideal for high volume and automated assembly applications.

The NM27C240 operates from a single 5V ±10% supply in the read mode.

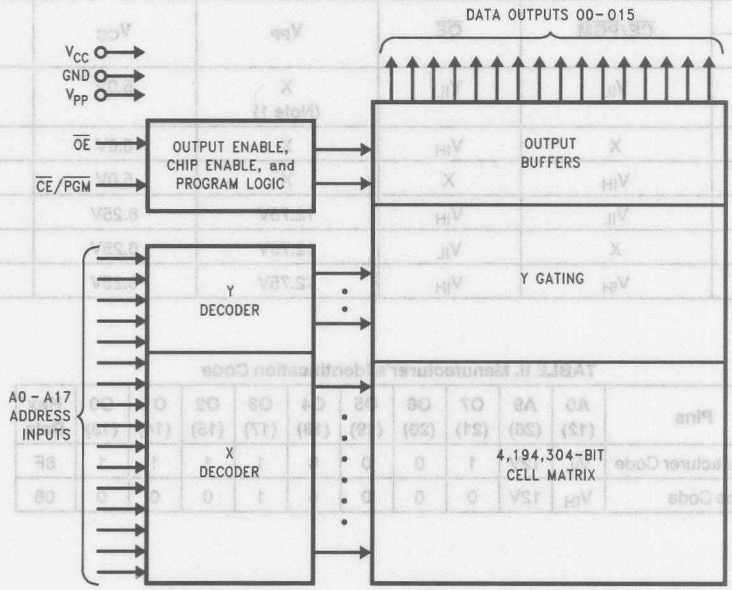
The NM27C240 is offered in both DIP and surface mount packages. The DIP package is a 40-pin dual-in-line ceramic with a quartz window to allow erasing. The surface mount package is a 44-pin PLCC that is offered in OTP.

This EPROM is manufactured using National's proprietary 0.8 micron CMOS AMG™ EPROM technology for an excellent combination of speed and economy while providing excellent reliability.

Features

- High performance CMOS
  - 120 ns access time
- Fast turn-off for microprocessor compatibility
- Simplified upgrade path
  - V_{PP} and PGM are "Don't Care" during normal read operation
- Compatible with 27240 and 27C240 EPROMs
- JEDEC standard pin configuration
  - 40-pin DIP package
  - 44-pin PLCC package
- Manufacturer's identification code
- Fast programming algorithm

Block Diagram



TL/D/11949-1

NM27C240

27C280	27C220	27C210	NM27C240	Pin	Pin	NM27C240	27C210	27C220	27C280
A18	XX V_{PP}	XX V_{PP}	XX/V_{PP}	1	40	V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{CE}$/PGM	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/$\overline{PGM}$	2	39	A17	XX/$\overline{PGM}$	$\overline{PGM}$	A17
O15	O15	O15	O15	3	38	A16	NC	A16	A16
O14	O14	O14	O14	4	37	A15	A15	A15	A15
O13	O13	O13	O13	5	36	A14	A14	A14	A14
O12	O12	O12	O12	6	35	A13	A13	A13	A13
O11	O11	O11	O11	7	34	A12	A12	A12	A12
O10	O10	O10	O10	8	33	A11	A11	A11	A11
O9	O9	O9	O9	9	32	A10	A10	A10	A10
O8	O8	O8	O8	10	31	A9	A9	A9	A9
GND	GND	GND	GND	11	30	GND	GND	GND	GND
O7	O7	O7	O7	12	29	A8	A8	A8	A8
O6	O6	O6	O6	13	28	A7	A7	A7	A7
O5	O5	O5	O5	14	27	A6	A6	A6	A6
O4	O4	O4	O4	15	26	A5	A5	A5	A5
O3	O3	O3	O3	16	25	A4	A4	A4	A4
O2	O2	O2	O2	17	24	A3	A3	A3	A3
O1	O1	O1	O1	18	23	A2	A2	A2	A2
O0	O0	O0	O0	19	22	A1	A1	A1	A1
$\overline{OE}$/V_{PP}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	20	21	A0	A0	A0	A0

TL/D/11949-2

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27C240 pins.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C240 Q, V 120	120
NM27C240 Q, V 150	150
NM27C240 Q, V 200	200

Extended Temperature Range (−40° to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27C240 QE, VE 120	120
NM27C240 QE, VE 150	150
NM27C240 QE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

Package types: NM27C240 Q, V XXX

NM27C240 Q, V, XXX

Q = Quartz-Windowed Ceramic DIP Package

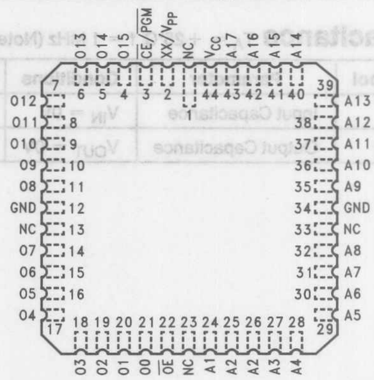
V = PLCC Package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.

Pin Names

A0–A15	Addresses
$\overline{CE}$/$\overline{PGM}$	Chip Enable/Program
$\overline{OE}$	Output Enable
O0–O15	Outputs
XX	Don't Care (During Read)
NC	No Connect

PLCC Pin Configuration



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Top View

3

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA		3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC}$ ±0.3V			100	μA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA	f = 5 MHz		40	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = VCC			10	μA
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	120		150		200		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	ns
t_{DF} (Note 2)	Output Disable to Output Float		35		45		55	ns
t_{OH} (Note 2)	Output Hold from Addresses $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		ns

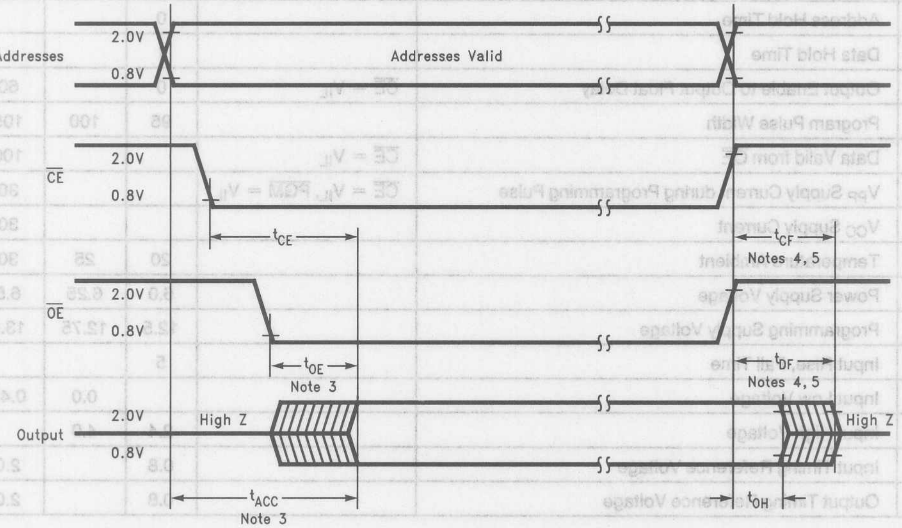
Capacitance T_A = +25°C, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	12	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA. C_L: 100 pF includes fixture capacitance.

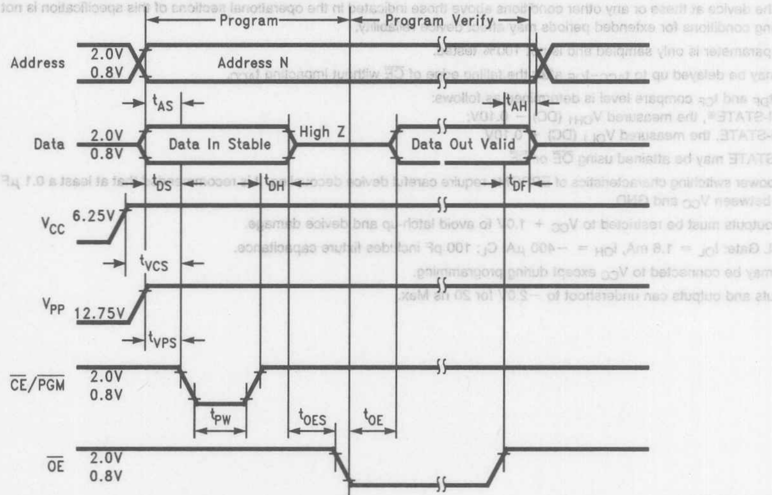
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

DC Electrical Characteristics (Notes 1, 2, 3, 4, and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1		2.4	µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				30	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

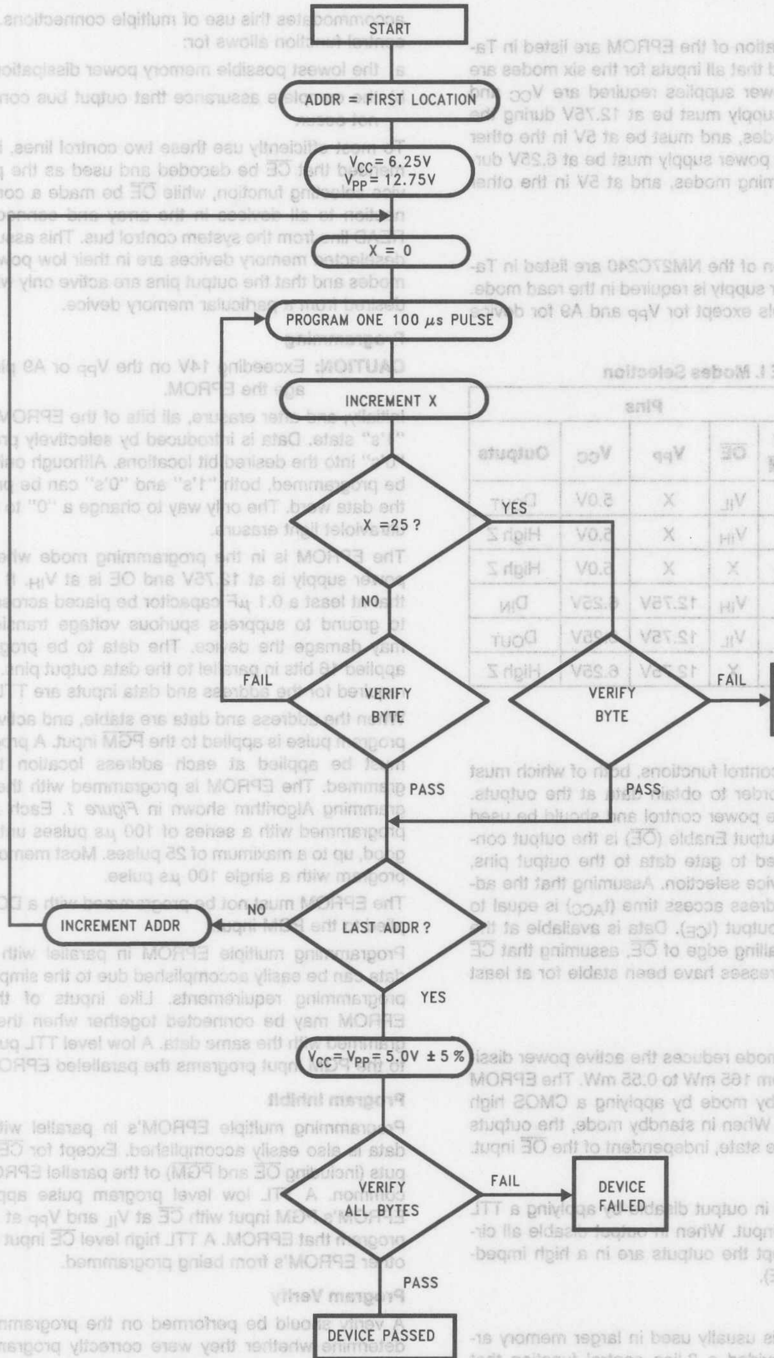
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/11949–6

FIGURE 1

3

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Mode Selection

The modes of operation of the NM27C240 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Mode	Pins				
	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	5.0V	High Z
Standby	V_{IH}	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of the device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM standby mode reduces the active power dissipation by over 99%, from 165 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that control function allows for:

a) the lowest possible memory power dissipation, and

b) the complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and OE is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, and active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's PGM input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

Functional Description (Continued)

After Programming

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

Manufacturer's Identification Code

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The manufacturer's identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27C240 is "8FEE", where "8F" designates that it is made by National Semiconductor, and "EE" designates a 4 Megabit (256k x 16) part.

The code is accessed by applying 12V ±0.5% to address pin A9. Addresses A1–A8, A10–A15, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O0–O7. Proper code access is only guaranteed at 25°C ±5°C.

Erasure Characteristics

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make sure full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

System Consideration

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O7 (12)	O6 (13)	O5 (14)	O4 (15)	O3 (16)	O2 (17)	O1 (18)	O0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	1	0	1	1	1	0	EE

3

National Semiconductor

Processor Oriented EPROM Selection Guide

General Description

National Semiconductor's family of Processor Oriented EPROMs are devices with features or functions to enhance their operation with various microprocessors and microcontrollers. There are 3 devices with specification improvements to help eliminate wait states and glue logic. Those are the NM27P512, NM27P210, and NM27P040.

Available Product

	Packages	Temperature Ranges*	Improved t_{DF}/t_{OH}
NM27P512	Q, N, V	C, E, M	Y
NM27P210	Q, V	C, E, M	Y
NM27P040	Q, N, V	C, E, M	Y
NM27P240 (Note 1)	V, Q	C, E, M	Y
NM27P020 (Note 1)	V, Q, T	C, E, M	Y
NM27P010 (Note 1)	V, N, Q, T	C, E, M	Y

Note 1: Contact your National Semiconductor sales representative for datasheet availability.

*Contact your National Semiconductor sales representative for military operating temperature range devices.

Ordering Information

NM 27 P 512 Q E 120

- NM — National Memory
- 27 — EPROM
- P — Processor Oriented
- 512 — Memory Configuration
  - 512 = 64k x 8
  - 010 = 128k x 8
  - 210 = 64k x 16
  - 020 = 256k x 8
  - 040 = 512k x 8
  - 240 = 256k x 16
- Q — Package
  - Q = Quartz Window Ceramic
  - N = Plastic DIP (OTP)
  - V = PLCC (OTP)
  - T = TSOP
- E — Operating Temperature Range
  - No Entry = 0°C to +70°C
  - E = −40°C to +85°C
  - M = −55°C to +125°C
- 120 — Speed

NM27P512
524,288-Bit (64K x 8) Processor Oriented CMOS EPROM

General Description

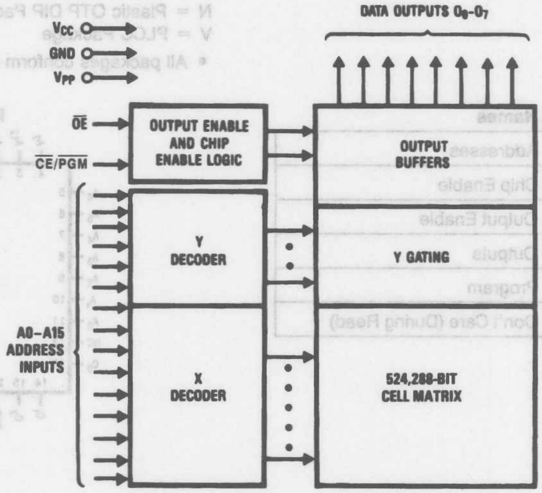
The NM27P512 is a 512K Processor Oriented EPROM configured as 64k x 8. It's designed to simplify microprocessor interfacing while remaining compatible with standard EPROMs. It can reduce both wait states and glue logic when the specification improvements are taken advantage of in the system design. The NM27P512 is implemented in National's advanced CMOS EPROM process to provide excellent reliability and access times as fast as 120 ns.

The interface improvements address two areas to eliminate the need for additional devices to adapt the EPROM to the microprocessor and to eliminate wait states at the termination of the access cycle. Even with these improvements, the NM27P512 remains compatible with industry standard JEDEC pinout EPROMs. The maximum specification for output turn-off time has been reduced, eliminating the need for wait states at the end of a read cycle. Also, the minimum specification for output hold time has been increased, eliminating the need for external circuitry to hold the data.

Features

- Fast output turn off to eliminate wait states
- Extended data hold time for microprocessor compatibility
- High performance CMOS
  — 120 ns access time
- JEDEC standard pin configuration
- Manufacturer's identification code

Block Diagram



TL/D/11365–1

A_{16}	A_{16}	A_{16}	A_{16}	
A_{15}	A_{15}	A_{15}	A_{15}	V_{PP}
A_{12}	A_{12}	A_{12}	A_{12}	A_{12}
A_7	A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

	XX/PGM	XX/PGM	A_{18}	A_{18}
V_{CC}	XX	A_{17}	A_{17}	A_{17}
A_{14}	A_{14}	A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}	A_{13}	A_{13}
A_8	A_8	A_8	A_8	A_8
A_9	A_9	A_9	A_9	A_9
A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

TL/D/11365–2

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27P512 pins.

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Access Time (ns)*
NM27P512 Q, N, V 120	120
NM27P512 Q, N, V 150	150
NM27P512 Q, N, V 200	200

Military Temp Range (−55°C to +125°C)

Parameter/Order Number	Access Time (ns)*
NM27P512 QM 200	200

Extended Temp Range (−40°C to +85°C)

Parameter/Order Number	Access Time (ns)*
NM27P512 QE, NE, VE 120	120
NM27P512 QE, NE, VE 150	150
NM27P512 QE, NE, VE 200	200

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

*All versions are guaranteed to function for slower speeds.

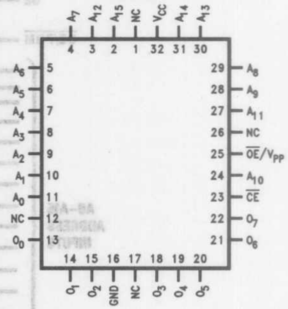
Package Types: NM27P512 Q, N, V XXX
Q = Quartz-Windowed Ceramic DIP Package
N = Plastic OTP DIP Package
V = PLCC Package

- All packages conform to the JEDEC standard.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

PLCC



TL/D/11365–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
All Input Voltages Except A9 with Respect to Ground	$-0.6V$ to $+7V$
V_{PP} and A9 with Respect to Ground	$-0.7V$ to $+14V$
V_{CC} Supply Voltage with Respect to Ground	$-0.6V$ to $+7V$
ESD Protection (MIL Std. 883, Method 3015.2)	>2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND $-0.6V$

Operating Range

Range	Temperature	V_{CC}	Tolerance
Comm'l	0°C to +70°C	+5V	±10%
Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.5	08	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA		3.5		V
I_{SB1}(10)	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA	f = 5 MHz		40	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10	10	μA

AC Electrical Characteristics

Symbol	Parameter	120		150		200		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50	ns
t_{DF}(2)	Output Disable to Output Float		25		25		25	ns
t_{CF}(2)	Chip Disable to Output Float		30		30		30	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	7		7		7		ns

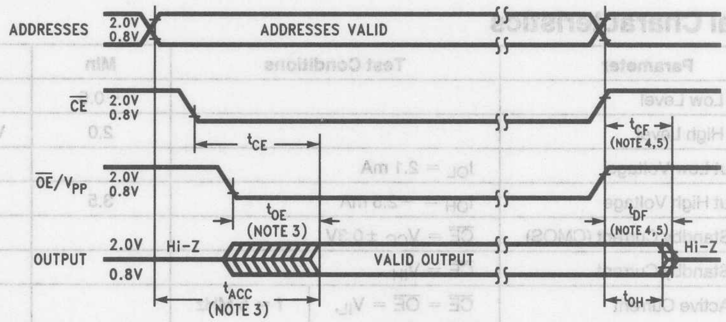
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	20	25	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level (Note 9)	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6, 7)



TL/D/11365-4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

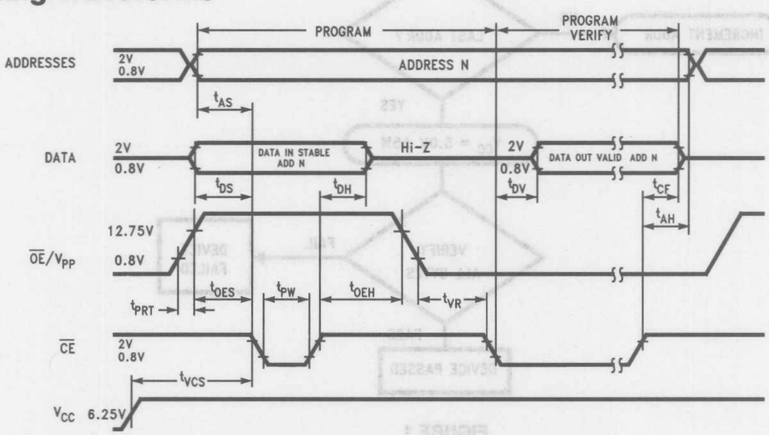
Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 10: CMOS inputs; V_{IL} = GND ±0.3V, $V_{IH} = V_{CC}$ ±0.3V.

Programming Characteristics (Notes 1 and 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OEH}	$\overline{OE}$ Hold Time		1			μs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			μs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing Reference Voltage		0.8		2	V

Programming Waveforms



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Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart

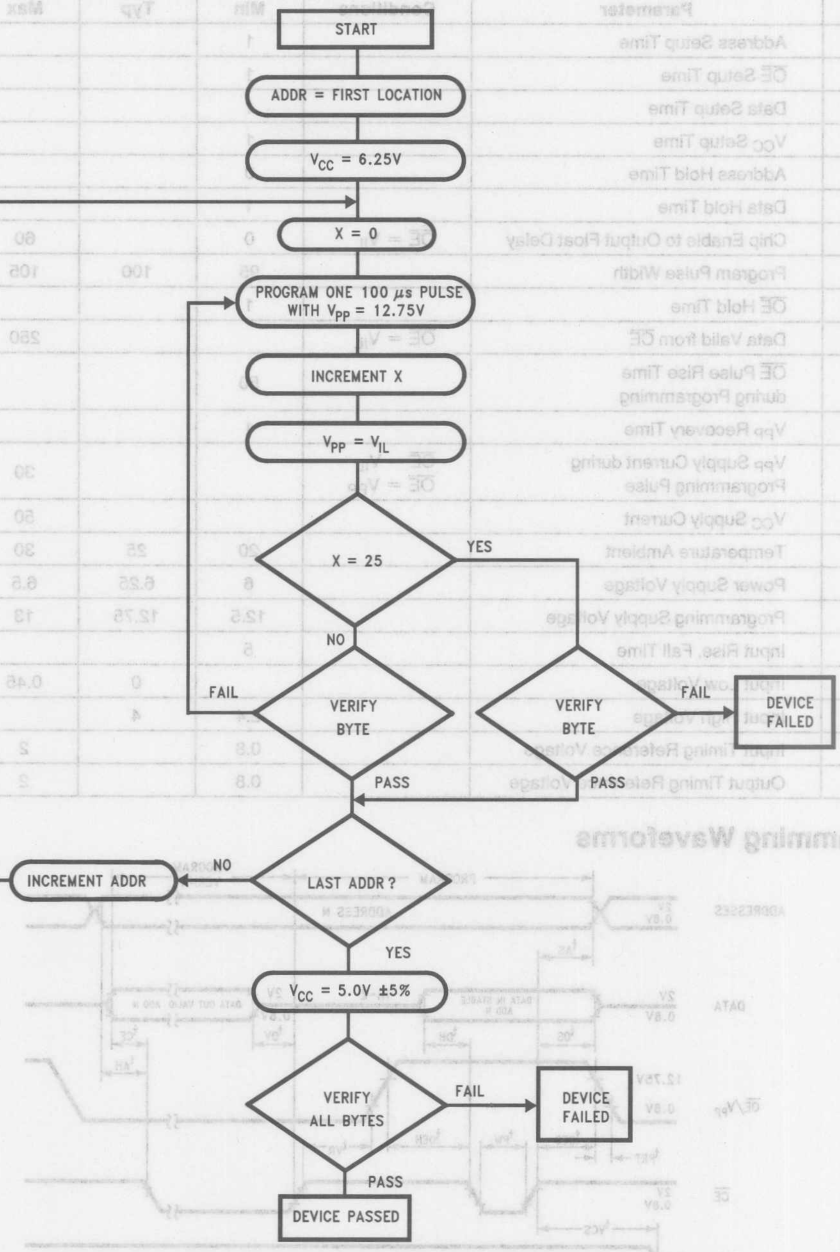


FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and OE/V_{PP}. The OE/V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE/PGM) is the power control and should be used for device selection. Output Enable (OE/V_{PP}) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from CE to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE, assuming that CE has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 385 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the CE/PGM input. When in standby mode, the outputs are in a high impedance state, independent of the OE input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the OE input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE/PGM be decoded and used as the primary device selecting function, while OE/V_{PP} be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 (OE/V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the OE/V_{PP} is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the CE/PGM input. A program pulse must be applied at each address location to be programmed.

The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the CE/PGM input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for CE/PGM all like inputs (including OE/V_{PP}) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's CE/PGM input with OE/V_{PP} at 12.75V will program that EPROM. A TTL high level CE/PGM input inhibits the other EPROMs from being programmed.

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with OE/V_{PP} and CE at V_{IL}. Data should be verified T_{DV} after the falling edge of CE.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27P512 is "8F85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512K part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C $\pm$5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15W-sec/cm².

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum EPROM erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	5.0V	High Z
Standby	V_{IH}	X	5.0V	High Z
Programming	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	0	1	85

National Semiconductor

NM27P210 1,048,576-Bit (64K x 16) Processor Oriented CMOS EPROM

General Description

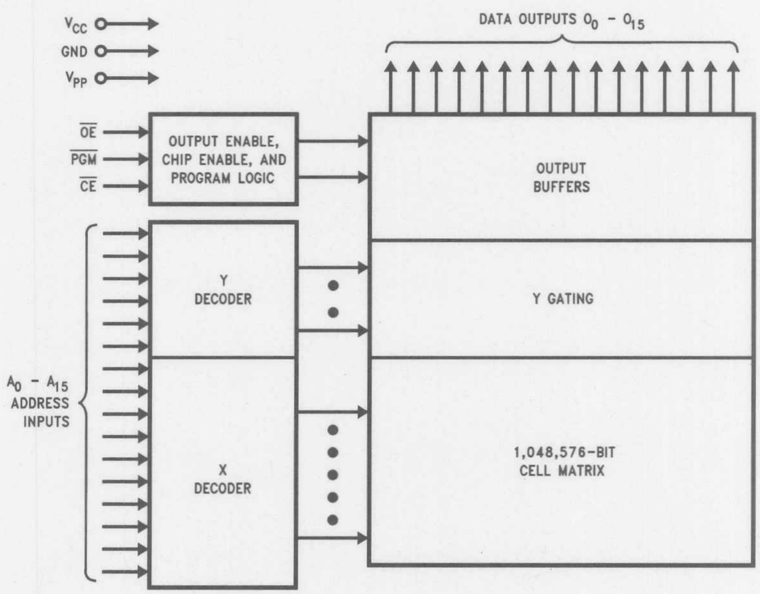
The NM27P210 is a 1024K Processor Oriented EPROM (POP™) configured as 64K x 16. It's designed to simplify microprocessor interfacing while remaining compatible with standard EPROMs. It can reduce both wait states and glue logic when the specification improvements are taken advantage of in the system design. The NM27P210 is implemented in National's advanced CMOS EPROM process to provide excellent reliability and access times as fast as 120 ns.

The interface improvements address two areas to eliminate the need for additional devices to adapt the EPROM to the microprocessor and to eliminate wait states at the termination of the access cycle. Even with these improvements, the NM27P210 remains compatible with industry standard JEDEC pinout EPROMs. The maximum spec. for output turn-off time has been reduced, eliminating the need for wait states at the end of a read cycle. Also, the minimum spec. for output hold time has been increased, eliminating the need for external circuitry to hold the data.

Features

- Fast output turn-off to eliminate wait states
- Extended data hold time for microprocessor compatibility
- High performance CMOS
  — 120 ns access time
- JEDEC standard pin configuration
- Manufacturer's identification code

Block Diagram



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Connection Diagrams

DIP PIN CONFIGURATIONS

27C280	27C240	27C220
A_{18}	XX/V_{PP}	XX/V_{PP}
$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$
O_{15}	O_{15}	O_{15}
O_{14}	O_{14}	O_{14}
O_{13}	O_{13}	O_{13}
O_{12}	O_{12}	O_{12}
O_{11}	O_{11}	O_{11}
O_{10}	O_{10}	O_{10}
O_9	O_9	O_9
O_8	O_8	O_8
GND	GND	GND
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3
O_2	O_2	O_2
O_1	O_1	O_1
O_0	O_0	O_0
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$

DIP
NM27P210

27C220	27C240	27C280
V_{CC}	V_{CC}	V_{CC}
$XX/\overline{PGM}$	A_{17}	A_{17}
A_{16}	A_{16}	A_{16}
A_{15}	A_{15}	A_{15}
A_{14}	A_{14}	A_{14}
A_{13}	A_{13}	A_{13}
A_{12}	A_{12}	A_{12}
A_{11}	A_{11}	A_{11}
A_{10}	A_{10}	A_{10}
A_9	A_9	A_9
GND	GND	GND
A_8	A_8	A_8
A_7	A_7	A_7
A_6	A_6	A_6
A_5	A_5	A_5
A_4	A_4	A_4
A_3	A_3	A_3
A_2	A_2	A_2
A_1	A_1	A_1
A_0	A_0	A_0

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27P210 pins.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P210 Q, V 120	120
NM27P210 Q, V 150	150

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P210 QM 200	150

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P210 QE, VE 120	120
NM27P210 QE, VE 150	150

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

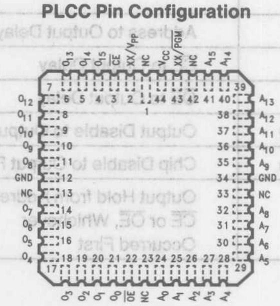
Package Types: NM27P210 Q, V XXX
Q = Quartz-Windowed Ceramic DIP package
V = PLCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
NC	No Connect

PLCC Pin Configuration



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Top View

Industrial	−40°C to +85°C	+5V	±10%
Military	−55°C to +125°C	+5V	±10%

Storage Temperature −65°C to +150°C

All Input Voltages except A9 with Respect to Ground (Note 10) −0.6V to +7V

V_{PP} and A9 with Respect to Ground −0.6V to +14V

V_{CC} Supply Voltage with Respect to Ground −0.6V to +7V

ESD Protection >2000V

All Output Voltages with Respect to Ground (Note 10) V_{CC} + 1.0V to GND − 0.6V

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA	3.5		V
I_{SB1} (Note 11)	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$		100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA; f = 5 MHz		50	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	μA
I_{LI}	Input Load Current	V_{IN} = 5.5 or GND	−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	μA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

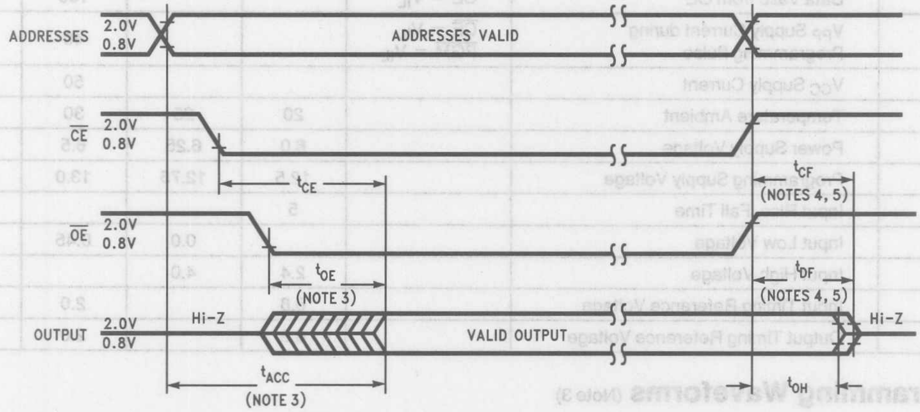
Symbol	Parameter	120		150		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50	ns
t_{DF} (Note 2)	Output Disable to Output Float		30		30	ns
t_{CF} (Note 2)	Chip Disable to Output Float		30		30	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	7		7		ns

C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤ 5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6, 7, & 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

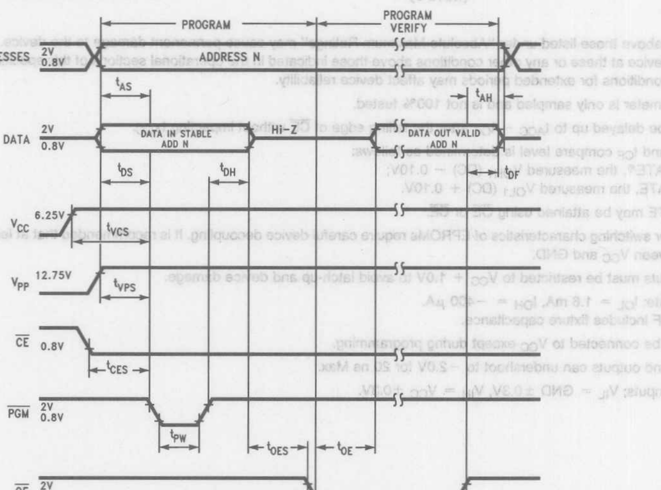
Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Note 11: CMOS inputs; V_{IL} = GND ± 0.3V, $V_{IH} = V_{CC} \pm 0.3$V.

Programming Characteristics (Notes 1, 2, 3, 4 & 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



TL/D/11366-5

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart

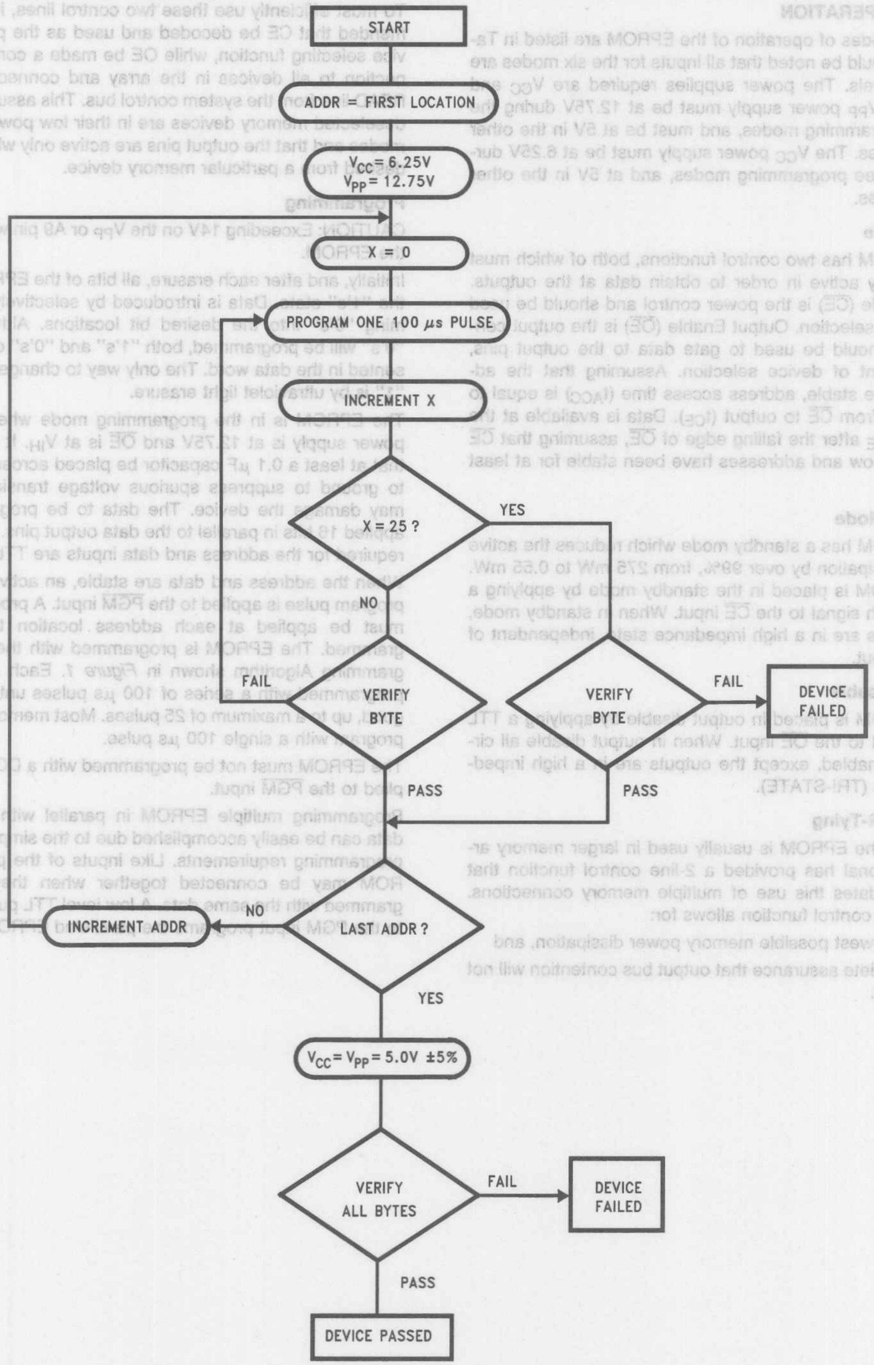


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FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 275 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27P210 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A_9. Addresses A_1–A_8, A_{10}–A_{15}, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	X	5.0V	High Z
Standby	V_{IH}	X	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

National Semiconductor

NM27P040
4,194,304-Bit (512K x 8) Processor Oriented CMOS EPROM

General Description

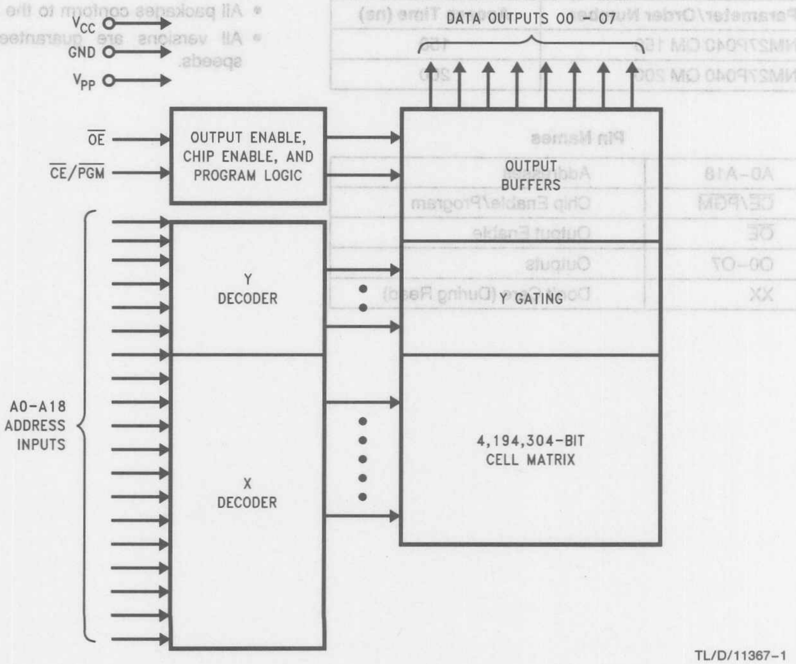
The NM27P040 is a 4096K Processor Oriented EPROM (POP™) configured as 512K x 8. It's designed to simplify microprocessor interfacing while remaining compatible with standard EPROMs. It can reduce both wait states and glue logic when the specification improvements are taken advantage of in the system design. The NM27P040 is implemented in National's advanced CMOS EPROM process to provide a reliable solution and access times as fast as 120 ns.

The interface improvements address two areas to eliminate the need for additional devices to adapt the EPROM to the microprocessor and to eliminate wait states at the termination of the access cycle. Even with these improvements, the NM27P040 remains compatible with industry standard JEDEC pinout EPROMs. The time from CE or OE being negated until the outputs are guaranteed to be in the high impedance state has been reduced to eliminate the need for wait states at the termination of the memory cycle and the data-out hold time has been extended to eliminate the need to provide data hold time for the microprocessor by delaying control signals or latching and holding the data in external latches.

Features

- Fast output turn off to eliminate wait states
- Extended data hold time for microprocessor compatibility
- High performance CMOS
  - 120 ns access time
- JEDEC standard pin configuration
- Manufacturer's identification code

Block Diagram



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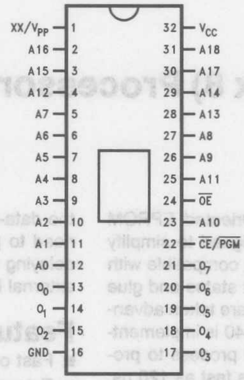
Connection Diagrams

27C080	27C020	27C010
A19	XX/V_{PP}	XX/V_{PP}
A16	A16	A16
A15	A15	A15
A12	A12	A12
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
O_0	O_0	O_0
O_1	O_1	O_1
O_2	O_2	O_2
GND	GND	GND

DIP
NM27P040



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27C010	27C020	27C080
V_{CC}	V_{CC}	V_{CC}
XX/$\overline{PGM}$	XX/$\overline{PGM}$	A18
XX	A17	A17
A14	A14	A14
A13	A13	A13
A8	A8	A8
A9	A9	A9
A11	A11	A11
$\overline{OE}$	$\overline{OE}$	$\overline{OE}/V_{PP}$
A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}/PGM$
O_7	O_7	O_7
O_6	O_6	O_6
O_5	O_5	O_5
O_4	O_4	O_4
O_3	O_3	O_3

Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27P040 pin.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P040 Q 120	120
NM27P040 Q 150	150
NM27P040 Q 170	170

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P040 QE 150	150
NM27P040 QE 170	170

Military Temperature Range (−55°C to +125°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27P040 QM 150	150
NM27P040 QM 200	200

Package Types: NM27P040 QXXX
Q = Quartz-Windowed Ceramic DIP

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.

Pin Names

A0–A18	Addresses
$\overline{CE}/\overline{PGM}$	Chip Enable/Program
$\overline{OE}$	Output Enable
O0–O7	Outputs
XX	Don't Care (During Read)

Storage Temperature	$-65°C$ to $+150°C$
All Input Voltages except A9 with Respect to Ground (Note 10)	$-0.6V$ to $+7V$
V_{PP} and A9 with Respect to Ground	$-0.6V$ to $+14V$
V_{CC} Supply Voltage with Respect to Ground	$-0.6V$ to $+7V$
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} +1.0V to GND −0.6V

Industrial	$-40°C$ to $+85°C$	±5V	±10%
Military	$-55°C$ to $+125°C$	±5V	±10%

Read Operation

DC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{IL}	Input Low Level		−0.2	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA	3.5		V
I_{SB1}	V_{CC} Standby Current (CMOS) (Note 11)	$\overline{CE} = V_{CC} \pm 0.3V$		100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$		1	mA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 mA f = 5 MHz		30	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$		10	μA
V_{PP}	V_{PP} Read Voltage		V_{CC} − 0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND	−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND	−10	10	μA

AC Electrical Characteristics Over operating range with $V_{PP} = V_{CC}$

Symbol	Parameter	120		150		170		250		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		120		150		170		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		120		150		170		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		50		50		50		50	ns
t_{DF} (Note 2)	Output Disable to Output Float		35		25		25		25	ns
t_{CF} (Note 2)	Chip Disable to Output Float		35		30		30		30	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	7		7		7		7		ns

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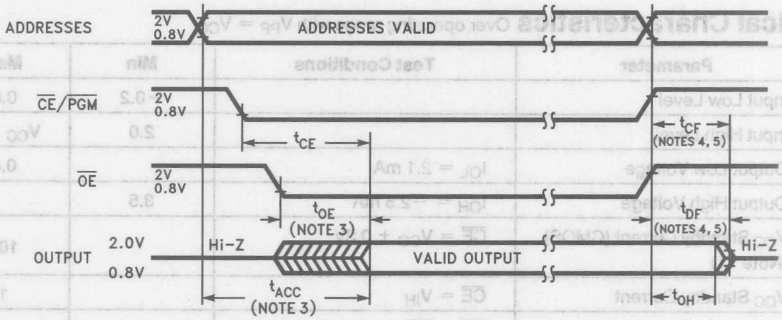
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)
Input Rise and Fall Times	≤ 5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 6, 7, and 9)



TL/D/11367-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

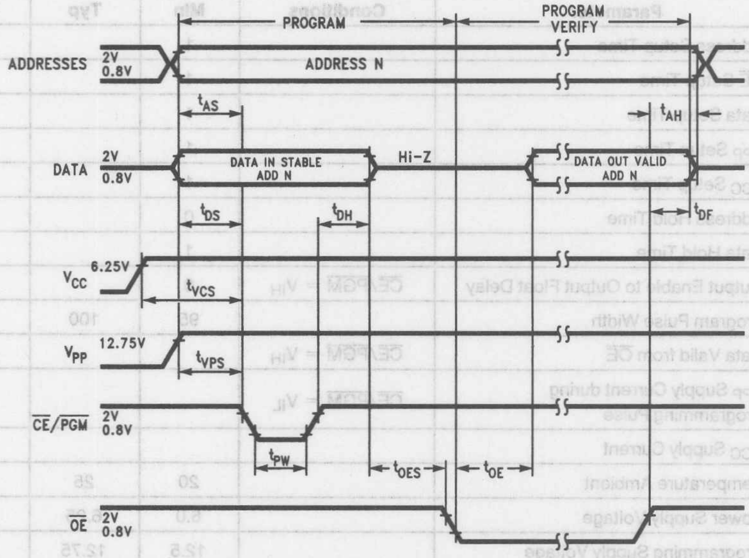
Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: CMOS input: V_{IL} = GND ±0.3V, $V_{IH} = V_{CC}$ ±0.3V.

Programming Waveform (Note 3)



TL/D/11367–4

Programming Characteristics (Notes 1, 2, 3 & 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = V_{IH}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IH}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				30	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

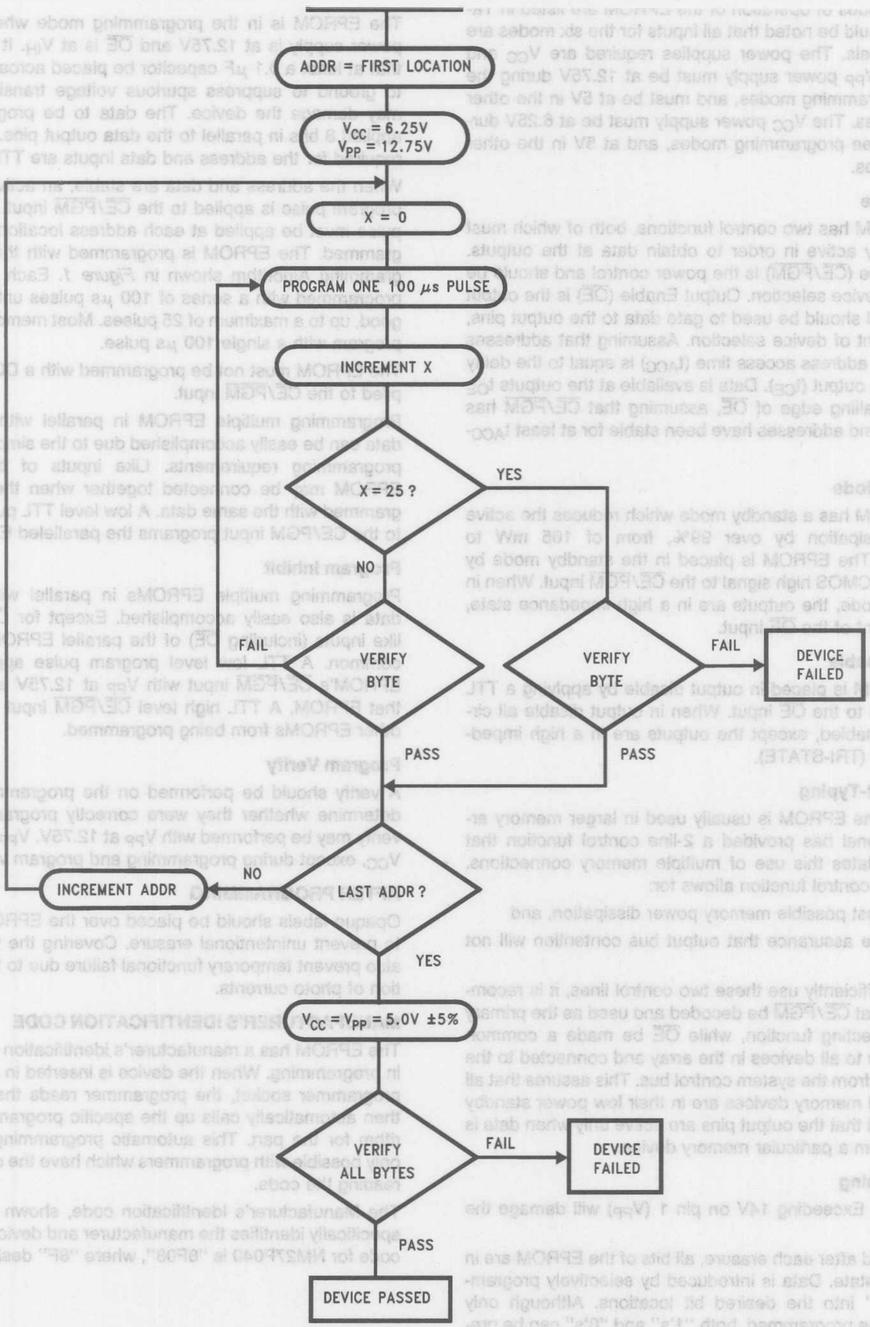
Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Progam Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{CE}/\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.



TL/D/11367–5

FIGURE 1

3

ble I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}/\overline{PGM}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}/\overline{PGM}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from of 165 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}/\overline{PGM}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Typing

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}/\overline{PGM}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be pre-

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}/\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}/\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the CE/PGM input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$ all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}/\overline{PGM}$ input with V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}/\overline{PGM}$ input inhibits the other EPROMs from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27P040 is "8F08", where "8F" designates that

Functional Description (Continued)

it is made by National Semiconductor, and "08" designates a 4 Megabit (512K x 8) part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A18, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C ±5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp. (If distance is doubled the erasure time increases by factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27P040 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	5.0V	D_{OUT}
Output Disable	X	V_{IH}	X	5.0V	High Z
Standby	V_{IH}	X	X	5.0V	High Z
Programming	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_H

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	0	0	0	0	1	0	0	0	08

3

National Semiconductor

NMC87C257
262,144-Bit (32K x 8) CMOS EPROM with On-Chip Address Latches

General Description

The NMC87C257 is a CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC87C257 has latched addresses for direct interfacing with address/data multiplexed microprocessors and microcontrollers. The A0–A7 pins can be tied to the respective O0–O7 pins and then bused to the microprocessor or microcontroller directly. No latch device is needed for interfacing.

The part is designed to operate with a single +5V power supply with ±10% tolerance.

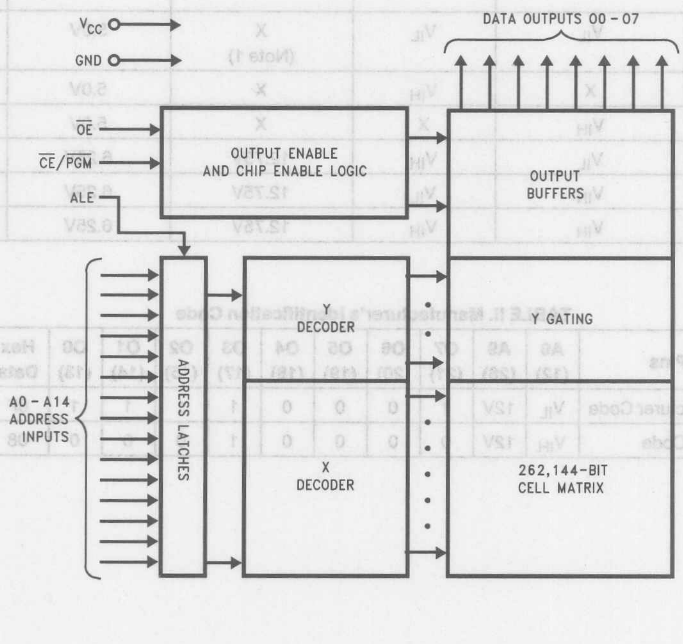
The part is packaged in a 28-pin dual-in-line package with a quartz window or PLCC. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure. The PLCC is not erasable.

This EPROM is fabricated with National's proprietary CMOS double-poly silicon gate technology.

Features

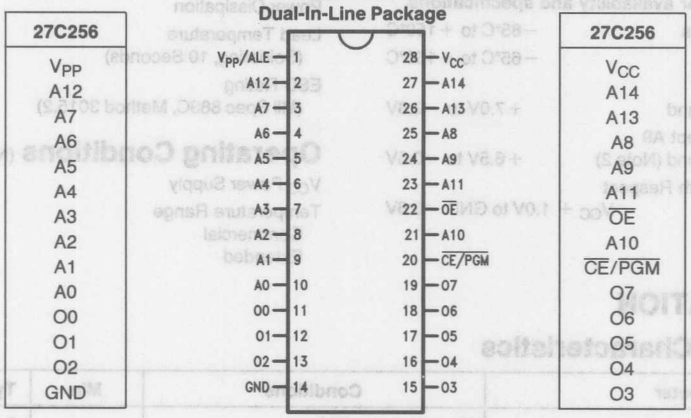
- Address latches for direct interfacing with address/data multiplexed microprocessors
- Low CMOS power consumption:
  - — Active power: 110 mW max
  - — Standby power: 0.55 mW max
- Pin compatible with standard 256K EPROM
- Fast and reliable programming
- TTL, CMOS compatible inputs/outputs
- TRI-STATE® output
- Manufacturer's identification code for automatic programming control use NMC27C256B PGM Algorithm
- High current CMOS level output drivers

Block Diagram



TL/D/11012–1

Dual-In-Line Package



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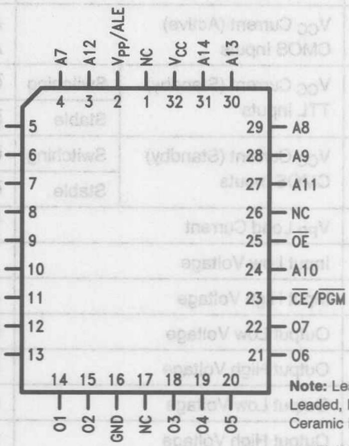
Note: Socket compatible 27C256 EPROM pin configuration is shown in the block adjacent to the NMC87C257 pins.

Pin Names

Symbol	Description
A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
ALE	Address Latch Enable
V_{PP}	Programming Supply
V_{CC}	Power Supply
GND	Ground
NC	No Connection

PLCC Pin Configuration



Note: Leadless or Leaded, Plastic or Ceramic Package

TL/D/11012-8

Top

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC87C257Q150, V150	150
NMC87C257Q200, V200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NMC87C257QE150	150
NMC87C257QE200	200

3

Office/Distributors for availability and specifications.

Temperature under Bias	−65°C to +150°C
Storage Temperature	−65°C to +150°C
V_{CC} Supply Voltages with Respect to Ground	+7.0V to −0.6V
All Input Voltages except A9 with Respect to Ground (Note 2)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 2)	V_{CC} + 1.0V to GND −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 Seconds)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	1700V

Operating Conditions (Note 3)

V_{CC} Power Supply	5V ±10%
Temperature Range	
Commercial	0°C to +70°C
Extended	−40°C to +85°C

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current		$V_{IN} = V_{CC}$ or GND		0.01	1.0	μA
I_{LO}	Output Leakage Current		$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$		0.01	1.0	μA
I_{CC1} (Note 4)	V_{CC} Current (Active) TTL Inputs		ALE = V_{IH}, f = 5 MHz All Inputs = V_{IH} or V_{IL}, I/O = 0 mA		15	30	mA
I_{CC2} (Note 4)	V_{CC} Current (Active) CMOS Inputs		ALE = V_{CC}, f = 5 MHz All Inputs = V_{CC} or GND, I/O = 0 mA		10	20	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	Switching	$\overline{CE} = V_{IH}$, ALE = V_{IH}		10	12	mA
		Stable	$\overline{CE} = V_{IH}$, ALE = V_{IL}		0.3	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	Switching	$\overline{CE} = V_{CC}$, ALE = V_{CC}		8	10	mA
		Stable	$\overline{CE} = V_{CC}$, ALE = GND		50	100	μA
I_{PP}	V_{PP} Load Current		$V_{PP} = V_{CC}$			10	μA
V_{IL}	Input Low Voltage			−0.2		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage		I_{OL} = 2.1 mA			0.40	V
V_{OH1}	Output High Voltage		I_{OH} = −2.5 mA	3.5			V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA			0.1	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	V_{CC} − 0.1			V

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 3: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 4: V_{PP} may be connected to V_{CC} except during programming.

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC87C257 150 Min	NMC87C257 150 Max	NMC87C257 200 Min	NMC87C257 200 Max	Units
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$		150		200	ns
t_{CE}	Chip Enable Access Time	$\overline{OE} = V_{IL}$		150		200	ns
t_{LL}	Chip Deselect Width		30		50		ns
t_{AL}	Address to ALE Latch Set-Up		5		15		ns
t_{LA}	Address Hold from ALE Latch		20		30		ns
t_{OE}	Output Enable to Output Valid	$\overline{CE} = V_{IL}$		50		75	ns
t_{LOE}	ALE to Output Enable		20		30		ns
t_{CF} (Note 1)	Chip Disable to Output in High Z	$\overline{OE} = V_{IL}$	0	50	0	55	ns
t_{DF} (Note 1)	Output Disable to Output in High Z	$\overline{CE} = V_{IL}$	0	50	0	55	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurred first		0		0		ns

Note 1: This parameter is only sampled and is not 100% tested.

Capacitance $T_A = +25°C$, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

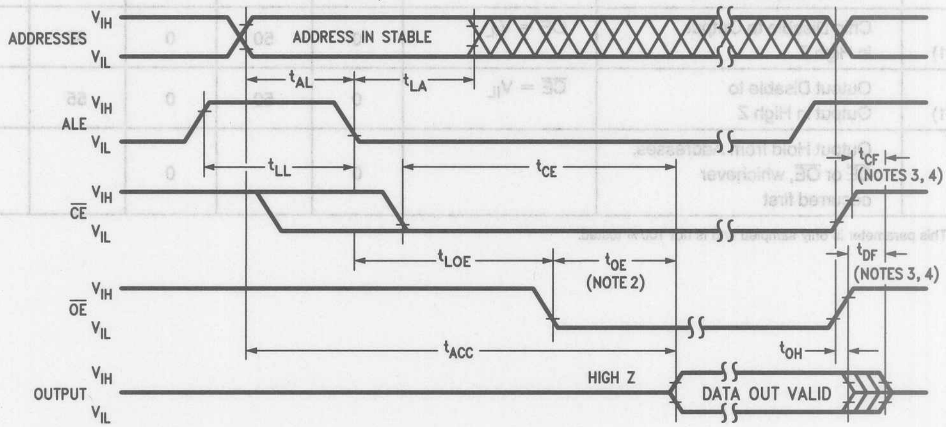
AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 7)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V

Timing Measurement Reference Level

Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Notes 5, 6 and 8)



TL/D/11012–3

Note 1: This parameter is only sampled and is not 100% tested.

Note 2: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 3: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 4: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 5: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

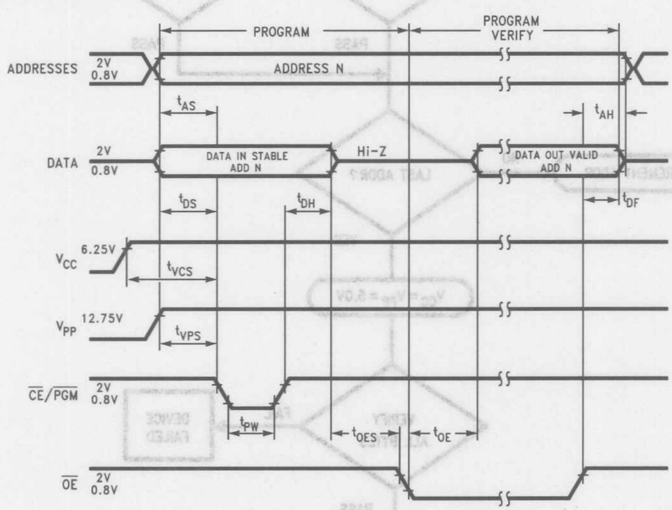
Note 6: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 7: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 8: V_{PP} may be connected to V_{CC} except during programming.

t_{AS}	Address Setup Time		1			μs
t_{OES}	$\overline{OE}$ Setup Time		1			μs
t_{DS}	Data Setup Time		1			μs
t_{VPS}	V_{PP} Setup Time		1			μs
t_{VCS}	V_{CC} Setup Time		1			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Output Enable to Output Float Delay		0		60	ns
t_{PW}	Program Pulse Width		95	100	105	μs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{OE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

Programming Waveforms



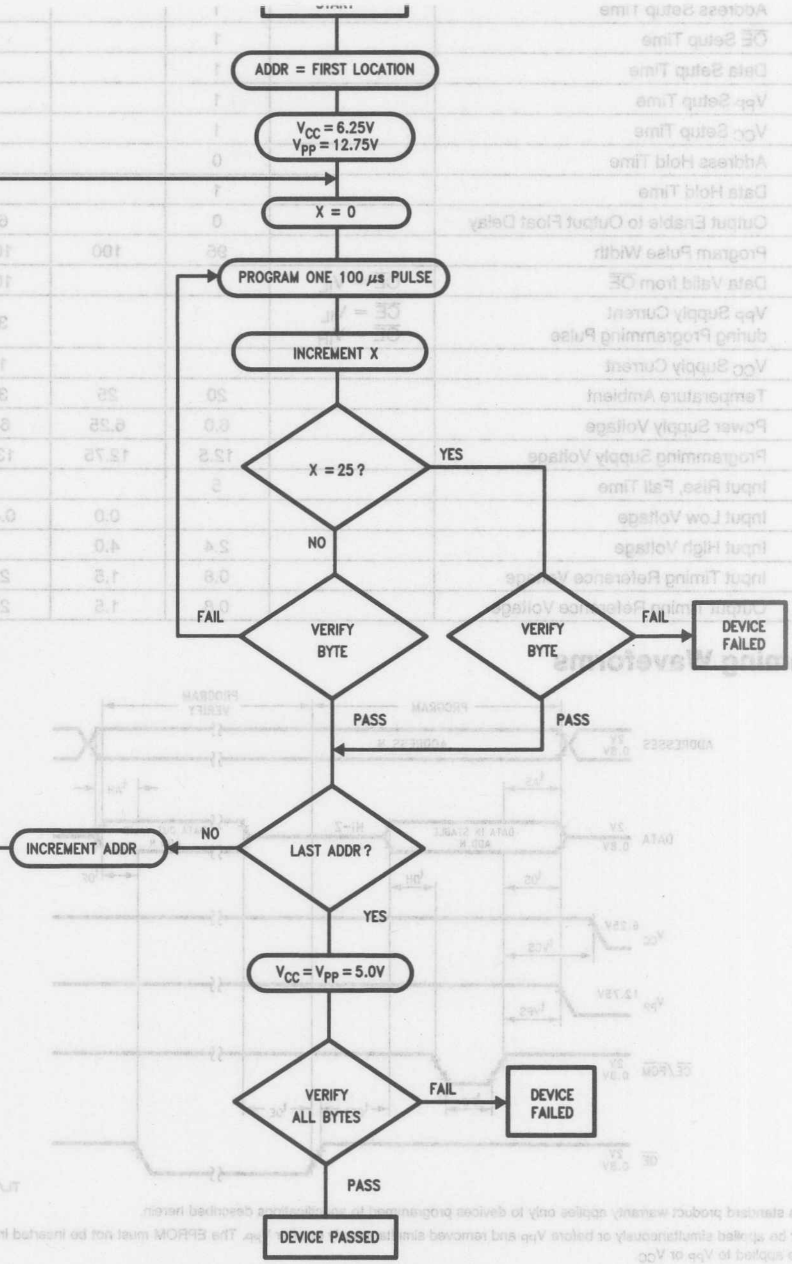
TL/D/11012–4

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.



TL/D/11012–5

FIGURE 1

Note 1: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Functional Description

DEVICE OPERATION

The seven modes of operation of the NMC87C257 are listed in Table I. It should be noted that all inputs for the seven modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 5V in the other modes.

Read Mode

The NMC87C257 has a chip enable (CE) and an output enable (OE), both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}), is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Address Latch Operation

The NMC87C257 has an Address Latch Enable (ALE) pin which latches the address inputs on a negative transition. Addresses must be stable for the address setup time (t_{AL}) before the ALE transition, and they must hold for the address hold time (t_{LA}) after the transition. After the hold time has transpired the address drive can be removed from the address input pins and the bus can be used for other signals. The ALE pin is a feed-through latch and the part will operate as a normal unlatched device when the ALE pin is held high.

An important application for the NMC87C257 is memory in an address/data multiplexed microprocessor system. In an 8 bit system the low order memory address pins, A0–A7, can be tied to the respective memory output pins, O0–O7 and run on an 8-bit bus to the AD0–AD7 pins of the microprocessor. This reduces the bus width and it can be done without adding an address latch interface device. In this application the Output Enable ($\overline{OE}$) pin should be held high until after the address hold time (t_{LA}) has transpired, to avoid bus contention.

Standby Mode

The NMC87C257 has a standby mode which reduces the active power dissipation by over 99%, from 110 mW to 0.55 mW. The NMC87C257 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input and a CMOS low signal to the ALE input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC87C257s are usually used in larger memory arrays, National has provided a 3-line control function that accommodates this use of multiple memory connections. The 3-line control function allows for:

a. the lowest possible memory power dissipation, and

b. complete assurance that output bus contention will not occur.

To most efficiently use these control lines, it is recommended that $\overline{CE}$ and ALE be decoded and used as the primary device selecting functions while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC87C257.

Initially, and after each erasure, all bits of the NMC87C257 are in the "1" state. Data is introduced by selectively programmings "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by untraviolet light erasure.

The NMC87C257 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The NMC87C257 is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse. The NMC87C257 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Functional Description (Continued)

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP}/ALE (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	D_{OUT}
Latched	V_{IL}	V_{IL}	V_{IL}	5V	D_{OUT}
Standby	V_{IH}	Don't Care	V_{IL}	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	Hi-Z
Program	V_{IL}	V_{IH}	12.75V	6.25V	D_{IN}
Program Verify	V_{IH}	V_{IL}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	12.75V	6.25V	Hi-Z

Programming multiple NMC87C257s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC87C257 may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC87C257.

Program Inhibit

Programming multiple NMC87C257s in parallel with different data is also easily accomplished. Except $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC87C257s may be common. A TTL low level program pulse applied to an NMC87C257 $\overline{CE}$ input with V_{PP} at 12.75V will program that NMC87C257. A TTL high level $\overline{CE}$ input inhibits the other NMC87C257 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC} except during programming and program verify.

Manufacturer's Identification Code

The NMC87C257 has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and the device type. The code for NMC87C257 is "8F04", where "8F" designates that it is made by National Semiconductor, and "04" designates a 256K part.

The code is accessed by applying 12.0V ± 0.5V to address pin A9. Addresses A1–A8, A10–A14, and all control pins are held at V_{IL} and V_{PP}/ALE is held at V_{IH}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O0–O7. Proper code access is only guaranteed at 25°C ± 5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC87C257 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. After programming, opaque labels should be placed over the NMC87C257 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC87C257 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 W-sec/cm^2.

The NMC87C257 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NMC87C257 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Functional Description (Continued)

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	0	0	0	0	0	1	0	0	04

TABLE III. Minimum NMC87C257 Erasure Time

Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

3

National Semiconductor

Low Voltage EPROM Selection Guide

General Description

National Semiconductor's family of Low Voltage EPROMs are devices with low power consumption for power sensitive systems. Specifically, hand held and portable battery operated products.

National's family of Low Voltage EPROMs includes mid to high density, high performance devices.

Available Product

	Packages	Temperature Ranges*	Improved t_{DF}/t_{OH}
NM27LV512	Q, V, T	C, E, M	Y
NM27LV010	Q, V, T	C, E, M	Y
NM27LV210	V, F	C, E, M	Y

*Contact your National Semiconductor sales representative for military operating temperature range devices.

Ordering Information

NM 27 LV 512 Q E 120

- **NM** — **National Memory**
- **27** — **EPROM**
- **LV** — **Low Voltage**
- **512** — **Memory Configuration**
  - 512 = 64k x 8
  - 010 = 128k x 8
  - 210 = 64k x 16
- **Q** — **Package**
  - Q = Quartz Window Ceramic
  - V = PLCC (OTP)
  - T = TSOP
  - F = TQFP (10 x 10 x 1.4)
- **E** — **Operating Temperature Range**
  - No Entry = 0°C to +70°C
  - E = −40°C to +85°C
  - M = −55°C to +125°C
- **120** — **Speed**

Note: Please consult with National Semiconductor representative regarding availability of other newly released low voltage devices.

National Semiconductor

PRELIMINARY

NM27LV512
524,288-Bit (64k x 8) Low Voltage EPROM

General Description

The NM27LV512 is a high performance Low Voltage Electrical Programmable Read Only Memory. It is manufactured using National's latest 1.2μ CMOS split gate SVG EPROM technology. This technology allows the part to operate at speeds as fast as 200 ns over commercial temperature (0°C to 70°C), and 250 ns over industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive handheld and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

National still maintains its commitment to high quality and reliability with EPI processing on the NM27LV512. Latch-up immunity is guaranteed for stresses up to 200 mA on address and data pins from −1V to V_{CC} + 0.3V. ESD protection is guaranteed to 2000V.

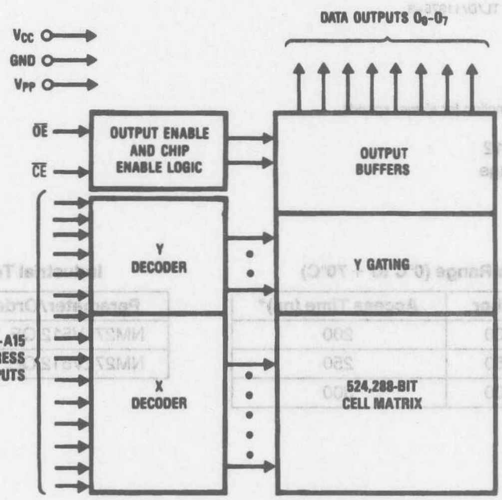
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has forseen this need and provides windowed LCC for prototyping and software development, PLCC for production runs, and TSOP for PC board space sensitive users.

The NM27LV512 is one member of National's growing Low Voltage product family.

Features

- 3.0V to 5.5V operation
- 200 ns access time
- Low current operation
  - 15 mA I_{CC} Active Current @ 5 MHz
  - 20 μA I_{CC} Standby Current @ 5 MHz
- Ultra Low Power operation
  - 50 μW Standby Power @ 3.3V
  - 50 mW Active Power @ 3.3V
- Surface mount package options
  - 28-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP

Block Diagram



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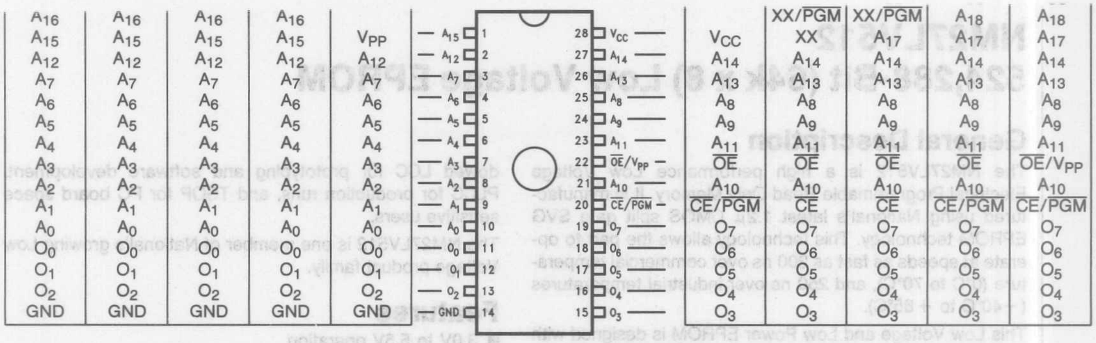

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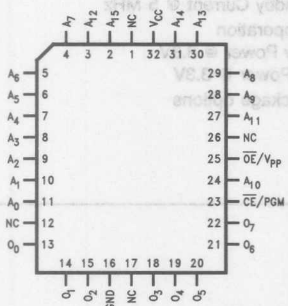
Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27LV512 pins.

PLCC



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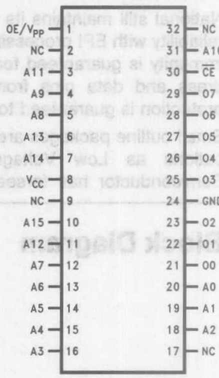
Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

TSOP



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*All versions are guaranteed to function for slower speeds.

Package Types: NM27LV512
- Q = Ceramic DIP Package
- V = PLCC Package
- T = TSOP Package

Commercial Temp Range (0°C to +70°C)

Parameter/Order Number	Access Time (ns)*
NM27LV512 Q, V, T, 200	200
NM27LV512 Q, V, T, 250	250
NM27LV512 Q, V, T, 300	300

Industrial Temp Range (−40°C to +85°C)

Parameter/Order Number	Access Time (ns)*
NM27LV512 QE, VE, TE 250	250
NM27LV512 QE, VE, TE 300	300

Storage Temperature	−65°C to +150°C	(MIL Std. 883, Method 3015.2)	>2000V
All Input Voltages Except A9 with Respect to Ground	−0.6V to +7V	All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND −0.6V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V		

Operating Range

Range	Temperature	V_{CC}	Tolerance
Comm'l	0°C to +70°C	3.3V	±0.3V
Industrial	−40°C to +85°C	3.3V	±0.3V

Read Operation

DC Electrical Characteristics

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.3	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage (TTL)	I_{OL} = 2.0 mA			0.4	V
V_{OH1}	Output High Voltage (TTL)	I_{OH} = −2.0 mA		2.4		V
V_{OL2}	Output Low Voltage (CMOS)	I_{OL} = 100 μA			0.2	V
V_{OH2}	Output High Voltage (CMOS)	I_{OH} = −100 μA		V_{CC} − 0.3		V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ±0.3V			20	μA
I_{SB2}	V_{CC} Standby Current (TTL)	$\overline{CE}$ = V_{IH}			100	μA
I_{CC1}	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	f = 5 MHz		15	mA
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA C, I Temp Ranges			15	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC} − 0.7	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 3.3V or GND		−1	1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 3.3V or GND		−1	1	μA

AC Electrical Characteristics

Symbol	Parameter	200		250		300		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay		75		100		120	ns
t_{DF}	Output Disable to Output Float	0	60	0	60	0	105	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		ns

3

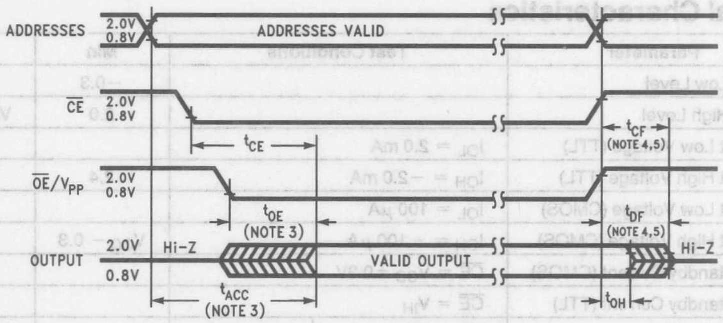
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$	20	25	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level (Note 9)	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6, 7)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

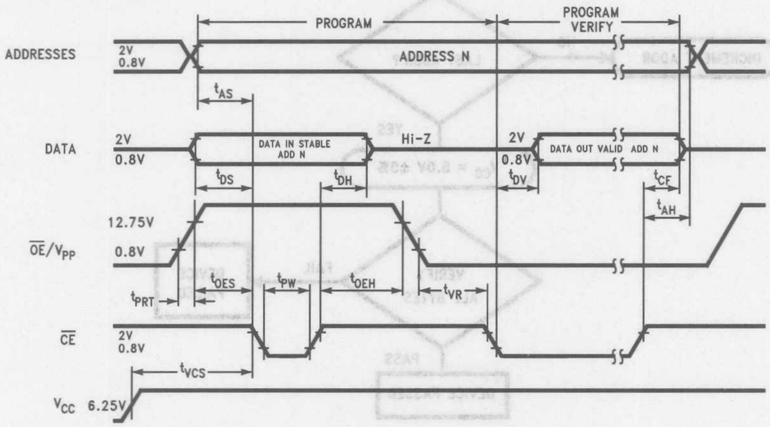
Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1 and 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{CF}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OEH}	$\overline{OE}$ Hold Time		1			µs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time during Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			µs
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8		2	V
t_{OUT}	Output Timing Reference Voltage		0.8		2	V

Programming Waveforms



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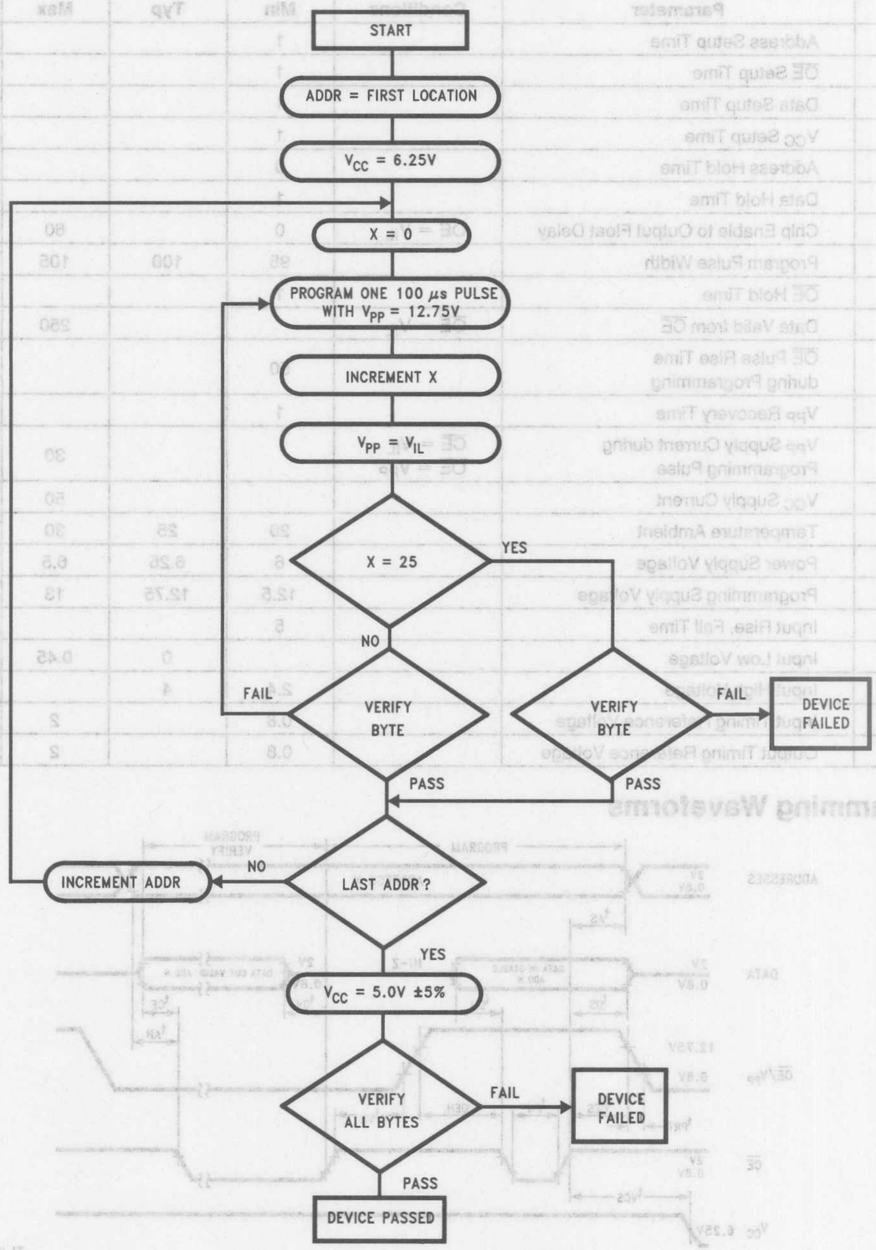
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings.

Fast Programming Algorithm Flow Chart (Same as NMC27C512A)



TL/D/11375-7

FIGURE 1

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and $\overline{OE}/V_{PP}$. The $\overline{OE}/V_{PP}$ power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}/V_{PP}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 44 mW to 110 μW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus.

This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the OE/V_{PP} is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed.

The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}/V_{PP}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROM's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROMs from being programmed.

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified T_{DV} after the falling edge of $\overline{CE}$.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27LV512 is "8F85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512k part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A15, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C $\pm$5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

posure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increase as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27LV512 are listed in Table I. A single 3.3V power supply is required in the read mode. All inputs are TTL levels excepts for V_{PP} and A9 for device signature.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	3.3V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	3.3V	High Z
Standby	V_{IH}	X	3.3V	High Z
Programming	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	0	1	85

3

National Semiconductor

PRELIMINARY

NM27LV010
1,048,576-Bit (128k x 8) Low Voltage EPROM

General Description

The NM27LV010 is a high performance Low Voltage Electrically Programmable Read Only Memory. It is manufactured using National's latest 0.8μ CMOS split gate AMG™ EPROM technology. This technology allows the part to operate at speeds as fast as 150 ns over Industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

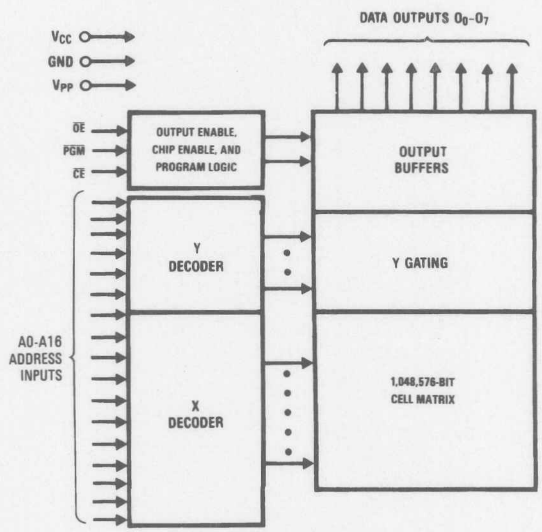
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has foreseen this need and provides windowed LCC for prototyping and software development, PLCC for production runs, and TSOP for PC board sensitive applications.

The NM27LV010 is one member of National's growing Low Voltage product Family.

Features

- 3.0V to 3.6V operation
- 150 ns access time
- Low current operation
  - — 15 mA I_{CC} active current @ 5 MHz
  - — 20 μA I_{CC} standby current @ 5 MHz
- Ultra low power operation
  - — 66 μW standby power @ 3.3V
  - — 50 mW active power @ 3.3V
- Surface mount package options
  - — 32-pin TSOP
  - — 32-pin PLCC

Block Diagram



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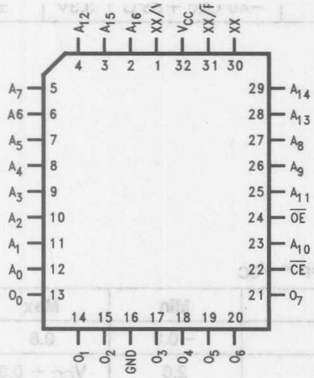
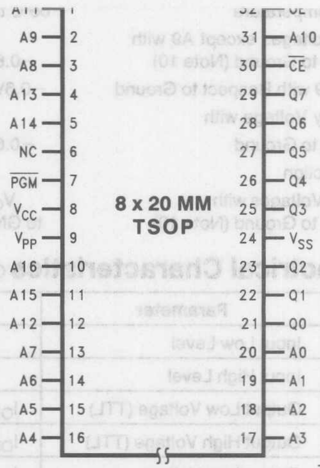


TL/D/11377-6

Top View



TL/D/11377-2

Top View

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 3.3 ± 0.3

Parameter/Order Number	Access Time (ns)
NM27LV010 C, V, T 150	150
NM27LV010 C, V, T 200	200
NM27LV010 C, V, T 250	250

Industrial Temperature Range (−40°C to +85°C)
V_{CC} = 3.3 ± 0.3

Parameter/Order Number	Access Time (ns)
NM27LV010CE, VE, TE	150
NM27LV010CE, VE, TE	200
NM27LV010CE, VE, TE	250

Note: Surface mount PLCC available for commercial and extended temperature ranges only.

Pin Names

A0–A16	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
V_{PP}	Programming Voltage

Package Types: NM27LV010 C, V, T
C = Quartz-Windowed LCC Package
V = PLCC
T = TSOP

- All packages conform to the JEDEC standard.
- All versions are guaranteed to function for slower speeds.
- Consult the NSC Sales office on new released products and packages.
- Consult the NSC representative for custom products for your specific application.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65^\circ C$ to $+150^\circ C$
All Input Voltages except A9 with Respect to Ground (Note 10)	$-0.6V$ to $+7V$
V_{PP} and A9 with Respect to Ground	$-0.6V$ to $+14V$
V_{CC} Supply Voltage with Respect to Ground	$-0.6V$ to $+7V$
ESD Protection	$>2000V$
All Output Voltages with Respect to Ground (Note 10)	$V_{CC} + 1.0V$ to GND $- 0.6V$

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	$0^\circ C$ to $+70^\circ C$	3.3V	$\pm 0.3V$
Industrial	$-40^\circ C$ to $+85^\circ C$	3.3V	$\pm 0.3V$

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			-0.3	0.8	V
V_{IH}	Input High Level			2.0	$V_{CC} + 0.3$	V
V_{OL1}	Output Low Voltage (TTL)	$I_{OL} = 2.0$ mA			0.4	V
V_{OH1}	Output High Voltage (TTL)	$I_{OH} = -2.0$ mA		2.4		V
V_{OL2}	Output Low Voltage	$I_{OL} = 100\ \mu A$			0.2	V
V_{OH2}	Output High Voltage (CMOS)	$I_{OH} = -100\ \mu A$		$V_{CC} - 0.3$		
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			20	μA
I_{SB2}	V_{CC} Standby Current(TTL)	$\overline{CE} = V_{IH}$			100	μA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O $= 0\ \mu A$	f = 5 MHz		15	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	μA
V_{PP}	V_{PP} Read Voltage			$V_{CC} - 0.7$	V_{CC}	V
I_{LI}	Input Load Current	$V_{IN} = 3.0V$ or GND			1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 3.0V$ or GND		-1	1	μA

AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	150		200		250		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		65		70		75	ns
t_{DF} (Note 2)	Output Disable to Output Float		50		50		50	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		ns

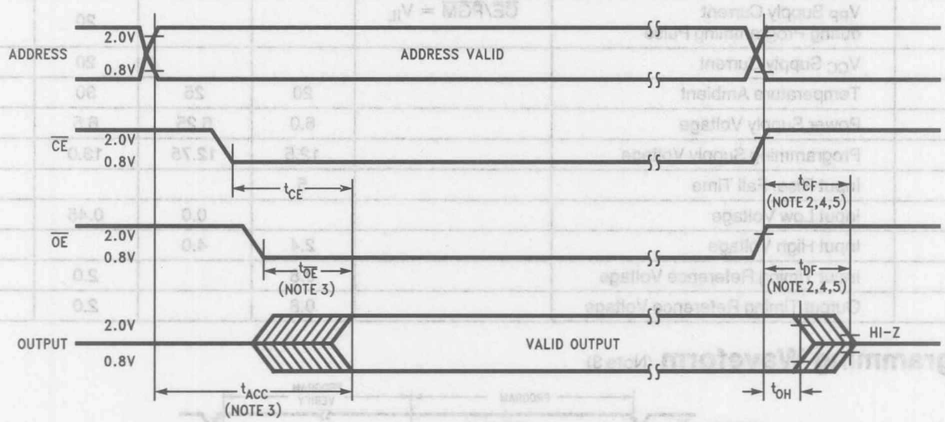
Capacitance $T_A = +25°C$, $f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	9	15	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	15	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤ 5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6, 7, and 9)



TL/D/11377–3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) − 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.2 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

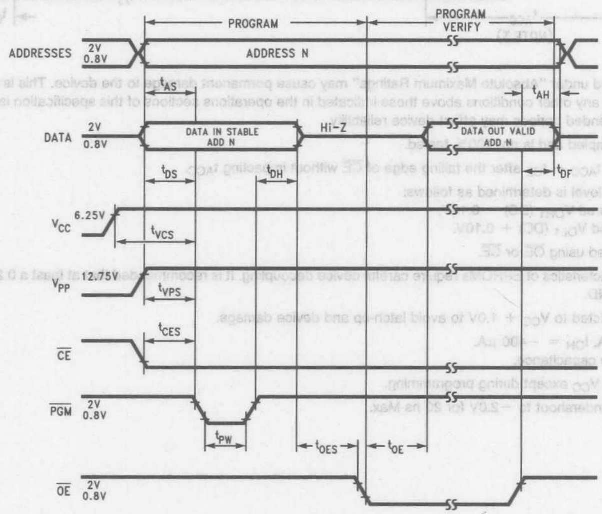
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			20	mA
I_{CC}	V_{CC} Supply Current				20	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveform (Note 3)



TL/D/11377-4

Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart

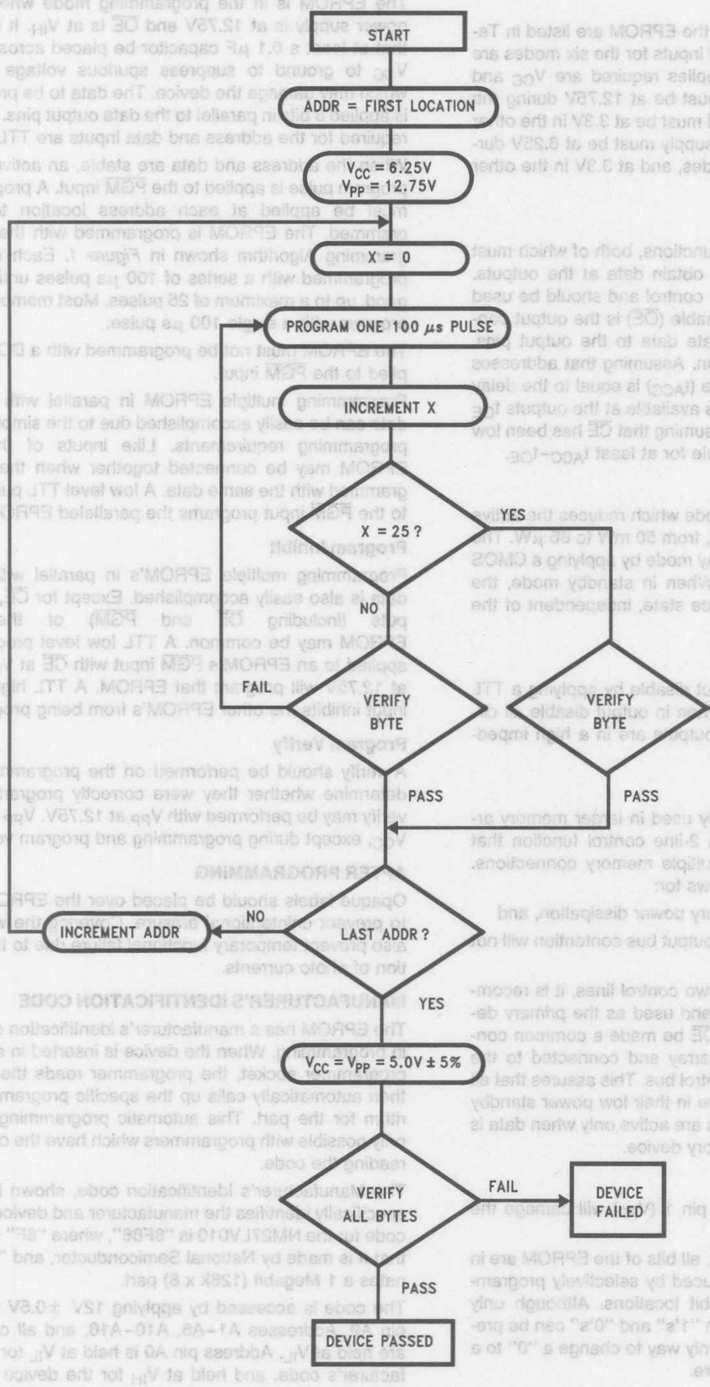


FIGURE 1

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{\text{CE}}$) is the power control and should be used for device selection. Output Enable ($\overline{\text{OE}}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{\text{CE}}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{\text{OE}}$, assuming that $\overline{\text{CE}}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 50 mW to 66 μW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{\text{CE}}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{\text{OE}}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{\text{OE}}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{\text{CE}}$ be decoded and used as the primary device selecting function, while $\overline{\text{OE}}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

power supply is at 12.75V and $\overline{\text{CE}}$ is at V_{IL}. It is required that at least a 0.1 μF capacitor be placed across V_{PP} and V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{\text{PGM}}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{\text{PGM}}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{\text{PGM}}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{\text{CE}}$, all like inputs (including $\overline{\text{OE}}$ and $\overline{\text{PGM}}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{\text{PGM}}$ input with $\overline{\text{CE}}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{\text{CE}}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27LV010 is "8F86", where "8F" designates that it is made by National Semiconductor, and "86" designates a 1 Megabit (128k x 8) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O0–O7. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 30W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

Mode Selection

The modes of operation of the NM27LV010 are listed in Table I. A single 3.3V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X	V_{CC}	3.3V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	X	V_{CC}	3.3V	High Z
Standby	V_{IH}	X	X	V_{CC}	3.3V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	12.75V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (12)	A9 (26)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	1	0	86

National Semiconductor

PRELIMINARY

NM27LV210
1,048,576-Bit (64K x 16) Low Voltage EPROM

General Description

The NM27LV210 is a high performance Low Voltage Electrical Programmable read only memory. It is manufactured using National's latest EPROM technology. This technology allows the part to operate at speeds as fast as 150 ns over industrial temperatures (−40°C to +85°C).

This Low Voltage and Low Power EPROM is designed with power sensitive hand held and portable battery products in mind. This allows for code storage of firmware for applications like notebook computers, palm top computers, cellular phones, and HDD.

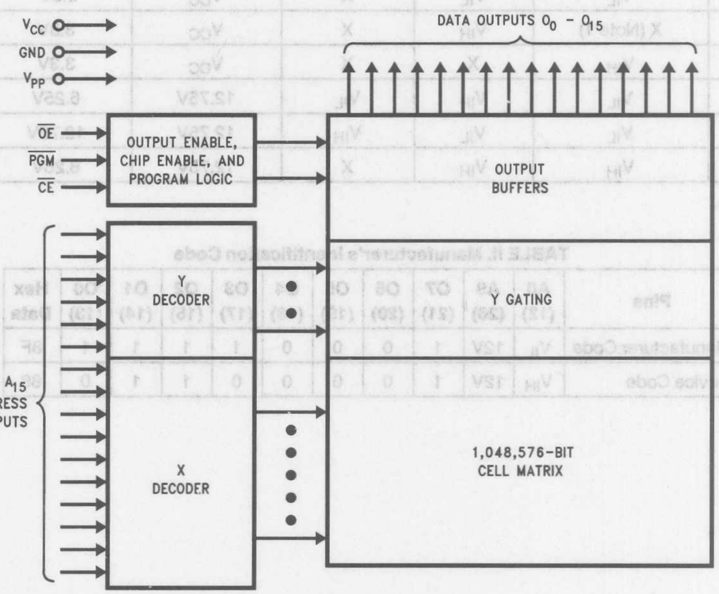
Small outline packages are just as critical to portable applications as Low Voltage and Low Power. National Semiconductor has foreseen this need and provides windowed CERQUAD for prototyping and software development, PLCC for production runs, and TQFP for PC board sensitive users.

The NM27LV210 is one member of National's growing Low Voltage product family.

Features

- 3.0V to 3.6V operation
- 150 ns maximum access time
- Low current operation
  - — 20 mA I_{CC} active current @ 5 MHz
  - — 20 μA I_{CC} standby current @ 5 MHz
- Ultra low power operation
  - — 66 μW standby power @ 3.3V
  - — 66 mW active power @ 3.3V
- Surface mount package options
  - — 44-Pin PLCC
  - — 44 Pin TQFP

Block Diagram



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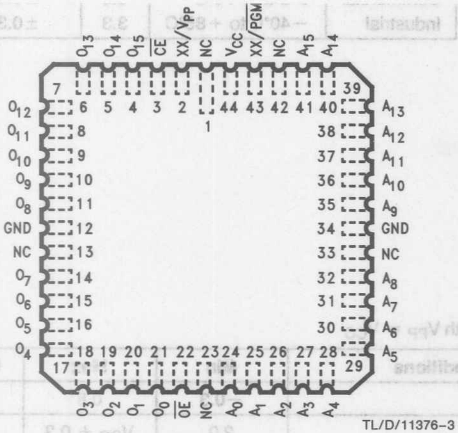
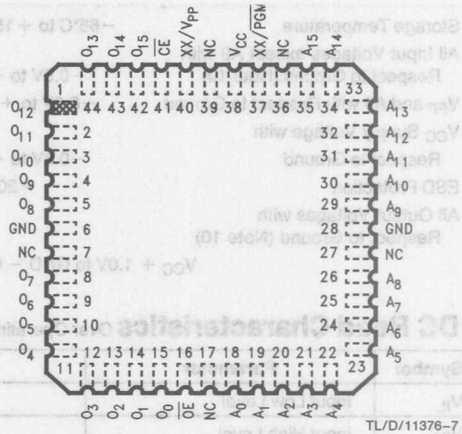


Top View



Top View

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 3.3V ±0.3%

Parameter/Order Number	Access Time (ns)
NM27LV210 V, F, 150	150
NM27LV210 V, F, 200	200
NM27LV210 V, F, 250	250

Industrial Temperature Range (−40°C to +85°C)
V_{CC} = 3.3V ±0.3%

Parameter/Order Number	Access Time (ns)
NM27LV210 VE, FE, 150	150
NM27LV210 VE, FE, 200	200
NM27LV210 VE, FE, 250	250

Note: Surface mount PLCC package available for commercial and extended temperature ranges only.

Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O15	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)
NC	No Connect
V_{PP}	Programming Voltage

Package Types: NM27LV210 C, V, F

V = PLCC package

F = TQFP package

C = Quartz—Windowed LCC package

- All packages conform to JEDEC standard.
- All versions are guaranteed to function in slower applications.
- Consult the NSC representative for newly released products/packages.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}	Tolerance
Commercial	0°C to +70°C	3.3	±0.3
Industrial	−40°C to +85°C	3.3	±0.3

DC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Test Conditions		Min	Max	Units
V_{IL}	Input Low Level			−0.3	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage (TTL)				0.4	V
V_{OH1}	Output High Voltage (TTL)			2.4		V
V_{OL2}	Output Low Voltage (CMOS)				0.3	V
V_{OH2}	Output High Voltage (CMOS)			V_{CC} − 0.3		V
I_{SB1}	V_{CC} Standby Current (TTL)	$\overline{CE} = V_{IH}$			100	µA
I_{SB2}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC} \pm 0.3V$			20	µA
I_{CC}	V_{CC} Active Current	$\overline{CE} = \overline{OE} = V_{IL}$, I/O = 0 µA	f = 5 MHz		20	mA
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$			10	µA
I_{LI}	Input Load Current	V_{IN} = 3.3 or GND		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 3.3V or GND		−1	1	µA

AC Read Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	150		200		250		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		65		70		75	ns
t_{DF} (Note 2)	Output Disable to Output Float	0	50	0	50	0	60	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		ns

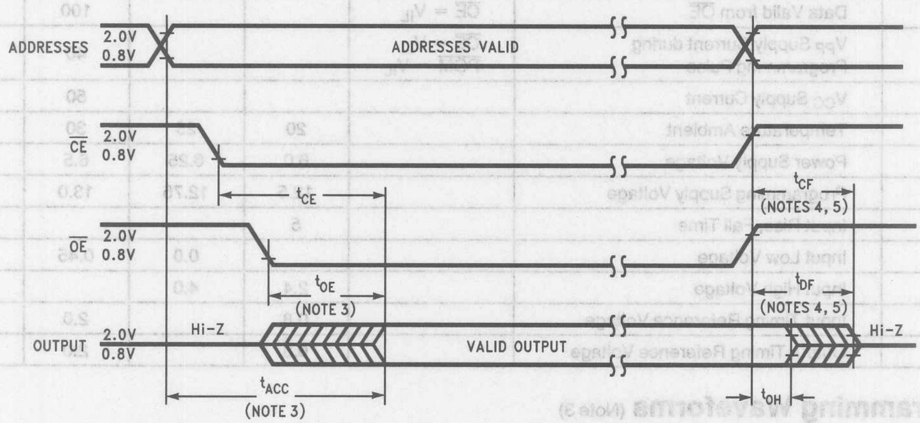
Capacitance $T_A = +25°C$, f = 1 MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	12	20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	13	20	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Timing Measurement Reference Level	
		Inputs	0.8V and 2V
Input Rise and Fall Times	≤ 5 ns	Outputs	0.8V and 2V
Input Pulse Levels	0.45V to 2.4V		

AC Waveforms (Notes 6, 7, & 9)



TL/D/11376–4

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{OH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

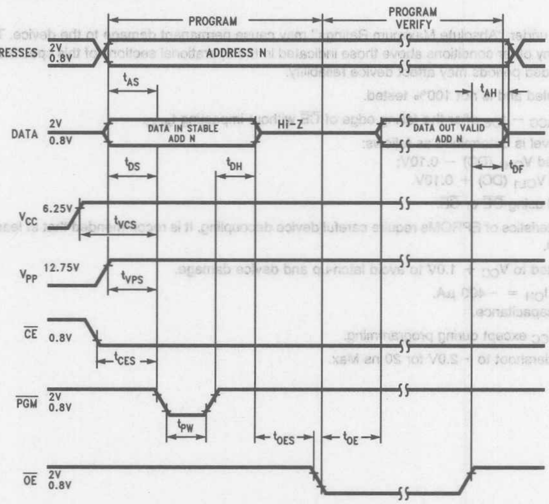
Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

3

Programming Characteristics (Notes 1, 2, 3, 4 & 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{CES}	$\overline{CE}$ Setup Time	$\overline{OE} = V_{IH}$	1			µs
t_{DS}	Data Setup Time		1			µs
t_{VPS}	V_{PP} Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			100	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IL}$			40	mA
I_{CC}	V_{CC} Supply Current				50	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6.0	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13.0	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



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Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

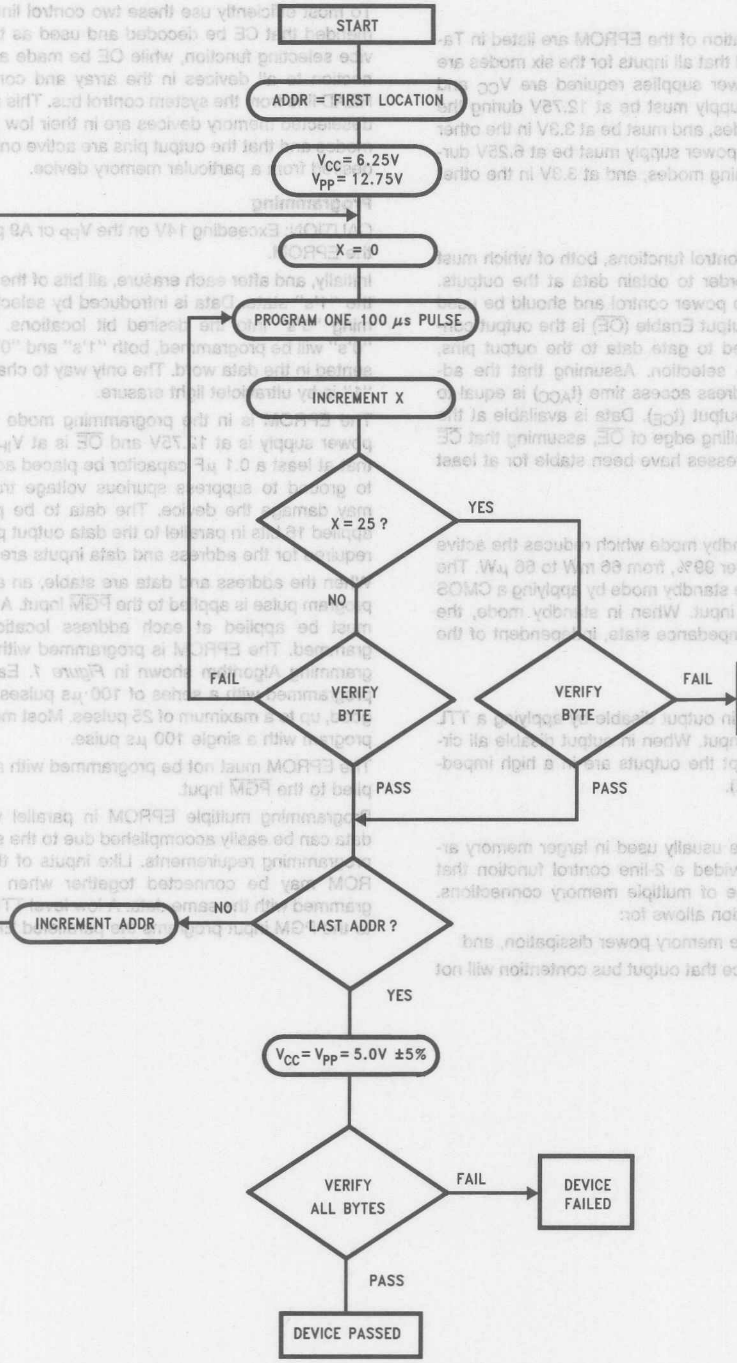
Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

Fast Programming Algorithm Flow Chart



TL/D/11376–6

FIGURE 1

3

Functional Description

DEVICE OPERATION

The six modes of operation of the EPROM are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 3.3V in the other three modes. The V_{CC} power supply must be at 6.25V during the three programming modes, and at 3.3V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 99%, from 66 mW to 66 μW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that CE be decoded and used as the primary device selecting function, while OE be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on the V_{PP} or A9 pin will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Fast Programming Algorithm shown in *Figure 1*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the PGM input programs the paralleled EPROM.

Programming multiple EPROM's in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel EPROM may be common. A TTL low level program pulse applied to an EPROM's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 12.75V will program that EPROM. A TTL high level $\overline{CE}$ input inhibits the other EPROM's from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 12.75V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for the NM27LV210 is "8FD6", where "8F" designates that it is made by National Semiconductor, and "D6" designates a 1 Megabit (64K x 16) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A_9. Addresses A_1–A_8, A_{10}–A_{15}, and all control pins are held at V_{IL}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the lower eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 30W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp (if distance is doubled the erasure time increases by factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance has changed, or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X (Note 1)	X	3.3V	D_{OUT}
Output Disable	X	V_{IH}	X	X	3.3V	High Z
Standby	V_{IH}	X	X	X	3.3V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	12.75V	6.25V	D_{OUT}
Program Inhibit	V_{IH}	X	X	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

TABLE II. Manufacturer's Identification Code

Pins	A0 (21)	A9 (31)	O_7 (12)	O_6 (13)	O_5 (14)	O_4 (15)	O_3 (16)	O_2 (17)	O_1 (18)	O_0 (19)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	1	0	1	1	0	D6

National Semiconductor

Low Current EPROM Selection Guide

General Description

National Semiconductor's family of low current EPROMs are devices that consume extremely low current in both active and standby modes. These Power Miser products are ideal for battery powered portables and hand-held systems, and for systems using "in-line" power. There are three devices offered in the JEDEC pinout: the NM27LC64, NM27LC256, and the NM27LC512.

Features

- Lower CMOS Power Consumption
  - 5V operation
  - 8.0 mA (max) active
  - 100 μA (max) standby
- JEDEC standard pin configuration
- High reliability with EPI processing
  - Latch-up immunity to 200 mA
  - ESD protection >2000V
- Manufacturer's identification code

Available Product

	Packages	Temperature Ranges
NM27LC64	Q, N	C, E
NM27LC256	Q, N	C, E
NM27LC512	Q, N, V, T	C, E

National Semiconductor

NM27LC64
65,536-Bit (8k x 8) Low Current CMOS EPROM

General Description

The NM27LC64 is a 8k x 8 EPROM manufactured on a proven, manufacturable CMOS process, consuming extremely low current in both the active and standby modes. The NC27LC64 consumes a mere 12.5 mW (typical) in CMOS, and 25 mW (typical) in TTL, at 3 MHz.

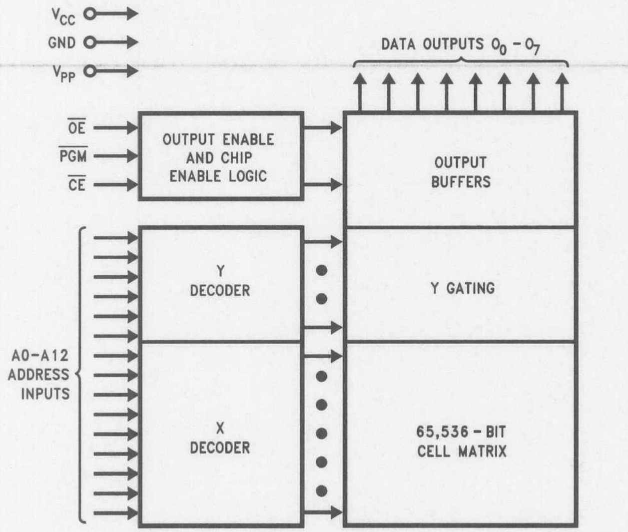
The NM27LC64 is one among a family of Power Miser (PM) products from National Semiconductor catering to the increasing low current demands of the market.

Offered in the JEDEC Pinout, this device is a replacement for high power devices, while also providing an upgrade path to higher densities.

Features

- Low power consumption
  - — 5V operation
  - — 4.5 mA (max) active
  - — 100 μA (max) standby
- 170 ns access time
- High reliability with EPI processing
  - — Latch-up immunity to 200 mA
  - — ESD protection exceeds 2000V
- JEDEC standard pin configuration
- Silicon Signature
- Manufacturer's identification code

Block Diagram



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Pin Names

Symbol	Description
A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O0–O7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (during Read)

27C512	27C256	27C64	NM27LC64	Pin	Pin	NM27LC64	27C64	27C256	27C512
A16									XX/$\overline{PGM}$
A15	A15	V_{PP}	V_{PP}	1	28	V_{CC}	V_{CC}	V_{CC}	XX
A12	A12	A12	A12	2	27	$\overline{PGM}$	A14	A14	A14
A7	A7	A7	A7	3	26	NC	A13	A13	A13
A6	A6	A6	A6	4	25	A8	A8	A8	A8
A5	A5	A5	A5	5	24	A9	A9	A9	A9
A4	A4	A4	A4	6	23	A11	A11	A11	A11
A3	A3	A3	A3	7	22	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/V_{PP}	$\overline{OE}$
A2	A2	A2	A2	8	21	A10	A10	A10	A10
A1	A1	A1	A1	9	20	$\overline{CE}$	$\overline{CE}$/PGM	$\overline{CE}$/PGM	$\overline{CE}$
A0	A0	A0	A0	10	19	O7	O7	O7	O7
O0	O0	O0	O0	11	18	O6	O6	O6	O6
O1	O1	O1	O1	12	17	O5	O5	O5	O5
O2	O2	O2	O2	13	16	O4	O4	O4	O4
GND	GND	GND	GND	14	15	O3	O3	O3	O3

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Note: Compatible EPROM pin configurations are shown in the blocks adjacent to the NM27LC64 pins.

Commercial Temperature Range (0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC64 Q, N, 120	120
NM27LC64 Q, N, 150	150
NM27LC64 Q, N, 200	200

Extended Temperature Range (−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC64 QE, NE, 120	120
NM27LC64 QE, NE, 150	150
NM27LC64 QE, NE, 200	200

Ordering Information

NM 27 LC 64 Q E 200

- **NM** — **National Memory**
- **27** — **EPROM**
- **LC** — **Low Current**
- **64** — **Size**
  - 64 = 64k
  - 256 = 256k
  - 512 = 512k
- **Q** — **Package**
  - Q = Ceramic DIP
  - N = Plastic DIP, OTP
- **E** — **Operating Temperature Range**
  - Blank = Commercial
  - E = Extended
- **200** — **Access Time**
  - 200 = 200 ns

3

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−55°C to +125°C
Storage Temperature	−65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to −0.6V
All Output Voltages with Respect to Ground (Note 10)	V_{CC} + 1.0V to GND −0.6V
V_{PP} Supply Voltage and A9 with Respect to Ground During Programming	+14.0V to −0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to −0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	+5V ±10%
Industrial	−40°C to +85°C	+5V ±10%

READ OPERATION

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Conditions		Min	Type	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND				10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$				10	μA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f = 3 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA	Comm'l		5	6.3	mA
			Ind'l		5	7	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 3 MHz Inputs = V_{CC} or GND, I/O = 0 mA, (*Figures 1* and *2*)	Comm'l		2	3	mA
			Ind'l		2	3.5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$			0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$			0.5	100	μA
I_{PP}	V_{PP} Load Current	$V_{PP} = V_{CC}$				10	μA
V_{IL}	Input Low Voltage			−0.1		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA		2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA				0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA		V_{CC} − 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	150		200		250		Units
			Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60		70	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		0		ns

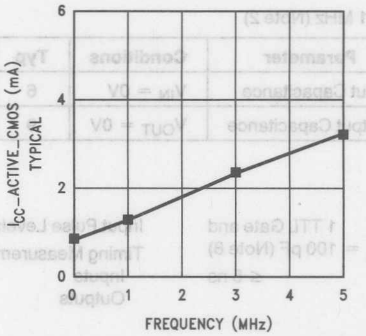


FIGURE 1. I_{CC}—Active—CMOS vs Frequency
$V_{CC} = V_{PP} = 5.0V$, Temperature = 25°C

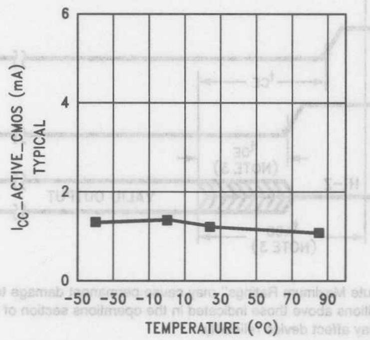


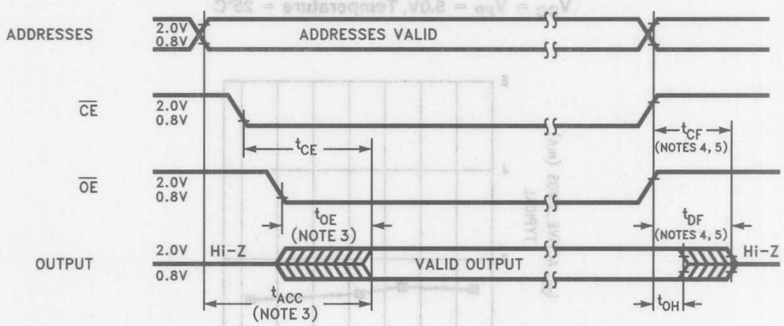
FIGURE 2. I_{CC}—Active—CMOS vs Temperature
$V_{CC} = V_{PP}$ 5.0V, Frequency = 1 MHz

C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	≤ 5 ns	Timing Measurement Reference Level	(Note 10)
		Inputs	0.8V and 2.0V
		Outputs	0.8V and 2.0V

AC Waveforms (Notes 6, 7 and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE®, the measured V_{CH1} (DC) $-$ 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) $+$ 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA.
$C_L = 100$ pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

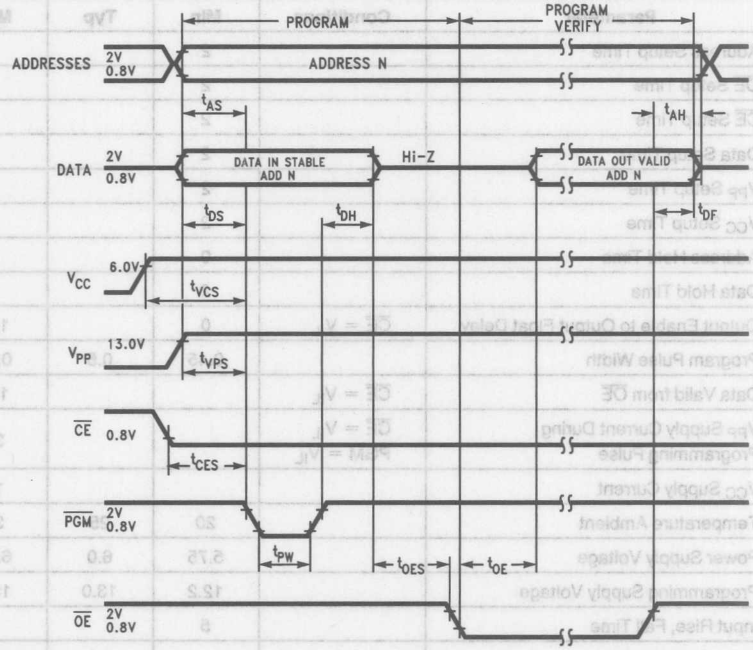
Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Note 11: CMOS inputs: V_{IL} = GND $\pm$0.3V, $V_{IH} = V_{CC}$ $\pm$0.3V.

t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{CES}	$\overline{CE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2.0	V

3

Programming Waveforms (Note 3)



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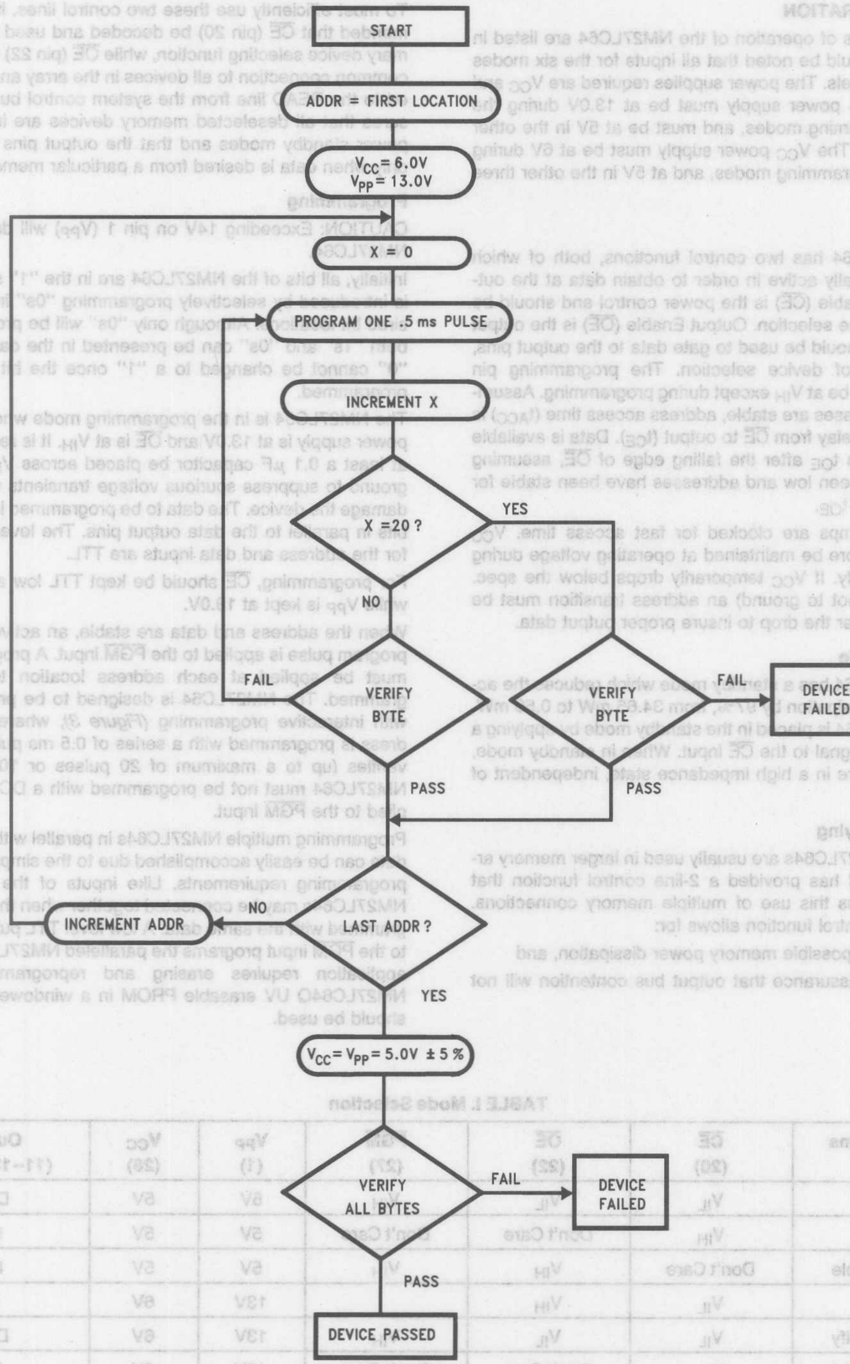
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings.

Interactive Programming Algorithm Flow Chart



TL/D/11421–7

FIGURE 3

The six modes of operation of the NM27LC64 are listed in Table I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NM27LC64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NM27LC64 has a standby mode which reduces the active power dissipation by 97%, from 34.65 mW to 0.55 mW. The NM27LC64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NM27LC64s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

mended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NM27LC64.

Initially, all bits of the NM27LC64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed.

The NM27LC64 is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 13.0V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NM27LC64 is designed to be programmed with interactive programming *(Figure 3)*, where each address is programmed with a series of 0.5 ms pulses until it verifies (up to a maximum of 20 pulses or 10 ms). The NM27LC64 must not be programmed with a DC signal applied to the $\overline{PGM}$ input.

Programming multiple NM27LC64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NM27LC64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NM27LC64s. If an application requires erasing and reprogramming, the NM27LC64Q UV erasable PROM in a windowed package should be used.

TABLE I. Mode Selection

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}		13V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13V	6V	Hi-Z

puts (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NM27LC64 may be common. A TTL low level program pulse applied to an NM27LC64's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NM27LC64. A TTL high level $\overline{CE}$ input inhibits the other NM27LC64s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NM27LC64 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NM27LC64 is "8FC2", where "8F" designates that it is made by National Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V $\pm$ 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C $\pm$ 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NM27LC64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming, opaque labels should be placed over the NM27LC64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NM27LC64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2

National Semiconductor

NM27LC256

262,144-Bit (32k x 8) Low Current CMOS EPROM

General Description

The NM27LC256 is a 32k x 8 EPROM manufactured on a proven, manufacturable CMOS process, consuming extremely low current in both the active and standby modes. The NM27LC256 consumes a mere 17.5 mW, (typical) making it ideal for battery powered portable and hand held systems, and for systems using "in-line" power.

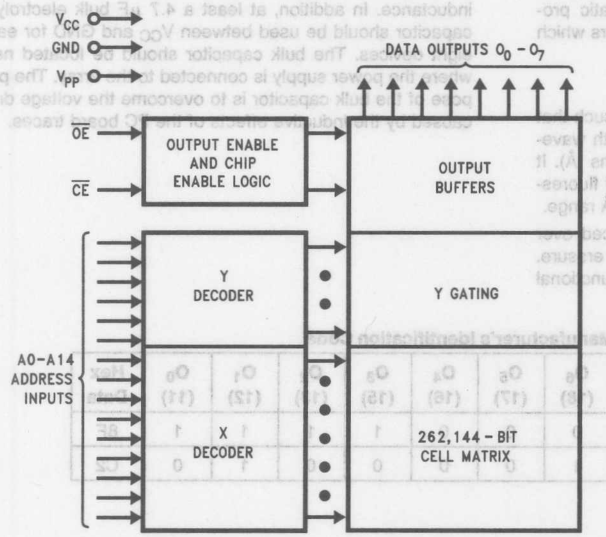
The NM27LC256 is one among a family of Power Miser products from National Semiconductor catering to the increasing low current demands of the market.

Offered in the JEDEC Pinout, the NM27LC256 offers a viable alternative to the user as a replacement for existing high power devices, while also providing an upgrade path to higher densities.

Features

- Low power consumption
  - 5V operation
  - 4.5 mA (max) active
  - 100 μA (max) standby
- 200 ns access time
- JEDEC standard pinout
- Manufacturer's identification code

Block Diagram



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Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

Connection Diagrams

27LC010	27LC512	27LC64
XX/V_{PP}		
A16		
A15	A15	V_{PP}
A12	A12	A12
A7	A7	A7
A6	A6	A6
A5	A5	A5
A4	A4	A4
A3	A3	A3
A2	A2	A2
A1	A1	A1
A0	A0	A0
O0	O0	O0
O1	O1	O1
O2	O2	O2
GND	GND	GND

DIP
NM27LC256

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27LC64	27LC512	27LC010
		V_{CC}
		XX/PGM
V_{CC}	V_{CC}	XX
$\overline{PGM}$	A14	A14
NC	A13	A13
A8	A8	A8
A9	A9	A9
A11	A11	A11
$\overline{OE}$	$\overline{OE}/V_{PP}$	$\overline{OE}$
A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O7	O7	O7
O6	O6	O6
O5	O5	O5
O4	O4	O4
O3	O3	O3

Note: Compatible EPROM plan configurations are shown in the blocks adjacent to the NM27LC256 plan

Commercial Temperature Range
(0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC256 Q, 200	200
NM27LC256 Q, 250	250

Extended Temperature Range
(−40°C to +85°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC256 QE, 200	200
NM27LC256 QE, 250	250

Ordering Information

NM 27 LC 256 Q E 200

- **National Memory** — NM
- **EPROM** — 27
- **Low Current** — LC
- **Size** — 256
  - 64 = 64k
  - 256 = 256k
  - 512 = 512k
- **Package** — Q
  - Q = Ceramic DIP
- **Operating Temperature Range** — E
  - E = Extended Temperature
  - Blank = Commercial Temperature
- **Access Time** — 200
  - 200 = 200 ns
  - 250 = 250 ns

Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.6V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V

Respect to Ground V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	5V ±10%
Industrial	−40°C to +85°C	5V ±10%

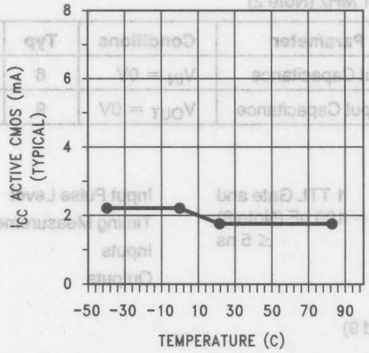
Read Operation

DC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Level			−0.1		0.8	V
V_{IH}	Input High Level			2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA				0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 μA		2.4			V
I_{SB1}	V_{CC} Standby Current (CMOS)	$\overline{CE} = V_{CC}$ ±0.3V			0.5	100	μA
I_{SB2}	V_{CC} Standby Current	$\overline{CE} = V_{IH}$			0.1	1.0	mA
I_{CC1}	V_{CC} Active Current TTL Inputs	$\overline{CE} = \overline{OE}$ V_{IL}, F = 3 MHz Inputs V_{IH} or V_{IL}	Com'l		8.0	11.0	mA
			Ind'l		8.0	12.0	
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, F = 3 MHz Inputs = V_{CC} or GND, I/O = 0 mA (See *Figures 1, 2*)	Com'l		3.5	5.5	mA
			Ind'l		3.5	6.0	
I_{PP}	V_{PP} Supply Current	$V_{PP} = V_{CC}$				10	μA
V_{PP}	V_{PP} Read Voltage			V_{CC}−0.7		V_{CC} + 0.7	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1		1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10		10	μA

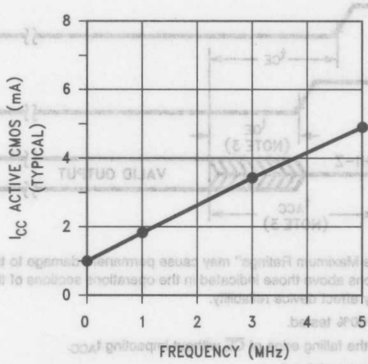
AC Electrical Characteristics Over Operating Range with $V_{PP} = V_{CC}$

Symbol	Parameter	200		250		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		200		250	ns
t_{OE}	$\overline{OE}$ to Output Delay		75		100	ns
t_{DF} (Note 2)	Output Disable to Output Float		60		60	ns
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First	0		0		ns



TL/D/11405–3

FIGURE 1. I_{CC}_ACTIVE_CMOS vs Temperature $V_{CC} = V_P = 5.0V$, Frequency 1 MHz



TL/D/11405–4

FIGURE 2. I_{CC}_ACTIVE_CMOS vs Frequency $V_{CC} = V_{PP} = 5.0V$, Temperature = 25°C

3

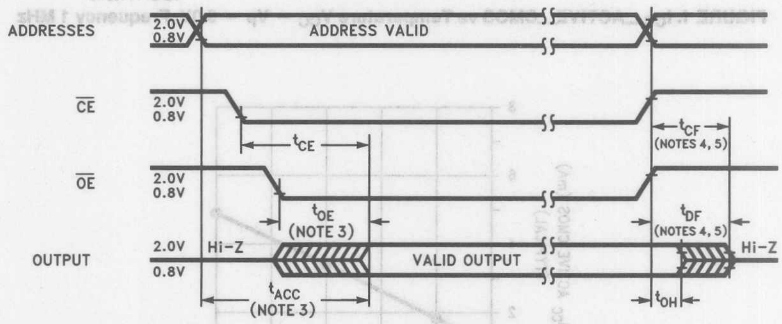
Capacitance $T_A = +25°C$, $1 = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Input Pulse Level	0.45V to 2.4V
Input Pulse Levels	≤ 5 ns	Timing Measurement Level (Note 10)	(Note 10)
		Inputs	0.8V to 2V
		Outputs	0.8V to 2V

AC Waveforms (Notes 6, 7, and 9)



TL/D/11405-5

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The T_{DF} and T_{CF} compare level is determined as follows:
High to TRI-STATE®, the measure V_{CH1} (DC) − 0.10V;
Low to TRI-STATE, the measure V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ μA, C_L: 100 pF includes fixture capacitance.

Note 9: V_{PP} may be connected to V_{CC} except during programming.

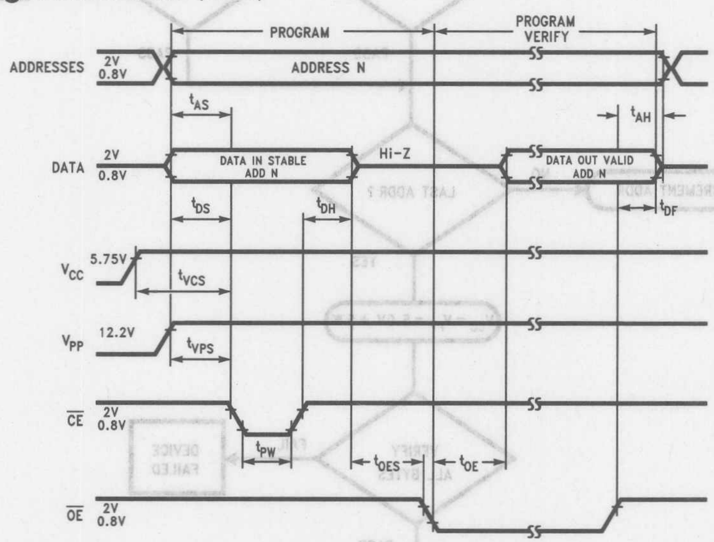
Note 10: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 11: CMOS inputs V_{IL} = GND ±0.3V, $V_{IH} = V_{CC}$ ± 0.3V.

Programming Characteristics (Notes 1, 2, 3, 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			μs
t_{OES}	$\overline{OE}$ Setup Time		2			μs
t_{DS}	Data Setup Time		2			μs
t_{VPS}	V_{PP} Setup Time		2			μs
t_{VCS}	V_{CC} Setup Time		2			μs
t_{AH}	Address Hold Time		0			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/\overline{PGM} = V_{IL}$	0		130	ns
t_{PW}	Program Pulse Width		0.45	0.5	0.55	ms
$t_{\overline{OE}}$	Data Valid from $\overline{OE}$	$\overline{CE}/\overline{PGM} = V_{IL}$			150	ns
I_{PP}	V_{PP} Supply Current during Programming Pulse	$\overline{CE}/\overline{PGM} = V_{IL}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_A	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		5.75	6.0	6.25	V
V_{PP}	Programming Supply Voltage		12.2	13.0	13.3	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0.0	0.45	V
V_{IH}	Input High Voltage		2.4	4.0		V
t_{IN}	Input Timing Reference Voltage		0.8		2.0	V
t_{OUT}	Output Timing Reference Voltage		0.8		2.0	V

Programming Waveforms (Note 3)



TL/D/11405–6

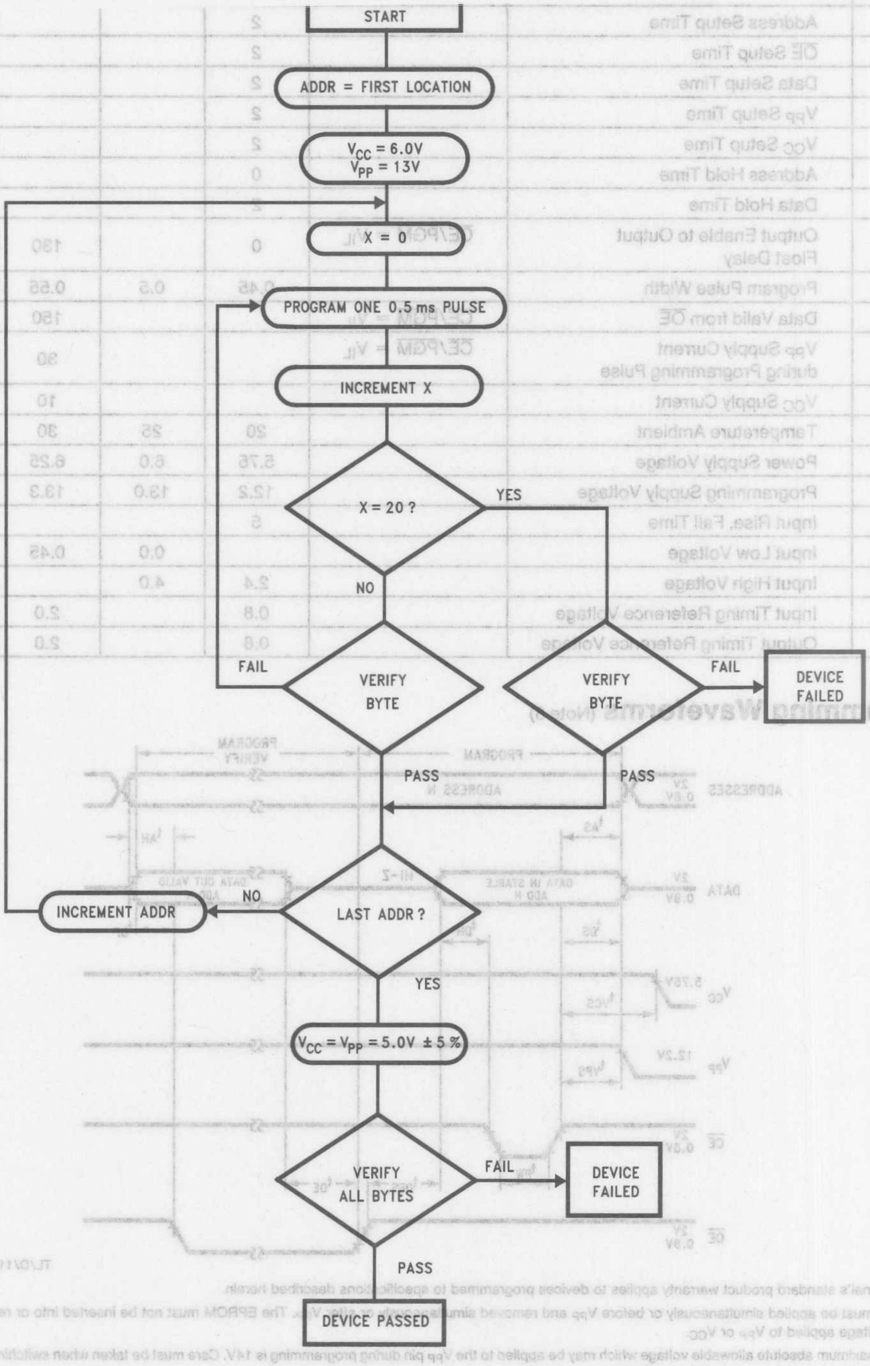
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the spurious V_{PP} voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the Interactive Program Algorithm, at typical power supply voltages and timings.

Note 5: During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.



TL/D/11405–7

FIGURE 3

ble I. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 13.0V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6.0V during the three programming modes, and at 5V in the other three modes.

Read Mode

The EPROM has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The EPROM has a standby mode which reduces the active power dissipation by over 97%, from 24.75 mW to 0.55 mW. The EPROM is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output Disable

The EPROM is placed in output disable by applying a TTL high signal to the $\overline{OE}$ input. When in output disable all circuitry is enabled, except the outputs are in a high impedance state (TRI-STATE).

Output OR-Tying

Because the EPROM is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

vice selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming; Interactive Algorithm

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the EPROM.

Initially, and after each erasure, all bits of the EPROM are in the "1's" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The EPROM is in the programming mode when the V_{PP} power supply is at 13.0V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. The EPROM is programmed with the Interactive Programming Algorithm shown in *Figure 3*. Each Address is programmed with a series of 500 μs pulses until it verifies good, up to a maximum of 20 pulses. Most memory cells will program with a single 500 μs pulse.

The EPROM must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple EPROM in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the parallel EPROM may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled EPROM.

Program Inhibit

Programming multiple EPROMs in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel EPROMs may be common. A TTL low level program pulse applied to an EPROMs $\overline{CE}$ input with V_{PP} at 13.0V will program that EPROM. A TTL high level $\overline{CE}/\overline{PGM}$ input inhibits the other EPROM from being programmed.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{CC}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	X	13V	6.0V	D_{IN}
Program Verify	X	V_{IL}	13V	6.0V	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	13V	6.0V	High Z

Note 1: X can be V_{IL} or V_{IH}.

Functional Description (Continued)

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

AFTER PROGRAMMING

Opaque labels should be placed over the EPROM window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

MANUFACTURER'S IDENTIFICATION CODE

The EPROM has a manufacturer's identification code to aid in programming. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

The Manufacturer's Identification code, shown in Table II, specifically identifies the manufacturer and device type. The code for NM27LC256 is "8FC4", where "8F" designates that it is made by National Semiconductor, and "C4" designates a 256k (32k8) part.

The code is accessed by applying 12V $\pm$0.5V to address pin A9. Addresses A1–A8, A10–A16, and all control pins are held at V_{IH}. Address pin A0 is held at V_{IL} for the manufacturer's code, and held at V_{IH} for the device code. The code is read on the eight data pins, O_0–O_7. Proper code access is only guaranteed at 25°C to $\pm$5°C.

ERASURE CHARACTERISTICS

The erasure characteristics of the device are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

The recommended erasure procedure for the EPROM is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity $\times$ exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The EPROM should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to device should be maintained at one inch. The erasure time increases as the square of the distance from the lamp. (If distance is doubled the erasure time increases by factor of 4.) Lamps lose intensity as they age. When a lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristic of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent of the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	1	0	0	0	1	0	0	C4

National Semiconductor

NM27LC512
524,288-Bit (64k x 8) Low Current CMOS EPROM

General Description

The NM27LC512 is a 64k x 8 EPROM manufactured on a proven, manufacturable CMOS process, consuming extremely low current in both the active and standby modes. The NM27LC512 consumes a mere 30 mW, making it ideal for portable and hand held computers, data acquisition and medical equipment, and for systems using in-line power.

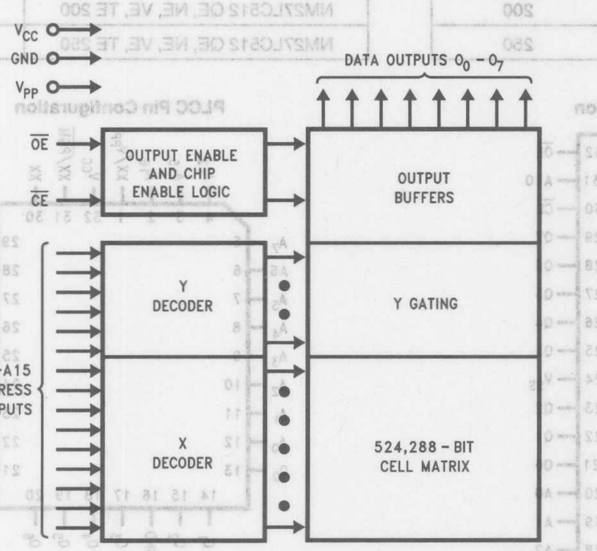
The NM27LC512 is one among a family of Power Miser products from National Semiconductor catering to the increasing low current demands of the market.

Offered in a JEDEC Standard Pinout, the NM27LC512 offers a viable alternative to the user as a replacement for existing high power devices, while also providing an upgrade path from lower densities.

Features

- Low CMOS power consumption
  - 5V operation
  - 8.0 mA (Max) active
  - 100 μA (Max) standby
- 150 ns access time
- JEDEC standard pin configuration
- Manufacturer's identification code

Block Diagram



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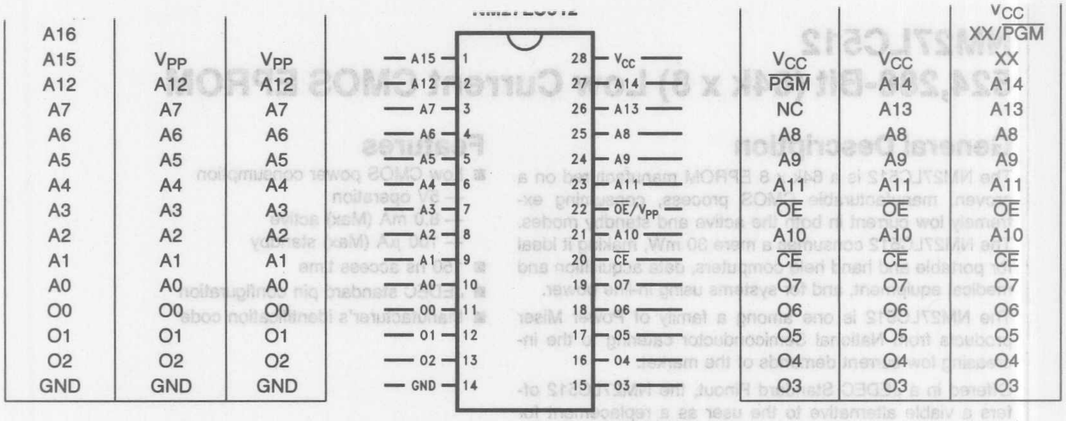
Pin Names

A0–A15	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}/V_{PP}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
XX	Don't Care (During Read)

3



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Note: Compatible EPROM plan configurations are shown in the blocks adjacent to the NM27LC512 plan.

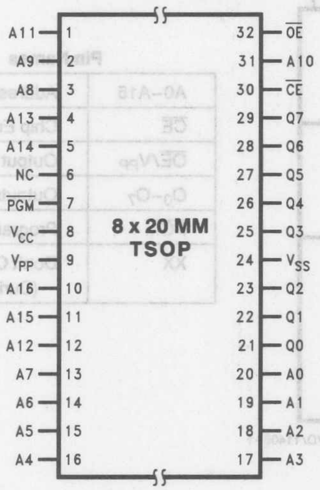
Commercial Temperature Range
(0°C to +70°C)
V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NM27LC512 Q, N, V, T 150	150
NM27LC512 Q, N, V, T 200	200
NM27LC512 Q, N, V, T 250	250

Extended Temperature Range
(−40°C to +85°C)
V_{CC} = 5V ± 10%

Parameter/Order Number	Access Time (ns)
NM27LC512 QE, NE, VE, TE 150	150
NM27LC512 QE, NE, VE, TE 200	200
NM27LC512 QE, NE, VE, TE 250	250

TSOP Pin Configuration



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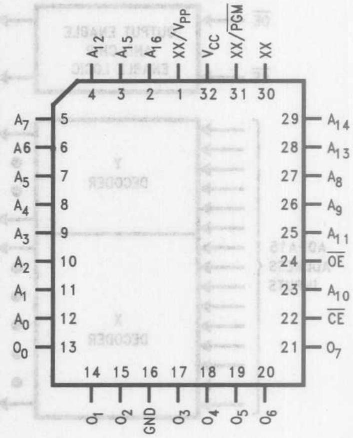
PLCC Pin Configuration



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
All Input Voltages Except A9 with Respect to Ground	−0.6V to +7V
V_{PP} and A9 with Respect to Ground	−0.7V to +14V
V_{CC} Supply Voltage with Respect to Ground	−0.6V to +7V
ESD Protection	>2000V
All Output Voltages with Respect to Ground	V_{CC} + 1.0V to GND − 0.6V

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%

Read Operation

DC Electrical Characteristics Over Operating Range

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Level			−0.2		0.8	V
V_{IH}	Input High Level			2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA				0.4	V
V_{OH}	Output High Voltage	I_{OH} = −2.5 mA		3.5			V
I_{SB1}	V_{CC} Standby Current CMOS Inputs	$\overline{CE}$ = V_{CC} ± 0.3V		0.5	50	100	μA
I_{SB2}	V_{CC} Standby Current TTL Inputs	$\overline{CE}$ = V_{IH}		0.1	0.4	1.0	mA
I_{CC1}	V_{CC} Active Current TTL Inputs	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, f = 3 MHz Inputs = V_{IH} or V_{IL}	Comm'l		11.0	15	mA
			Ind'l		11.0	15	
I_{CC2}	V_{CC} Active Current CMOS Inputs	$\overline{CE}$ = GND, f = 3 MHz Inputs = V_{CC} or GND, I/O = 0 mA (Refer to *Figures 1, 2*)			6.5	10	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}				10	μA
I_{LI}	Input Load Current	V_{IN} = 5.5V or GND		−1		1	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or GND		−10		10	μA

AC Electrical Characteristics Over Operating Range

Symbol	Parameter	150		200		250		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE}	$\overline{CE}$ to Output Delay		150		200		250	
t_{OE}	$\overline{OE}$ to Output Delay		60		75		100	
t_{DF} (Note 2)	Output Disable to Output Float		50		55		60	
t_{OH} (Note 2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever Occurred First	0		0		0		

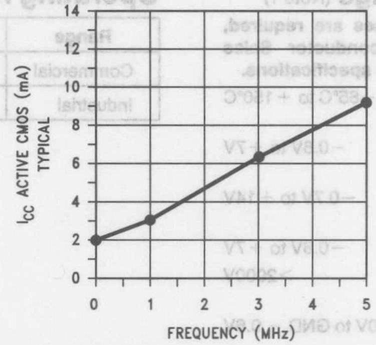

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FIGURE 1. I_{CC}—ACTIVE—CMOS vs Frequency
V_{CC} = 5.0V, Temperature = 25°C

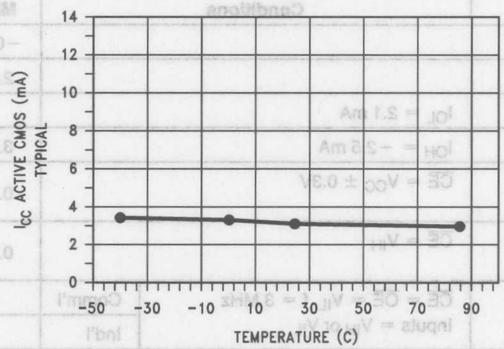

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FIGURE 2. I_{CC}—ACTIVE—CMOS vs Temperature
V_{CC} = 5.0V, Frequency = 1 MHz

3

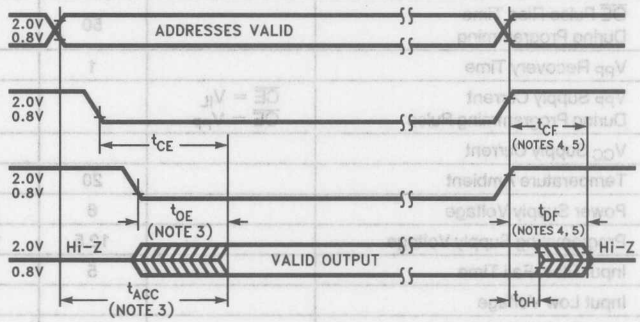
Capacitance $T_A = +25°C$, $f = 1$ MHz (Note 2)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	9	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF (Note 8)	Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	≤ 5 ns	Timing Measurement Reference Level	(Note 9)
		Inputs	0.8V to 2V
		Outputs	0.8V to 2V

AC Waveforms (Notes 6, 7, and 9)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operations sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The T_{DF} and T_{CF} compare level is determined as follows:
High to TRI-STATE®, the measure V_{CH1} (DC) − 0.10V;
Low to TRI-STATE, the measure V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: $I_{OL} = 1.6$ mA, $I_{OH} = -400$ µA.
C_L: 100 pF includes fixture capacitance.

Note 9: Inputs and outputs can undershoot to −2.0V for 20 ns Max.

Note 10: CMOS inputs V_{IL} = GND ±0.3V, $V_{IH} = V_{CC}$ ± 0.3V.

t_{AS}	Address Setup Time		1			µs
t_{OES}	$\overline{OE}$ Setup Time		1			µs
t_{DS}	Data Setup Time		1			µs
t_{VCS}	V_{CC} Setup Time		1			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		1			µs
t_{cf}	Chip Enable to Output Float Delay	$\overline{OE} = V_{IL}$	0		60	ns
t_{PW}	Program Pulse Width		95	100	105	µs
t_{OEH}	$\overline{OE}$ Hold Time		1			µs
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE} = V_{IL}$			250	ns
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			ns
t_{VR}	V_{PP} Recovery Time		1			µs
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{PP}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
T_R	Temperature Ambient		20	25	30	°C
V_{CC}	Power Supply Voltage		6	6.25	6.5	V
V_{PP}	Programming Supply Voltage		12.5	12.75	13	V
t_{FR}	Input Rise, Fall Time		5			ns
V_{IL}	Input Low Voltage			0	0.45	V
V_{IH}	Input High Voltage		2.4	4		V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2	V
t_{OUT}	Output Timing Reference Voltage		0.8	1.5	2	V

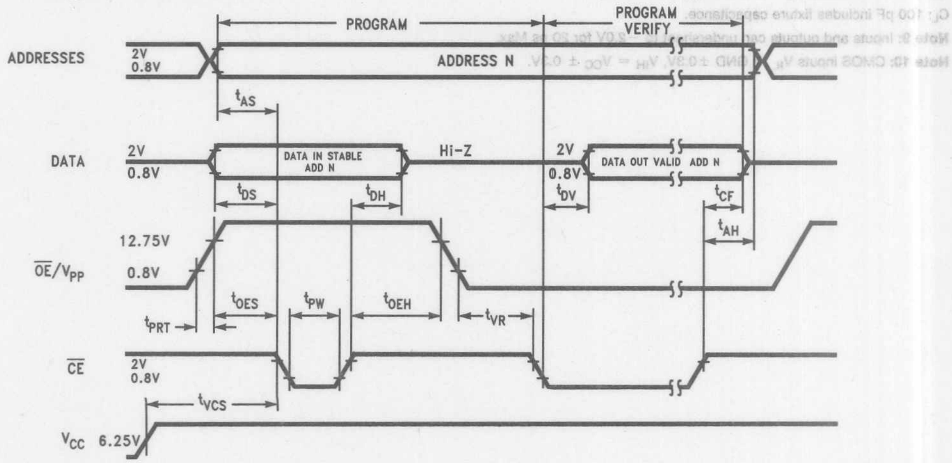
Note 1: National's standard product warranty applies to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 3: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least 0.1 µF capacitor is required across V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 4: Programming and program verify are tested with the fast Program Algorithm at typical power supply voltages and timings.

Programming Waveforms



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Fast Programming Algorithm Flow Chart

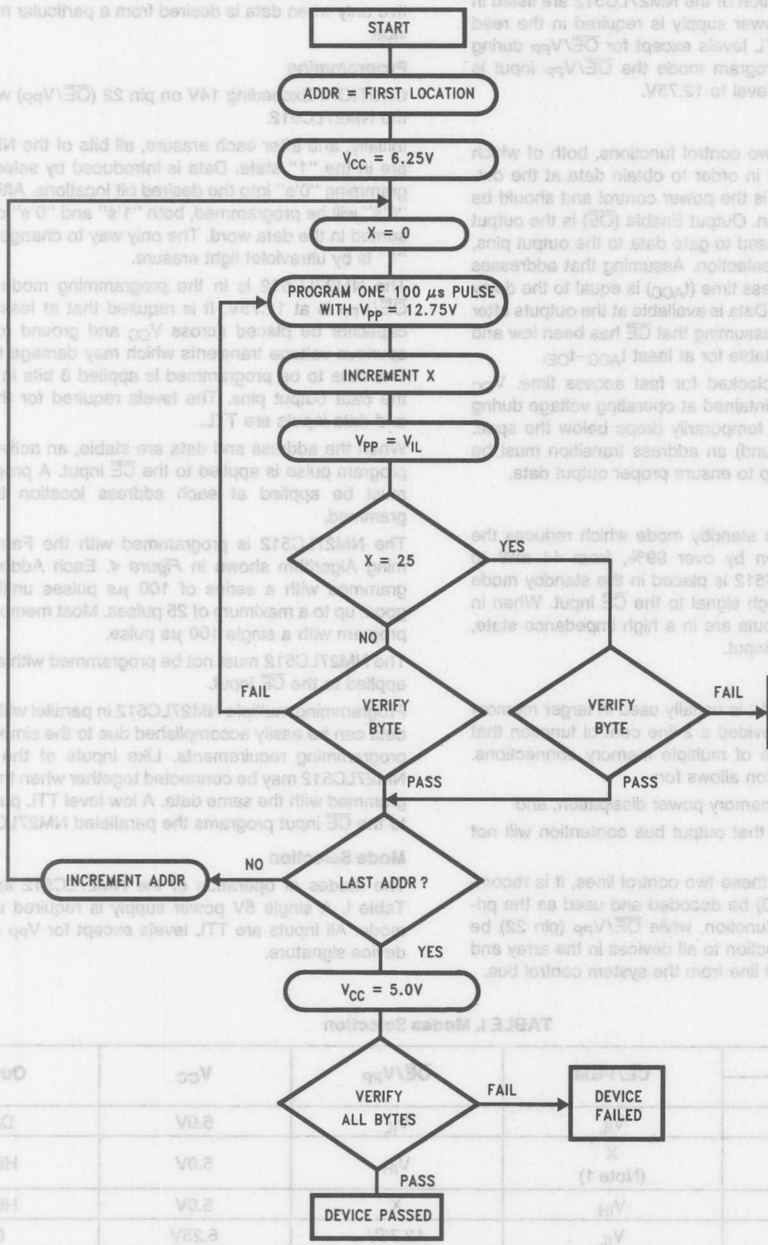


FIGURE 4

Functional Description

DEVICE OPERATION

The six modes of operation of the NM27LC512 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL low level to 12.75V.

Read Mode

The NM27LC512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to ensure proper output data.

Standby Mode

The NM27LC512 has a standby mode which reduces the active power dissipation by over 99%, from 44 mW to 0.55 mW. The NM27LC512 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because the NM27LC512 is usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}/V_{PP}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 22 ($\overline{OE}/V_{PP}$) will damage the NM27LC512.

Initially, and after each erasure, all bits of the NM27LC512 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NM27LC512 is in the programming mode when the $\overline{OE}/V_{PP}$ is at 12.75V. It is required that at least a 0.1 μF capacitor be placed across V_{CC} and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed.

The NM27LC512 is programmed with the Fast Programming Algorithm shown in *Figure 4*. Each Address is programmed with a series of 100 μs pulses until it verifies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 μs pulse.

The NM27LC512 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming multiple NM27LC512 in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NM27LC512 may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NM27LC512.

Mode Selection

The modes of operation of the NM27LC512 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and A9 for device signature.

TABLE I. Modes Selection

Pins / Mode	$\overline{CE}$/PGM	$\overline{OE}/V_{PP}$	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	5.0V	D_{OUT}
Output Disable	X (Note 1)	V_{IH}	5.0V	High Z
Standby	V_{IH}	X	5.0V	High Z
Programming	V_{IL}	12.75V	6.25V	D_{IN}
Program Verify	X	V_{IL}	6.25V	D_{OUT}
Program Inhibit	V_{IH}	12.75V	6.25V	High Z

Note 1: X can be V_{IL} or V_{IH}.

Functional Description (Continued)

Program Inhibit

Programming multiple NM27LC512 in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NM27LC512 may be common. A TTL low level program pulse applied to an NM27LC512's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 12.75V will program that NM27LC512. A TTL high level $\overline{CE}$ input inhibits the other NM27LC512 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

Manufacturer's Identification Code

The NM27LC512 has a manufacturer's identification code to aid in programming. The code, shown in Table II, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NM27LC512 is , "8F 85", where "8F" designates that it is made by National Semiconductor, and "85" designates a 512k part.

The code is accessed by applying 12V ±0.5V to address pin A9. Addresses A1–A8, A10–A15, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read on the 8 data pins. Proper code access is only guaranteed at 25°C ±5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in an EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NM27LC512 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range.

After programming opaque labels should be placed over the NM27LC512 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NM27LC512 is exposure to short wave ultraviolet light which has a wavelength of 2537Å. The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NM27LC512 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure. Table III shows the minimum NM27LC512 erasure time for various light intensities.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE II. Manufacturer's Identification Code

Pins	A0 (10)	A9 (24)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	12V	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	12V	1	0	0	0	0	1	0	1	85

TABLE III. Minimum NM27LC512 Erasure Time

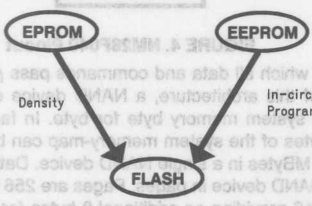
Light Intensity (Micro-Watts/cm^2)	Erasure Time (Minutes)
15,000	20
10,000	25
5,000	50

Section 4
Application Notes

Section 4 Contents

Flash technology is basically an outgrowth of EPROM technology. Toshiba first invented Flash technology in the mid 80's. Intel quickly developed its own version based on a simpler cell structure, ETOX (EPROM Tunnel Oxide). Cells based on the ETOX structure are the basis for the majority of the Flash products sold today.

Flash memory takes the features of EEPROM and combines them with the density of EPROM *(Figure 1)*. Like EEPROM, Flash offers in-circuit programmability. But Flash also uses only one transistor per cell which enables it to achieve densities as high as 16Mb. This is equivalent to current DRAM densities. In fact, Flash should keep pace with and possibly exceed DRAM densities because there is no additional capacitor in the cell.



TL/D/11951-1

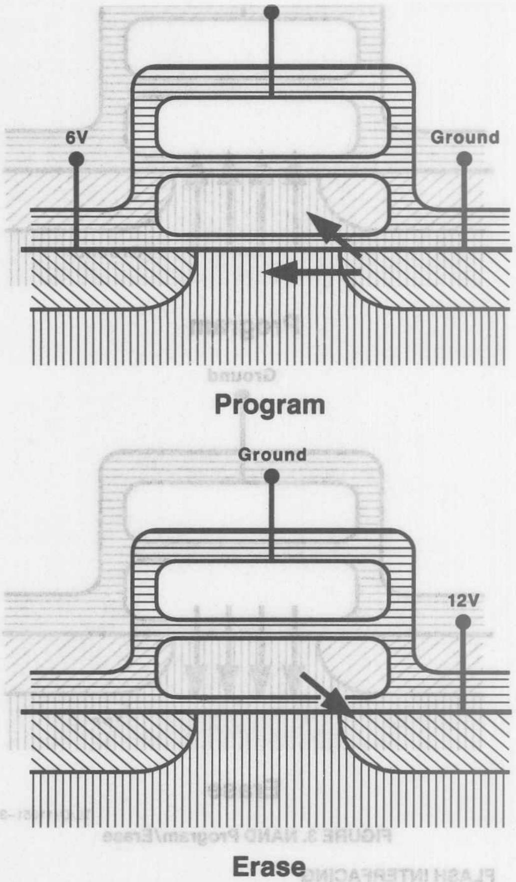
FIGURE 1. FLASH Advantage

There are actually two different kinds of Flash memory. One kind, NOR Flash, is very similar to EPROM's. The other, called NAND Flash, is comparable to E²PROM's. The main difference between NOR and NAND is how the cells are programmed/erased and how data is read off the device. National Semiconductor is the only U.S. manufacturer to offer both types of Flash. In the NOR Flash, National offers the 1Mb NM28F010 and the 4Mb NM28F040. For NAND, National offers the 16Mb NM29N16.

PROGRAM/ERASE METHODS

Both types of Flash have their own advantages and disadvantages due to the program/erase method used and the architecture. NOR Flash uses EPROM programming methods but erases using an E²PROM method. For programming, NOR uses Hot Electron-Injection (HEI). In this operation, the control gate is held at V_{PP} (12V) while the drain is at 6V and the source grounded *(Figure 2)*. Electrons are injected from the drain to the floating gate. This operation requires a lot of current (mA's) and is the reason why EPROMs and NOR Flash require a 12V supply. The advantage of this method is a relatively fast program (10 μs/byte) while also offering individual byte programmability. For erase, NOR uses Fowler-Nordheim (F-N) tunneling like E²PROMs. To prevent over erasure, an additional step has been added to the erase operation. Prior to erasing, all bytes are programmed to the "1" state. They are then erased by putting the control gate at ground and the source at 12V. Electrons tunnel from the floating gate to the source. The added step to prevent overerasure causes NOR Flash to take longer to erase ($\approx$1 sec.).

An obstacle to the system designer is that individual bytes can not be erased, whole blocks must be erased. National's NM28F040 offers one the smallest block sizes at 16 Kb. The 1Mb parts (xx28F010) have standardized on the entire chip erasing at the same time.



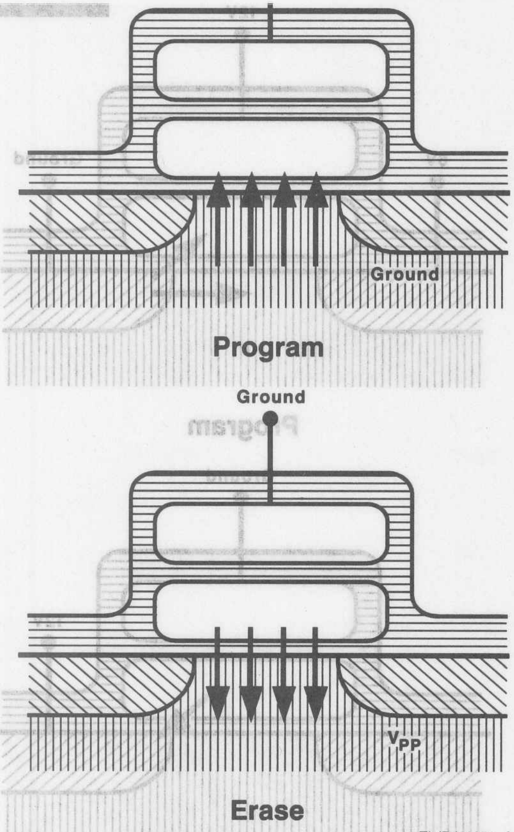
TL/D/11951-2

FIGURE 2. NOR Program/Erase

In contrast to NOR Flash, NAND Flash uses F-N tunneling for both program and erase operations. Programming the cell involves placing the control gate at V_{PP} ($\approx$ 20V) while the channel region is grounded *(Figure 3)*. Electrons tunnel through the gate oxide into the floating gate. An advantage of this method over HEI is that less current is used (μA's). Since the tunneling is from the channel, there is also less stress on the gate oxide. The lower current used allows NAND devices to be built with a single 5V power supply. The lower stress gives NAND devices higher endurance levels (10^6 program/erase cycles versus 10^5 for NOR Flash).

Erasing the NAND cell involves grounding the control gate and pulling the channel region to V_{PP} ($\approx$ 20V). Without the added erase step used by NOR devices, NAND is able to erase in milliseconds rather than seconds.

4



TL/D/11951–3

FIGURE 3. NAND Program/Erase

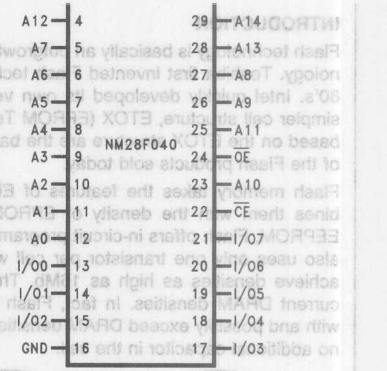
FLASH INTERFACING

Interfacing to a NOR Flash device is just like interfacing to an EPROM. In fact, some NOR Flash devices maintain the same pinout configuration as the similar density EPROM *(Figure 4)*. Reads are performed by placing the address on the address lines, pulling $\overline{CE}$ and $\overline{OE}$ low and then reading the databus.

Programming involves sending in a programming command (40H, this and the following NOR command examples are standardized commands for 1Mb devices) while strobing $\overline{WE}$ low. This is followed by the address and the data while again strobing $\overline{WE}$ low. A successful program can be verified by issuing a program verify command (C0H) and reading the data. The data read out then needs to be compared against the data inputted by the processor.

The erase operation involves writing two consecutive erase commands (20H). Again a verify command (A0H) is sent to check for a successful erase. There is typically a one second delay between the second erase command and the erase verify command.

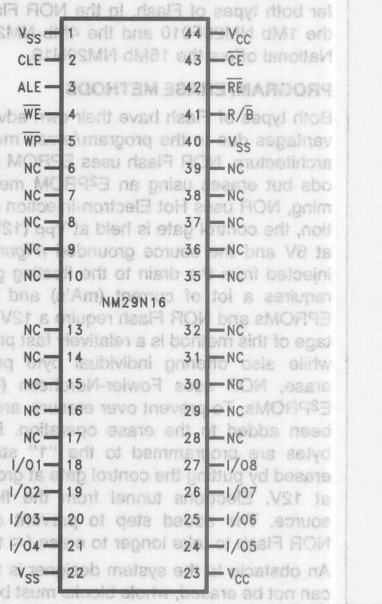
Interfacing to a NAND device is similar to interfacing to a peripheral device on a PC motherboard. The device does not have any address pins but instead has eight I/O lines



TL/D/11951–4

FIGURE 4. NM28F040 Pinout

through which all data and commands pass *(Figure 5)*. Because of this architecture, a NAND device does not map into the system memory byte for byte. In fact, as little as three bytes of the system memory-map can be used to address 2 MBytes in a single NAND device. Data is pulled out of the NAND device in pages. Pages are 256 bytes with the NM29N16 providing an additional 8 bytes for a total of 264 bytes per page. The additional eight bytes may be used for redundancy or error code correction. The read operation involves sending the read command (00H) followed by a three cycle address. The address tells the device which page (16 pages to a block, 512 blocks to a device) to pull from the array and where to set the pointer within the page. The data is pulled from the array and is ready to read after



TL/D/11951–5

FIGURE 5. NM29N16 Pinout

a 25 μs delay. Sending consecutive $\overline{RE}$ pulses reads out data a byte at a time starting at the location pointed to by the pointer.

Programming the device involves sending the data input command (80H), the three cycle address and the data, a byte at a time. This is followed by the program command (10H).

The ready/busy (R/$\overline{B}$) pin will go low for approximately 300 μs while the programming occurs. A verify command (70H) can be sent to ensure of proper operation.

The erase operation consists of sending in the auto block erase command (60H) followed by a two cycle address of the block to erase. The NM29N16 offers designers increased flexibility by using one of the smallest block sizes of any Flash at 4 KBytes. The erase execution command (D0H) is then given to commence the erase procedure.

Again, the ready/busy (R/$\overline{B}$) pin will go low, this time for approximately 6 ms. The verify command can again be used to check for proper operation.

SUMMARY

Overall, Flash memory is a step closer towards the ideal memory device that includes non-volatility with fast read times, high density and low cost. There are a number of compromises that the system designer must make in using Flash, but these are more than overcome by the benefits enjoyed by using Flash (just think of trying to pull an EPROM from a system already in the field as opposed to sending the customer a disk to update his system). In the future, Flash will also allow new systems to come to market that otherwise would not be able to because of weight, cost or power constraints.

Interfacing the NM29N16 in a Microcontroller Environment

National Semiconductor
Application Note 910
Cliff Zitlaw
Rob Frizzell

INTRODUCTION

The NM29N16 is a 2Mbyte NAND Flash EEPROM memory that operates from a single 5V supply. This device does not have the parallel data, address, and control bus interfaces traditionally found on memory devices. The NM29N16 uses a byte wide serial interface with internal address, data, and control registers. The serial interface dramatically reduces the number of pins required to interface to the NM29N16. While the interface is nontraditional, it can easily be interfaced to standard microcontrollers. This application note describes how the NM29N16 can be interfaced to the Motorola 68HC11 microcontroller.

68HC11 INTERFACE

The NM29N16 can be interfaced to a microcontroller using the data bus, control bus, and a few I/O port bits. *Figure 1* shows the NM29N16 interfaced to a minimal 68HC11 system. The 68HC11 is configured in the expanded multiplexed mode which allows access to external memory devices. Most microcontrollers offer a mode that allows access to external memory and the NM29N16 should fit easily into all of these environments.

The I/Os of the NM29N16 were connected directly to the 68HC11 data bus. The NM29N16 occupies addresses C000H to DFFFH in the 68HC11 memory map due to the use of a three to eight (74HCT138) address decoder. While 8Kbytes of memory is taken in this design, the NM29N16 only requires a single address (C000H) out of that block. Due to timing constraints, the $\overline{RE}$ (Read Enable) and $\overline{WE}$ (Write Enable) signals must be ORed with the C000H address decode signal. $\overline{CE}$ (Chip Enable), CLE (Command Latch Enable), and ALE (Address Latch Enable) are controlled directly from three 68HC11 I/O port bits. The R/$\overline{B}$ (Ready/Busy) status output of the NM29N16 is polled by one I/O port bit.

A MAX707 µP supervisory chip is used to drive the $\overline{RESET}$ input of the 68HC11. The MAX707 forces its $\overline{RESET}$ output low until V_{CC} reaches 4.75V. Once V_{CC} exceeds 4.75V the $\overline{RESET}$ output remains low for an additional 200 ms before going high. This $\overline{RESET}$ output is also used to drive the $\overline{WP}$ (Write Protect) input of the NM29N16 to insure against inadvertent writes when V_{CC} is below 4.75V.

68HC11 TO NM29N16 COMMUNICATION

Information is transferred back and forth with a series of read and write operations that access the NM29N16 data, address and control registers. Loading the address register is accomplished by bringing $\overline{CE}$ low, ALE high and then loading data through the data bus with write operations to address C000H. Control register access is performed in a similar manner except that CLE is brought high instead of ALE. Data register access is performed when both ALE and CLE are low.

The EEPROM array in the NM29N16 is not directly accessible from the controller. An intermediate data register is used to transfer a page (264 bytes) of information back and forth between the EEPROM memory and the external controller. There are three basic forms of data transfers; erase operations that operate on a 16 page block, program operations that alter the contents of a single page, and read operations. During these three operations the R/$\overline{B}$ output goes low until the transfer or erase has completed.

A read operation is performed with a four step sequence. The command register is first loaded with the read instruction. The address register is then loaded with the page and byte address to access. At this point an internal recall operation is performed to transfer the contents of an EEPROM page to the 264 byte data register. After the recall has completed the accessed data is finally accessible by reading the contents of the data register. This is accomplished by pulsing $\overline{RE}$ low to read out sequential bytes.

Erase and program operations are performed similarly by accessing the data, control, and address registers. The simple access to these registers allow software routines that are as simple as that required to interface with a traditional parallel memory device.

SOFTWARE DRIVERS FOR A 68HC11 TO NM29N16 INTERFACE

A software listing is provided to demonstrate several features of the NM29N16. Different subroutines were developed that perform the basic read and write functions. These routines can be used with only minor modifications to interface the NM29N16 to any microcontroller.

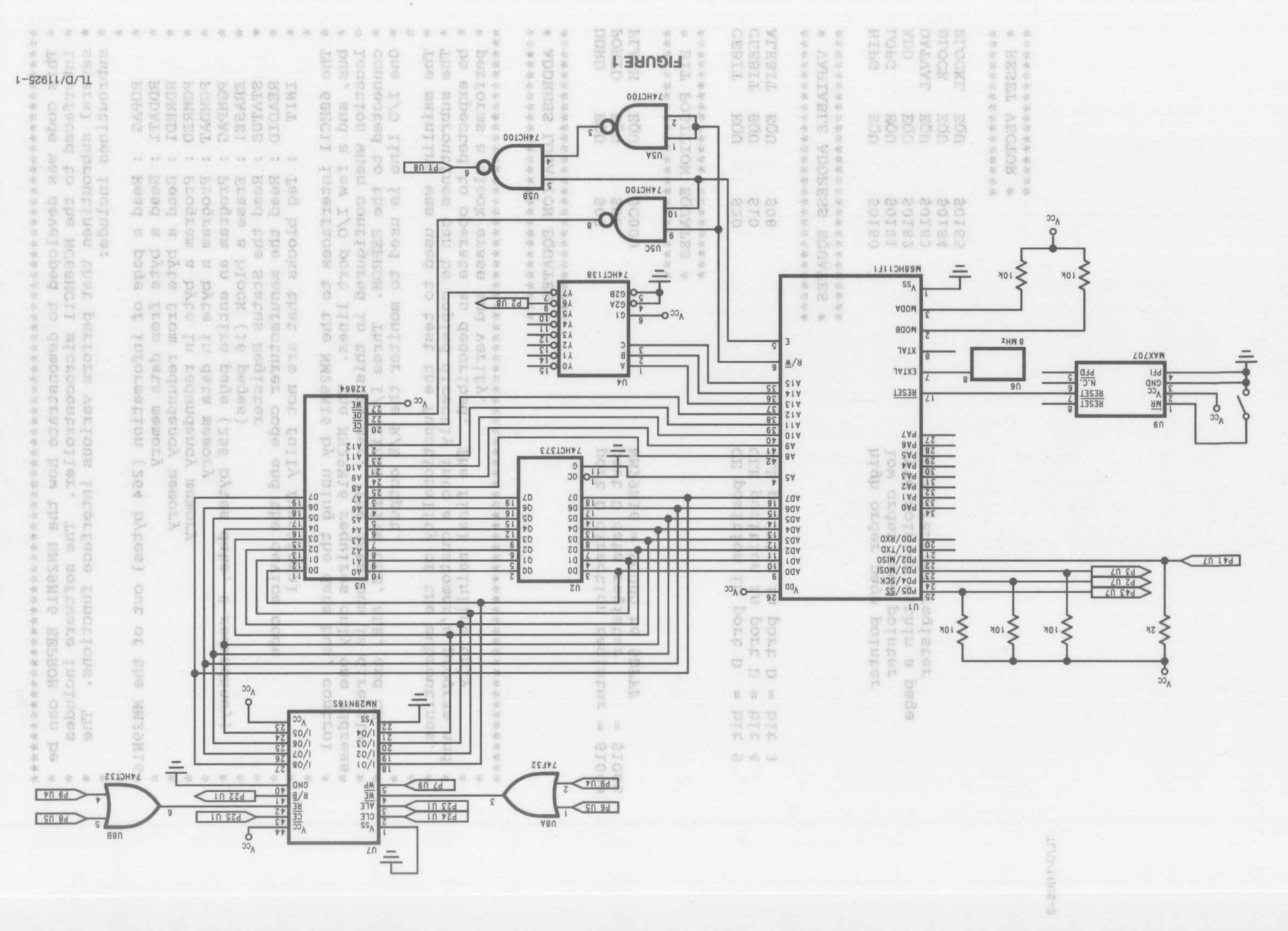

NM29N16S
X2864
74HCT373
74HCT138
74HCT00
74HCT32
74F32
M68HC11F1
MAX707
8 MHz
TL/D/11925-1

FIGURE 1

```
*                                                                      *
*    RDPAG  : Read a page of information (264 bytes) out of the NM29N16*
*    RDDAT1 : Read a byte from data memory                             *
*    RDRED1 : Read a byte from redundancy memory                       *
*    PGMRED : Program a byte in redundancy memory                      *
*    PGMDAT : Program a byte in data memory                            *
*    PGMPAG : Program an entire page (256 bytes data, 8 redundancy)    *
*    ERASE1 : Erase a block (16 pages)                                 *
*    STATUS : Read the Status Register                                 *
*    READID : Read the manufacturer code and the device code           *
*    INIT   : Tag blocks that are not fully functional                 *
*                                                                      *
* The 68HC11 interfaces to the NM29N16 by using the data bus, control  *
* bus, and a few I/O port lines.  The NM29N16 requires only one address*
* location when configured in this manner.  The data bus is directly   *
* connected to the EEPROM.  Three I/O lines drive CLE, ALE, and CE.    *
* One I/O line is used to monitor the R/B output.                      *
*                                                                      *
* The mainline was used to test the functionality of the subroutines.  *
* The subroutines can be copied directly into a customer's program and *
* be expected to operate as described.  The final mainline only        *
* performs a block erase and verify.                                   *
************************************************************************

****************************
* ADDRESS LOCATION EQUATES *
****************************

DDRD     EQU     $09                   port D direction register = $1009
PORTD    EQU     $08                   port D data register      = $1008
FLASH    EQU     $C000                 NM29N16 = $C000 to $DFFF

************************
* BIT POSITION EQUATES *
************************

CEBIT    EQU     $20                   CE position in port D  = bit 5
CLEBIT   EQU     $10                   CLE position in port D = bit 4
ALEBIT   EQU     $08                   ALE position in port D = bit 3

****************************
* VARIABLE ADDRESS EQUATES *
****************************

HIPG     EQU     $0180                 high order page pointer
LOPG     EQU     $0181                 low order page pointer
ADD      EQU     $0182                 byte pointer within a page
DATVAL   EQU     $0183                 data transfer register
BLOCK    EQU     $0184
BLOCKL   EQU     $0185

****************
* RESET VECTOR *
****************
```

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```
        ORG     $FFFE      reset vector to $E000
        FDB     $E000

******************************
* PROGRAM STARTING LOCATION *
******************************

        ORG     $E000      program execution begins at $E000
BEGIN:  LDS     #$01FF     initialize stack pointer
        LDX     #$1000     initialize "address index register"
        LDAA    #$FF       initialize I/O ports
        STAA    PORTD,X
        LDAA    #$3B
        STAA    DDRD,X
        BCLR    PORTD,X #CLEBIT
        BCLR    PORTD,X #ALEBIT   CE=1 CLE=0 ALE=0 initially

************
* MAINLINE *
************

        LDAA    #$00
        STAA    LOPG
        STAA    HIPG
        JSR     ERASE1
        JSR     STATUS

LOOP:   BRA     LOOP       wait until reset loop

************************************************************************
* RDPAGE copies a page from the NM29N16 into SRAM memory on the 68HC11.*
* All 264 bytes (data and redundancy) are copied into the SRAM buffer. *
* The page number to be transfered is passed in the variables LOPG and *
* HIPG.  The EEPROM data is copied into the 68HC11 SRAM between        *
* addresses 0000H and 0107H.                                           *
************************************************************************

RDPAGE: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$00
        STAA    FLASH             load READ(1) instruction into
        BSET    PORTD,X #CEBIT    the command register
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$00              load the byte pointer in the address
        STAA    FLASH             register with 00H (start of page)
        LDAA    LOPG
        STAA    FLASH             load low order page number
        LDAA    HIPG
        STAA    FLASH             load high order page number
        BCLR    PORTD,X #ALEBIT
        JSR     WAIT              wait for recall into data register
        LDY     #$0000
NEXTR:  LDAA    FLASH             read data from EEPROM and fill SRAM
        STAA    $00,Y             buffer with data register contents
        INY
        CPY     #$0108            loop until all 264 bytes have
        BNE     NEXTR             been transfered
        BSET    PORTD,X #CEBIT
```

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4

```
        JSR     WAIT                pause to assure EEPROM is idle
        RTS

***********************************************************************
* RDDAT1 and RDRED1 are used to read the contents of a single address *
* in the EEPROM array.  Data can be read from either the DATA portion *
* of the array (RDDAT1) or the REDUNDANT portion (RDRED1).  The       *
* location to be accessed is defined in the variables ADD, LOPG, and  *
* HIPAG.  LOPG and HIPG define the page to be accessed and ADD        *
* indicates a position within the page.  ADD can range between 0 and  *
* 255 for DATA accesses or between 0 and 7 for REDUNDANT accesses.    *
* The value in the chosen location is returned in the variable DATVAL.*
***********************************************************************

RDDAT1: LDAA    #$00                READ(1) command
        BRA     RDJMP
RDRED1: LDAA    #$50                READ(2) command
RDJMP:  BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        STAA    FLASH               load appropriate READ command into
        BSET    PORTD,X #CEBIT       the command retister
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    ADD                 load the byte address into the
        STAA    FLASH                address register
        LDAA    LOPG
        STAA    FLASH               load the low order page number
        LDAA    HIPG
        STAA    FLASH               load the high order page number
        BCLR    PORTD,X #ALEBIT
        JSR     WAIT                wait for recall to data register
        LDAA    FLASH               load the value from the chosen

        LDAA    FLASH

        STAA    DATVAL               address and save the result in DATVAL
        BSET    PORTD,X #CEBIT
        JSR     WAIT                pause until EEPROM is idle
        RTS

***********************************************************************
* PGMRED, PGMDAT, and PGMPAG are used to program either a single byte *
* or an entire page.  During program operations the entire data register*
* must be loaded and then the contents transfered to an EEPROM page.  *
* EEPROM bits can only be flipped from a one (erased state) to a zero *
* (programmed state) during a program operation.  To program a single *
* byte the entire data register must be filled with FFH except for the *
* byte that is to be programmed.  During the programming cycle bits   *
* that are zero in the data register will force the corresponding bits *
* in the chosen page to the zero state, other bits will remain        *
* unchanged.                                                          *
*                                                                     *
* These routines use a SRAM data array located on the 68HC11 between  *
* address 0000H and 0107H.  This array is transfered byte for byte into *
* the NM29N16 data register during the data load portion of the       *
* programming cycle.  If single byte is to be altered the location    *
* in the SRAM array corresponding to the address to be programmed is  *
* loaded with the new data and all other addresses in the array are   *
* filled with FFH.                                                    *
```

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```
* is contained in the variable DATVAL, the page number is contained in  *
* PGLO and PGHI, and the byte position within the page is contained in  *
* ADD.                                                                   *
*                                                                        *
* The routine PGMPAG assumes that the SRAM array already has the data   *
* that will be programmed into the EEPROM.  PGLO and PGHI contain the   *
* page number to be programmed.                                          *
**************************************************************************

PGMRED: JSR     FILLFF                  fill SRAM array with FFH
        LDY     #$0100                  load Y with redundant memory offset
        BRA     PGMB
PGMDAT: JSR     FILLFF                  fill SRAM array with FFH
        LDY     #$0000                  load Y with data memory offset
PGMB:   LDAB    ADD                     data or redundant address to alter
        ABY                             calculate absolute address in page
        LDAA    DATVAL
        STAA    $00,Y                   write new data byte into SRAM array
PGMPAG: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$80                    load command register with
        STAA    FLASH                    data input command
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        LDAA    #$00                    load address register with
        STAA    FLASH                    start of page
        LDAA    LOPG
        STAA    FLASH                   load low order page number
        LDAA    HIPG
        STAA    FLASH                   load high order page number
        BCLR    PORTD,X #ALEBIT
        LDY     #$0000
LOADB:  LDAA    $00,Y                   transfer data from SRAM array
        STAA    FLASH                    into the NM29N16 data register
        INY
        CPY     #$0108                  loop until all 264 bytes have
        BNE     LOADB                    been transfered
        BSET    PORTD,X #CLEBIT
        LDAA    #$10                    load command register with
        STAA    FLASH                    start program command
        BSET    PORTD,X #CEBIT
        BCLR    PORTD,X #CLEBIT
        JSR     WAIT                    pause to make sure EEPROM idle
        RTS

FILLFF: LDY     #$0000                  fill SRAM addresses 0000H to
        LDAA    #$FF                     0107H with FFH
LOOPF:  STAA    $00,Y
        INY
        CPY     #$0108
        BNE     LOOPF
        RTS

**************************************************************************
* ERASE1 performs an erase operation on a single block (16 pages). The *
* block to be erased is specified in the variables LOPG and HIPG. The  *
* lower 4 bits of LOPG are not used so that the least significant bit of*
```

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```
ERASE1: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$60               load command register with
        STAA    FLASH               block erase command
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        LDAA    LOPG               load low order block number
        STAA    FLASH               (XXXX0123)
        LDAA    HIPG               load high order block number
        STAA    FLASH               (45678XXX)
        BCLR    PORTD,X #ALEBIT
        BSET    PORTD,X #CLEBIT
        LDAA    #$D0               load command register with erase
        STAA    FLASH               execution command
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #CEBIT
        JSR     WAIT               pause until EEPROM is idle
        RTS

************************************************************************
* STATUS is used to read the NM29N16 status register.  This command can *
* be used after erase and program cycles to determine if the results    *
* were successfull.  The contents of the status register are returned in*
* the variable DATVAL.                                                  *
************************************************************************

STATUS: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$70               load command register with
        STAA    FLASH               status read command
        BSET    PORTD,X #CEBIT
        BCLR    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    FLASH              read status register
        STAA    DATVAL             save results
        BSET    PORTD,X #CEBIT
        RTS

********************************************************************
* READID is used to read the NM29N16 device and manufacturer codes. *
* The manufacturer code is returned in the A register and the device*
* code is returned in the B register.                               *
********************************************************************

READID: BSET    PORTD,X #CLEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$90               load the command register with
        STAA    FLASH               the ID read command
        BSET    PORTD,X #CEBIT
        BCLR    PORTD,X #CLEBIT
        BSET    PORTD,X #ALEBIT
        BCLR    PORTD,X #CEBIT
        LDAA    #$00               load the address register with
        STAA    FLASH               address 0
        BCLR    PORTD,X #ALEBIT
        LDAA    FLASH              read the manufacturer code
```

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```
        LDAB    FLASH                          read the device code
        BSET    PORTD,X #CEBIT
        RTS

**********************************************************************
* WAIT is used to pause until the NM29N16 returns to the ready mode. *
* The routine polls the R/B (ready/busy) pin until it returns high.  *
**********************************************************************

WAIT:   LDAA    PORTD,X                        check bit 2 of port D (R/B line)
        ANDA    #$04
        CMPA    #$00
        BEQ     WAIT                           loop until R/B returns high
        RTS

************************************************************************
* INIT is used to determine which blocks in the NM29N16 are usable.  The *
* sequence is as follows:                                              *
*                                                                      *
*  1      Start with block 0                                           *
*  2      Erase and verify block                                       *
*  3      Write $AA to each page in the block and verify               *
*  4      Erase and verify block                                       *
*  5      Write $55 to each page in the block and verify               *
*  6      Erase and verify block                                       *
*  7      If steps 1-5 were successful tag the good block with data $F0 *
*          in address 0 of the redundancy memory in page 0 of the block *
*           just verified                                              *
*  8      Step through all 512 blocks                                  *
************************************************************************

INIT:   LDY     #$0000                         start with block 0
        STY     BLOCK
LOOP1:  LDY     BLOCK
        STY     HIPG
        JSR     ERASE1                         erase block
        JSR     STATUS                         see if erase was successful
        LDAA    DATVAL
        ANDA    #$01
        BEQ     NXTSTP                         jump to BADBLK if erase unsuccessful
        JMP     BADBLK
NXTSTP: LDAA    #$AA                           verify that $AA can be written
        JSR     FILLXX                          to all pages in the block
        LDY     BLOCK
        LDAB    #$0F                           start with page 15 and work down
        CLC                                     to page 0
        ABY
        STY     HIPG
        LDAA    #$00
        STAA    ADD
LOOPAA: JSR     PGMPAG                         program page with $AA
        JSR     STATUS                         see if programming is successful
        LDAA    DATVAL
        ANDA    #$01
        BNE     BADBLK                         jump to BADBLK if bad page found
        LDAA    LOPG
        ANDA    #$0F                           loop until all pages have been
        BEQ     DONEAA                          tested
        DEC     LOPG                           step to next page in the block
        BRA     LOOPAA                          being verified
```

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```
DONEAA: JSR     ERASE1        erase block
        JSR     STATUS        see if erase was successful
        LDAA    DATVAL
        ANDA    #01
        BNE     BADBLK        jump to BADBLK if erase unsuccessful
        LDAA    #$55          verify that $55 can be written to
        JSR     FILLXX        all pages in the block
        LDY     BLOCK
        LDAB    #$0F          start with page 15
        CLC
        ABY
        STY     HIPG
        LDAA    #$00
        STAA    ADD
LOOP55: JSR     PGMPAG        program page with $55
        JSR     STATUS        see if programming is successful
        LDAA    DATVAL
        ANDA    #$01
        BNE     BADBLK        jump to BADBLK if bad page found
        LDAA    LOPG
        ANDA    #$0F          loop until all pages in block
        BEQ     DONE55        have been verified
        DEC     LOPG          step to next page
        BRA     LOOP55
DONE55: JSR     ERASE1        erase block
        JSR     STATUS        see if erase is successful
        LDAA    DATVAL        jump to DATVAL if bad block found
        ANDA    #01
        BNE     BADBLK        jump to BADBLK if erase unsuccessful
        LDAA    #$F0          tag good block by writing $F0 into
        STAA    DATVAL         byte 0, page 0 (redundancy memory)
        LDY     BLOCK          of the block just verified
        STY     HIPG
        LDAA    #$00
        STAA    ADD
        JSR     PGMRED
BADBLK: LDY     BLOCK         exit routine if all 512 blocks
        CPY     #$1FF0         have been tested
        BEQ     DONE
        CLC                   step to next block (16 pages)
        LDAB    #$10
        ABY
        STY     BLOCK
        JMP     LOOP1         go verify next block
DONE:   RTS

FILLXX: LDY     #$0000        fill SRAM addresses 0000H to
LOOPF2: STAA    $00,Y          0107H with value in A reg
        INY
        CPY     #$0108
        BNE     LOOPF2
        RTS
```

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SUMMARY

The NM29N16 provides an extremely flexible interface for many systems. By not utilizing address lines, the device gives designers the ability to incorporate multiple megabytes of memory without the use of an expensive processor or system bus. The application described here is only one example of this. With this architecture, the NM29N16 should enable new types of portable systems to be developed.

National offers two types of Flash Devices, namely NOR type and NAND type. The device densities ranging from 1 Mbit to 16 Mbit, suited for various kinds of applications like BIOS code storage, Solid state file storage, Image file storage, etc. Some of the devices also feature Auto program/erase operations which aid in elegant, compact programming code.

This note describes the various hardware considerations that a system designer has to consider when using National's Flash devices.

ORGANIZATION

1. DEVICE CONSIDERATIONS

   This section addresses the various issues like programming voltage (V_{PP}) generation and control, V_{CC} considerations, etc.

2. NOR DEVICES

   The NOR Flash device section covers the individual design considerations for the following Flash devices

   NM28F010: 1 Mbit, byte wide device.

   NM28F040: 4 Mbit, byte wide device.

   NM28F044: 4 Mbit, byte wide device.

3. NAND DEVICE

   This section covers NAND type NM29N16 device, which is a 16 Mbit, 5V only device ideally suited for large file storage type of applications, like Solid state Disk, PCMCIA based Memory cards, etc.

4. ICP (In-Circuit Programming)

   Finally, this note also discusses the In-Circuit Programming (ICP) in general, and the various types of ICP configurations available today.

1.0 DEVICE CONSIDERATIONS

V_{PP} Specifications: National's Flash devices have ±5% tolerance specification on the 12V level that is required for V_{PP}. This specification is guaranteed by most of the off-the-shelf industry standard power supplies. In fact the PC-AT® system power supply has a +5% and −4% tolerance specification on the +12V level.

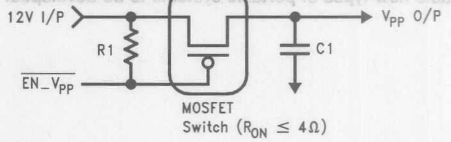

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FIGURE 1

The *Figure 1* represents a typical MOSFET Switch for the 12V line in the interface design towards Flash devices. MOSFET of the above configuration is available from a number of vendors, and MTD4P05 Motorola device is one good example. The only consideration is that the ON-RESISTANCE of the selected Switch should be low enough to keep the V_{PP} o/p within ±5% tolerance range.

The 12V V_{PP} programming voltage required for Programming/Erasing operations on the device is gated from the source (power supply's +12V TAP) through an enabling circuitry (e.g., a MOSFET Switch) to the Flash memory's V_{PP} pin. An enable signal from the system's control circuitry, say, "$\overline{V_{PP}\_EN}$" could then be used to switch ON/OFF the 12V path to the Flash memory's V_{PP} Pin.

Usage of this 12V Switch achieves two purposes:

1. Having the Switch turned off during power up ensures that V_{PP} voltage at the V_{PP} Pin of the device doesn't ramp up before the V_{CC} ramps to the required 5V level, which is a basic requirement for the Flash device.
2. In systems, especially laptop portables, having 12V supply enabled ON continuously is not a favourable choice in terms of the power drain of the Battery, since the need for 12V on the V_{PP} Pin is only during Programming/Erasing, etc. operations and not for the typical Read operation. Hence a Switch to turn on the 12V for V_{PP} only during the required limited times saves considerable power.

Additional Considerations: The *Figure 2* shows a typical circuit of a power control circuitry. This kind of a circuitry helps in improving the data integrity. The power sensing device in essence monitors the power supply's 5V output and

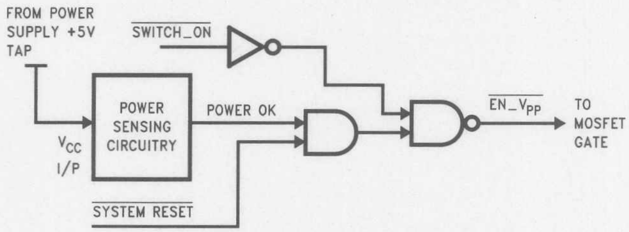

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FIGURE 2

asserts a "power OK" signal only when the input V_{CC} is within the tolerance limits. When the input V_{CC} levels cross the tolerance level, the "power OK" signal is deasserted (driven low) which in turn switches off the MOSFET switch and thus disabling the 12V from reaching the V_{PP} Pin anymore. System's reset signal is also coupled along with this "power OK" signal to take care of power_up and warm reset conditions. "Switch ON" signal is an output from system control circuitry which determines when to apply 12V at the V_{PP} pins of the Flash device under normal operations.

V_{PP} Generation: In the above discussion it is assumed that the 12V ±5% supply is readily available in the system, but for systems where this tolerance requirement is not met or when the 12V ±5% supply is not available at all from the system power supply there are ample V_{PP} Generation circuits available which generally employ one of the following techniques.

1. DC to DC conversion.
2. Regulation from a higher voltage (Down conversion).
3. Voltage boosters (5V to 12V).

A number of solutions employing the above mentioned techniques are available from National Semiconductor. Please refer to the listing given at the end of this note for the source.

V_{CC} Specifications: NSC Flash devices have a tolerance specification of ±5% on the 5V V_{CC} line. Though most of the available Power supplies have a ±5% tolerance specification on their +5V line, variation of this voltage within this tolerance range is dictated by the system loading and switching frequency of the devices at any given instant of time. Proper consideration should be given in choosing a matched Power supply in terms of the Power wattage against the total expected maximum load on the 5V line. Also adequate powerline decoupling especially around the memory devices and high speed switching devices should be ensured, which would take care of the V_{CC} droop caused by device switching to be within the tolerant limits.

Power Sequencing: To protect the device against any data corruption during Power cycling the following power sequencing is required.

Power On Condition: V_{PP} must be applied only after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high.

Power Off Condition: V_{PP} must be turned off after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high. V_{CC} can only be turned off after V_{PP} has reached 0V.

The sample circuit shown in *Figure 2* employing a power sensing unit inherently takes care of the Power-Sequencing required, without any additional logic.

2.0 NOR DEVICES

1. NM28F010 (128k x 8)

The following note describes the In-circuit programming aspects for a system using National's NM28F010 Flash memory device.

NM28F010 is a 1,048,576 bit Flash Electrically Erasable and Programmable Non-volatile memory device. It features single command for typical operations like READ, CHIP ERASE and PROGRAM allowing ease of use for in-circuit programming from within a system.

Software Considerations: The following two tables depict the various modes of NM28F010 Flash device operation and the command definitions to set to a particular mode.

Mode Selection Table

Mode		Signals							
		$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Address	Data	V_{CC}	V_{PP}	Power
READ	Read	L	H	L	Read Address	Data Output	5V	0 ~ V_{CC} or 12V	Active
	Output Deselect	L	*	H	*	High Impedance			
	Standby	H	*	*	*				Standby
COMMAND INPUT	$\overline{WE}$ Control	L	⊔	H	(Note 1)	Command Data			
	$\overline{CE}$ Control	⊔	L	H	(Note 1)	Command Data			
PROGRAM/ERASE		*	H	H	H		5V	12V	Active
PROGRAM/ERASE VERIFY		L	H	L	(Note 1)	Data Output			
ID READ		L	H	L	0x0/0x1	Data Output			

*H or L

Note 1: Refer Command Definition Table

Command Definition Table

Function	No. of Bus Cycles	First Bus Cycle			Second Bus Cycle		
		Type	Address	Data	Type	Address	Data
Read	1	WRITE	*	00H	NA	NA	NA
ID Read	2	WRITE	*	90H	READ	0x0H/0x1H	Mfg/Dev ID
Chip Erase	2	WRITE	*	20H	WRITE	*	20H
Erase Verify	2	WRITE	Byte Address	A0H	READ		EV Data
Program Setup/ Begin	2	WRITE	*	40H	WRITE	Byte Address	WR Data
Program Verify	2	WRITE	Byte Address	C0H	READ	*	WV Data
Reset	2	WRITE	*	FFH	WRITE	*	FFH

*H or L

Interface Block Diagram

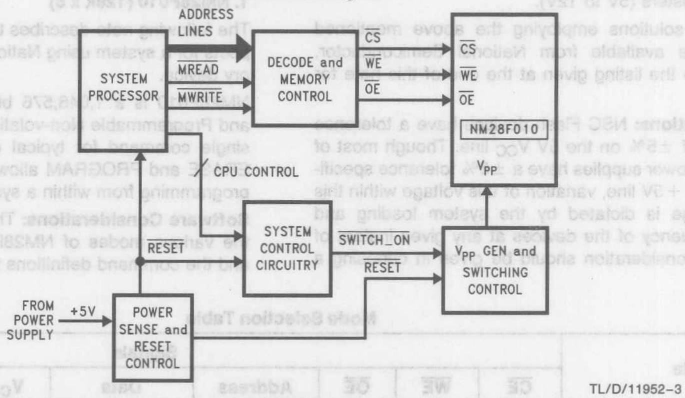


FIGURE 3

Operating Modes: NM28F010 features seven modes of operation as shown in COMMAND DEFINITION TABLE. Setting the device to any particular mode is by writing an appropriate opcode to the Command register of the device. Note that the Command register by itself doesn't occupy any address range of the device and write to the Command register is enabled only when V_{PP} is at 12V level.

A detailed description of the various operating modes can be found in NM28F010 data sheets.

Figure 3 depicts a typical wiring diagram of control signals for a system using National's NM28F010 FLASH Memory with a block level specifications of the integral functional units discussed earlier.

Description: Interface to NM28F010 Flash memory is very much similar to that of conventional 27C010 EPROM except that the system's memory write enable $\overline{\text{MWRITE}}$ is also considered.

The DECODE and MEMORY CONTROL logic could be a simple combinatorial PAL®, like 16L8, which takes in the higher order address lines, memory read and memory write control signals as input and generates Flash memory chip select ($\overline{\text{CS}}$), output enable ($\overline{\text{OE}}$) and write enable ($\overline{\text{WE}}$).

2. NM28F040/NM28F044

NM28F040 and NM28F044 are 4,194,304 bit (512 x 8) CMOS Flash devices featuring single command for Read, Auto Chip erase, Auto Block erase and Auto Program/Verify allowing ease of use for in-circuit programming. NM28F040 is a 32 pin device whereas NM28F044 is a 44 pin device.

UNIQUE FEATURES

Block Mode Erase: These Flash devices can either be full chip erased or in terms of a specific block of 16 kbyte. This block mode erase feature allows ease of management of code blocks.

Auto Function: Both these devices feature a unique "AUTO-FINISH" facility for commands like Chip erase, Block erase and Program/Verify. Once after issuing any of the above commands to the device, all that is required is to sample the device data lines, D7 for operation completion (RDY/BUSY) and D4 for status of completion (FAIL/PASS). These devices have the necessary logic built-in inside the chip to do all of the iterative routines of the programming software. Looping through the same part of the code till operation proves to be a success or failure becomes unnecessary and all those iterative functions can now be removed from the code, resulting in a compact elegant programming algorithm.

Software Considerations: The following two tables outline the various operational modes and the command definition to set the various modes.

READ	Read	L	L	Address	Output	5V	0 ~ V_{CC} or 12V	Active
	Output Deselect	L	H	*	High Impedance			
	Standby	H	*	*				Standby
COMMAND INPUT		⊔	H	(Note 1)	Command Data			
PROGRAM/ERASE		*	*	*		5V	12V	Active
PROGRAM/ERASE STATUS POLLING		L	L	*	DO ~ 3,5,6:Z D4-fail/pass D7-rdy/busy			
ID READ		L	L	0x0/0x1	Data Output			

*H or L

Note 1: Refer COMMAND DEFINITION TABLE

Command Definition Table

Function	No. of Bus Cycles	First Bus Cycle			Second Bus Cycle		
		Type	Address	Data	Type	Address	Data
Read	1	WRITE	*	00H	NA	NA	NA
ID Read	2	WRITE	*	90H	READ	0x0H/0x1H	Mfg/Dev ID
Auto Byte Program	2	WRITE	*	10H	WRITE	Byte Address	WR Data
Auto Chip Erase	2	WRITE	*	30H	WRITE	*	30H
Auto Block Erase	2	WRITE	*	20H	WRITE	Block Address	D0H
Reset	2	WRITE	*	FFH	WRITE		FFH

Operating Modes: Both NM28F044 and NM28F040 feature same modes of operation, viz., Read, ID Read, Reset, Auto Byte Program, Auto Chip Erase and Auto Block Erase.

The Read, ID Read and Reset modes of operation of these two devices are the same as that of NM28F010, however the Program and Erase modes are significantly different from NM28F010.

A more detailed description of the various operating modes can be found in the relevant device data sheets.

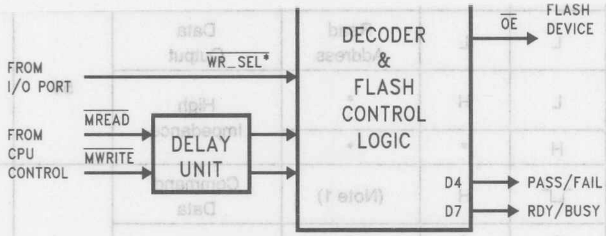
HARDWARE CONSIDERATIONS

1. NM28F044

Designing around NM28F044 is very much similar to NM28F010 which we discussed earlier, but with the following difference:

Two of the data lines, D7 and D4, signify the operation completion and status of completion respectively. Once after issuing any of the Auto Byte Program, Auto Chip Erase and Auto Block Erase commands to the device, all that is required is to do a read on the device after a specified time (depending on the command issued). A High (High logic level) on the data line D7 signifies that the operation for the issued command was completed. The data line stays at Low (Low logic level) if the operation is not completed yet. Similarly, when D7 has become high, a Low (Low logic level) on the D4 line signifies success of the operation and a High (High logic level) signifies failure.

4



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(*"$\overline{\text{WR\_SEL}}$" signal could be same as "$\overline{\text{EN\_V}_{PP}}$" signal)

FIGURE 4

NM28F040 Flash device is different from NM28F044 Flash device in sense that it doesn't have a "$\overline{\text{WE}}$" signal. The "$\overline{\text{CS}}$" signal in this device acts as a multiplexed pin for both chip select (in the case of a read from the device) and write enable (in the case of a write to the device). Write mode is differentiated from the READ mode by the following conditions:

$\overline{\text{CS}}$	$\overline{\text{OE}}$	Operation on the Device
L	L	READ
*	H	WRITE

* → $\overline{\text{CS}}$ pulsing when $\overline{\text{OE}}$ is held high

But "$\overline{\text{CS}}$" signal continues to behave like a chip select signal (read mode) as long as V_{PP} voltage remains below V_{CC}, no matter whatever operation (READ or WRITE) is done on the device. *Figure 4* shows one possible way of interfacing NM28F040 Flash device in a system.

"$\overline{\text{CS}}$" Generation: The potential problem of chip select ($\overline{\text{CS}}$) signal glitching and thus leading to the possibilities of corrupting any valid data in the Flash device can be easily surmounted with simple logic. Data corruption chances are possible in NS28F040 Flash device only when 12V power is enabled to the V_{PP} pin of the device and then there is an extraneous cycle happening on the bus (bus cycle to a device other than the Flash device).

Memory decode designs in general incorporate a mechanism of gating the decoded signal (from the address bus) with Memory control signals ($\overline{\text{MREAD}}$ and $\overline{\text{MWRITE}}$) to generate a valid chip select to the memory. **Glitches become apparent when the total time for the address bus to get stabilized to valid logic levels (say, Tsb) and the time to decode the address lines (say, Td) is longer than the Memory control signal ($\overline{\text{MREAD}}$ or $\overline{\text{MWRITE}}$) driven valid delay (say, Tv).**

In systems where both the Address lines and the memory control signals are driven simultaneously this "glitching" scenario is inherent and one common way of eliminating the glitches in the output (chip select) signal is to delay the memory control signal by an amount greater than **Tsb + Td** and using this delayed signal for gating purpose. Simple DELAY LINE devices can be used to delay the control signals, as shown in *Figure 4*.

Processors like I80486, output Address, Memory control (M/IO) and Read Write (PW/R) control signals all at the same instant whenever an external cycle is started on the system bus. In this scenario, generating the chip select signal from address and M/IO and PW/R control signals all gated together would have the output chip select signal glitching for a period equal to the above mentioned **Tsb + Td.** But by using a delayed (by an amount **Tsb + Td**) memory READ/WRITE signal for final gating, chances for glitches in the chip select signal is eliminated.

"$\overline{\text{WE\_SEL}}$" Signal: The "$\overline{\text{WE\_SEL}}$" signal shown in *Figure 4* is a signal from one of the available general purpose I/O ports. This signal in most cases is the same as the "$\overline{\text{EN\_V}_{PP}}$" signal which was discussed earlier.

Prior to doing any write operation on the Flash device, the V_{PP} circuitry must be turned on so that V_{PP} voltage at the V_{PP} pin is 12V. "$\overline{\text{EN\_V}_{PP}}$" is a signal generated for this purpose. The same signal can be used in the $\overline{\text{CS}}$ generation logic to gate the decoded address signal with either of the memory control signals ($\overline{\text{MREAD}}$ and $\overline{\text{MWRITE}}$) which ever becomes valid during a particular Flash device access. The need for having to do this is due to the multiplexed nature of the chip select pin of the Flash device.

The following representative schematic *(Figure 5)* explains the above discussion.

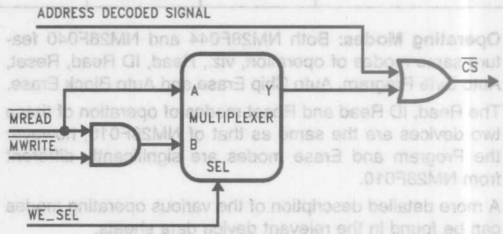

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FIGURE 5

Common Considerations: In all the three Flash devices discussed so far, it is essential that proper command codes are entered in proper sequence. Inputting any command code other than those described could render an improper device functionality. Also accidental removal of V_{PP} supply during any Erase or Program operation in progress should be taken care of, for in some cases the valid data in the device could get corrupted. It's also essential to employ a POWER ON/OFF sequence as described earlier to safeguard the valid data against any corruption possibilities during power cycling.

3.0 NAND DEVICE

NM29N16 (2M x 8-Bit)

GENERAL DESCRIPTION

National's NM29N16 is 16.5 Mbit NAND Electrically Erasable and Programmable device. NM29N16 is a 5V only device, which does not require 12V for any of the Programming or Erase operations.

Organization: NM29N16 is organized as (256 + 8) bytes x 16 Pages x 512 Blocks. Programming is done in terms of a Page (264 Bytes each) while Erasing is done in terms of a Block or multiples of Blocks (16 Pages each). *Figure 6* depicts a conceptual organization of the Device.

NM29N16 is a byte_wide serial type of device in which the Address and Data are time multiplexed on the same I/O pins as there are no separate Address pins. Address in input as three bytes of Data during Address input cycles. The Program and Erase operations are handled automatically by the device, resulting in minimal Processor intervention and elegant programming code.

Additionally, the device aids in mapping out bad memory locations by providing an extra 8 bytes of redundant memory for every page in the device. This feature makes NM29N16 Flash device as an ideal candidate for SOLID STATE FILE STORAGE applications. Alternatively, this redundant 8 byte space per page can be used for normal storage resulting in extra capacity (16.5 Mbits instead of 16 Mbits).

Applications: NM29N16 is ideally suited for applications like,

1. Solid State File Storage
2. Voice Recording
3. Image File Storage, etc.

NM29N16 type of a device is the most sought after in Solid State File Storage where large data is stored and retrieved at a single access (Normally in terms of some specified Blocks Size). With the advent of PCMCIA based systems, Solid State Data Storage has become an intelligent form of Data storage and NM29N16 with its unique features is the ideal candidate for PCMCIA based Solid State Disk.

Device Specific Details: NM29N16 has the following control signals, whose combination, as depicted in the following truth table, signify the various operations that can be performed on the device. The control signals are **CLE** (command latch enable), **ALE** (address latch enable), $\overline{\textbf{CE}}$ (chip enable), $\overline{\textbf{WE}}$ (write enable), $\overline{\textbf{RE}}$ (read enable) and $\overline{\textbf{WP}}$ (write protect).

Truth Table

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$
Command Input	H	L	L	⊔	H	X
Data Input	L	L	L	⊔	H	X
Address Input	L	H	L	⊔	H	X
Address Output	L	H	L	H	⊔	X
Serial Data Output	L	L	L	H	⊔	X
During Programming (BUSY)	X	X	X	X	X	H
During Erasing (BUSY)	X	X	X	X	X	H
Program/Erase Inhibit	X	X	X	X	X	L

H: V_{IH} L: V_{IL} X: V_{IL} or V_{IH}

Operating Modes: The device supports the following modes of operation, viz., Read Mode-1, Read Mode-2, Status Read, ID Read, Auto Page Program, Auto Block Erase, Auto Multi-Block Erase, Suspend/Resume and Reset.

The device is set into any of the above modes by writing an appropriate opcode into the device Command Register. Then if needed the Address and Data registers are updated. Thus programming the device for any mode of operation involves anything from one step to four step process, depending on the mode. Various Command codes (opcodes) needed for those above mentioned modes are listed in the Command Table.

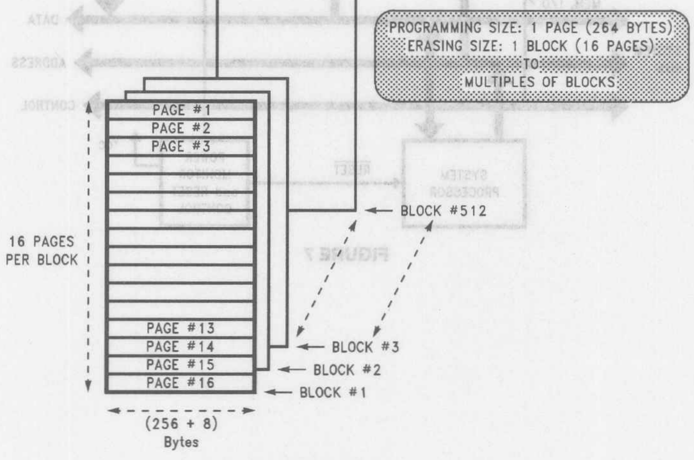

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FIGURE 6

Command Table

Modes of Operation	First Cycle (opcode)	Second Cycle #
Read Mode-1	00	
Read Mode-2	50	
Reset	FF	
Auto Program	80	10
Auto Block Erase	60	D0
Auto Multi Block Erase	60*	D0
Erase Suspend	B0	
Erase Resume	D0	
Status Read	70	
Register Read	E0	
ID Read	90	

Note: Second cycle shown above for the Program/Erase operations is a confirmatory cycle. The actual execution begins only after this command write. This feature is to safeguard against any inadvertent erasures, especially during Power Up.

*For Multi-Block erase operations, Command code (60) is repeated for every block to be erased. Typical sequence for a three block erasure would be, <OPCODE "60"> <Add of Block#1> <OPCODE "60"> <Add of Block #2> <OPCODE "60"> <Add of Block#3> <OPCODE "D0">.

DESCRIPTION OF OPERATIONS: There are basically two types of operations performed on the device, viz., READ and WRITE.

READ Type Operations: Read mode-1, Read mode-2, Status read, Register read and ID read are the operations which conform to Read type. For all these modes the appropriate command code is first written into the device Command register (first cycle). Then depending on the mode issued, address information is written into the Address register, which is essentially three write cycles following the Command input cycle. Then after a specified delay data is read off the Data register through a typical read cycle. Address information is not input for a Status Read operation. All these Registers, viz., Command, Data, Address and Status, do not occupy any of the device's memory location. They are indeed selected by the combination of logic levels of the control signals ALE and CLE. Note also that the Command Register cannot be read back for the contents.

The starting address is composed of 3 bytes, which are entered right after the command input in three successive write cycles. The format of the address is input as shown below:

	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8
First Address Cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second Address Cycle	A8	A9	A10	A11	A12	A13	A14	A15
Third Address Cycle	A16	A17	A18	A19	A20	L	L	L

Note: I/O bits 6, 7 and 8 should be set to low level during the third address cycle.

A12 to A20 form the Block address (selects one out of 512 Blocks).

A11 to A8 form the Page address (selects one out of 16 pages) within a selected Block.

A0 to A7 form the column address (selects the starting address of the data transfer within a page).

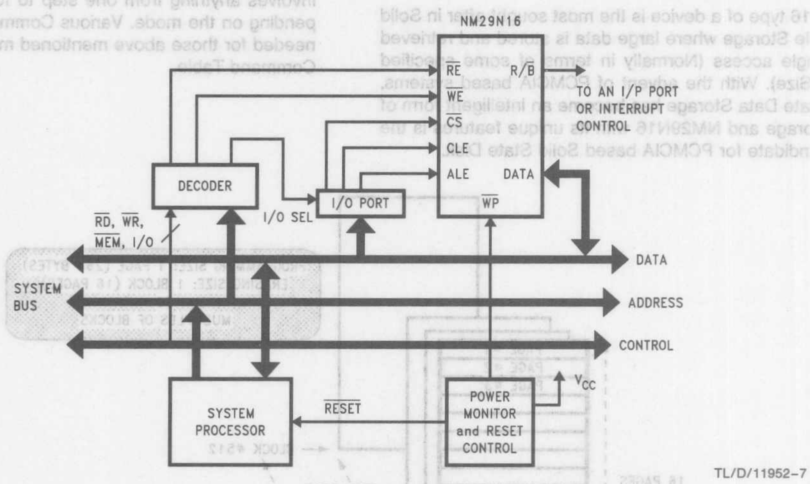


FIGURE 7

WRITE Type Operations: Operations like Program, Erase, Erase suspend, and Reset conform to Write type of command. Setting the device for these operating modes is similar to earlier described READ type operations. In these modes the device is updated with some new information.

A more detailed description of the various operating modes are found in the Device data sheets. Refer to the table given at the end of this note.

Hardware Interface: The *Figure 7* shows one of the methods of interfacing NM28N16 Flash device in a system. A generic Processor (Micro-controller) is assumed in this discussion. The external interface attributes (Bus Control Interface) of this generic processor is commonly found in almost all of the available Processors.

Types of Cycles: The cycle types that are typically performed on NM29N16 Flash device fall into three categories, viz., Command, Address and Data cycles. The following table explains the control signal configuration during these three cycles.

Cycle Types		CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$
Command	Input	H	L	L	⊔	H
Address	Input	L	H	L	⊔	H
	Output	L	H	L	H	⊔
Data	Input	L	L	L	⊔	H
	Output	L	L	L	H	⊔

The Input/Output cycles (in Address and Data cycles) are differentiated by $\overline{WE}$ and $\overline{RE}$ pulsing respectively with other being stable. In general all these three cycles happen either $\overline{RE}$ or $\overline{WE}$ pulsing during a stable window of the other control signals as shown in the above table.

I/O Port: Having an I/O Port type of interface is necessitated by the fact that the NM29N16 Flash Device control signals are not of the same type which are normally found in common Flash Devices. NM29N16 device is meant for large data storage applications (Memory cards, Solid state disk, etc.) where the device form factor is also crucial. In view of this, the device features an optimized Pinout, resulting in a compact device and yet with a much larger capacity. The control signals of this NM29N16 Flash device is not directly compatible to existing Micro-controller interface control. An I/O Port type of interface between this Flash device and any common Micro-controller normally considered for this type of an application, simplifies the interfacing task without any complex logic.

The I/O Port shown in the above diagram is any general purpose I/O port, normally found in a system. One such I/O port is availed to establish the key interface to the NM29N16 Flash device. Three control signals, viz., "$\overline{CS}$", "CLE" and "ALE" are driven by this I/O port as shown. Before doing an actual NM29N16 access, the system CPU initially writes to this I/O Port with the needed signal configuration for the type of the cycle (Command, Address or Data). Then a normal Read or Write cycle to the Flash device memory space would do an actual Read or Write cycle on the device.

Decoder: The decoder unit generates the Read/Write control signals for the Flash device. System address, memory control signals form the input to this unit. This unit could be a combination of discrete devices like 'LS139 or just a combinatorial $\overline{PAL}$ like 16L8 device.

Power Monitor: This unit basically monitors the V_{CC} power point for the required operating level. Whenever the system V_{CC} falls out of the ±5% tolerance range, this unit generates the system Reset as well as the write protect signal ($\overline{WP}$). This unit takes care of the POWERON condition also by keeping the system Reset and $\overline{WP}$ asserted till the system V_{CC} reaches the proper required level and thus protecting the data against corruption. Power monitor unit is available from numerous vendors in the form of a single device. One typical example of such a device would be Dallas Semiconductor component DS1231.

Ready/Busy Signal: This status output signal can be routed to an Input Port, which the CPU can keep polling for the status of operation completion or alternatively to the system's Interrupt control so as to generate an interrupt upon operation completion.

4.0 ICP (IN-CIRCUIT PROGRAMMING)

In-circuit programming (ICP) as opposed to device level programming is an efficient method of programming the most widely used programmable devices like, PROM, EPROM, PAL, PLD, Micro-controllers, FPGA, FLASH memory, etc. ICP is a means of programming these devices after they have been assembled into their target boards. There are broadly two categories of In-circuit programming, one being *Production oriented* and the other being *End user oriented.*

ICP Benefits: Obvious advantages of ICP over the traditional device-level programming are streamlined manufacturing flow, simplified handling, lesser inventory overheads and reduced production costs. ICP has become a preferred method of programming the device with the gaining usage of surface-mount devices (SMDs) and the Just-in-time production methods.

ICP Configurations: Different configurations are available today to achieve the programming of these devices in their target enclosure.

1. *Standalone In-circuit Programmers:* This is the Production oriented type of configuration and in this, the target (device assembled) board(s) get plugged on to slots assigned for programming purpose in the Standalone In-circuit Programmer, much like individual devices (ICs) getting plugged into the IC sockets of a Device Programmer. Then the relevant programming algorithm, resident in the In-circuit Programmer, is executed by the In-circuit Programmer to program the device with the proper data. A typical example of this kind of programmer would be DATA I/O's BoardSite. In this case the target boards usually have additional circuitry to isolate the programmable device(s) from the onboard's logic which is essential during the device programming. The level of complexity of this additional logic varies depending on the type of the device and the number of such devices.

This kind of configuration is well suited for production site programming where assembled boards are directly programmed for the devices present instead of programming the individual devices and house keeping them before assembly into a particular board.

2. *Programming via serial link:* In this configuration the target board has a serial link interface for the purpose of programming (or reprogramming) the device(s) on board. This target board is hooked to a conventional Device programmer via the serial interface, in which case the Device Programmer does the programming job as it would program an individual device.

Compared to the earlier discussed *Production type ICP*, this falls into *End-user type of ICP*, and this method eases the task of any code update at customer site without having to disassemble the target board from the system. But then a device programmer is required to be carried to the customer site to do any re-programming.

3. *In-System Programming:* In this configuration, typically a remote host downloads the software to be updated onto the target system through, say, a serial link. Then the target system executes the resident programming algorithm to program the mounted device. Instead of a serial link, a floppy diskette containing the updated code could be downloaded into the target system for programming purposes.

This approach of In-circuit Programming is preferred where frequent code change is involved, especially in customer field locations, where dismantling the whole system for device replacement purposes is not welcomed and it is not required to carry any device programmer to the customer site.

Flash Memory: An In-circuit Programmable device of particular concern here is a FLASH device which as byfar come in as a drop in replacement for the conventional EPROMs. Apart from delivering the "functional compatibilities", they feature a significant advantage over EPROMs in terms of Re-programming conveniences whenever a code_update is necessitated. Unlike EPROMs which have to be removed from the target board, Ultra-Violet erased, programmed with the new code and then plugged back into the target board, the FLASH devices are erased instantly and re-programmed with the new code all performed when the device is in the target board only, thus bringing all the benefits of ICP.

NAND FLASH Operation

National Semiconductor
Application Note 922
Rob Frizzell

INTRODUCTION

The NM29N16 is a 16Mb FLASH memory that utilizes the NAND architecture. The device incorporates a number of features that make it suitable for numerous portable applications that need large amounts of data storage but can not use a disk drive due to power or weight considerations. While making such systems possible, the NM29N16 also offers greater performance over disk drives in the area of data transfer time, program time, and endurance.

The following sections give a general overview of the NM29N16 and describe how it operates. The operation of the three basic functions: read, write and program, is gone over in detail followed by the physics behind the device operation.

GENERAL DESCRIPTION

The NM29N16 is a unique memory device that does not operate like normal EPROM or SRAM memory devices. All data that is read and written to the device is done in pages, which contain 264 bytes. Data is transferred from/to an on-chip buffer that stores the page. When the data is read out, it is read out sequentially, byte after byte, in order. This data transfer method allows the NM29N16 to not have any address pins which simplifies both board layout and the system interface. The device is easily interfaced to high end microprocessors and low end microcontrollers.

The NM29N16 is organized as 8192 pages of data with each page consisting of 264 bytes. *Figure 1* gives a three-dimensional view of how the device is organized. Each page allows for 256 bytes of data storage plus an additional 8 bytes that may be used for error correction or redundancy.

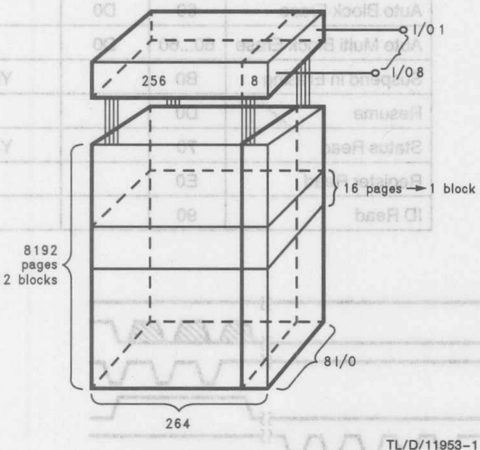


FIGURE 1. NM29N16 Conceptual Layout

There are 16 pages to a block (512 blocks in a device). The block is the smallest unit which can be erased (4 kbytes).

Each block within the array consists of a chain of 16 NAND cells connected in series. *Figure 2* shows a typical cell.

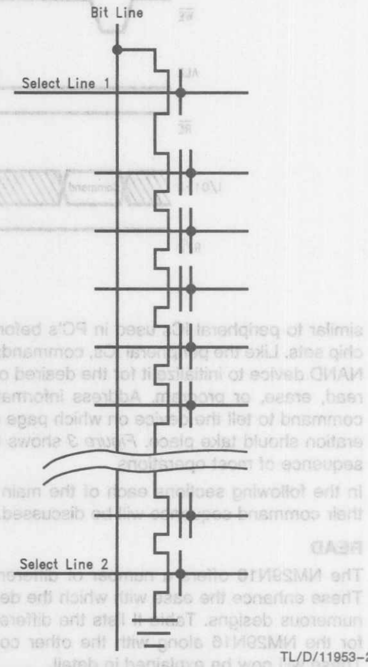


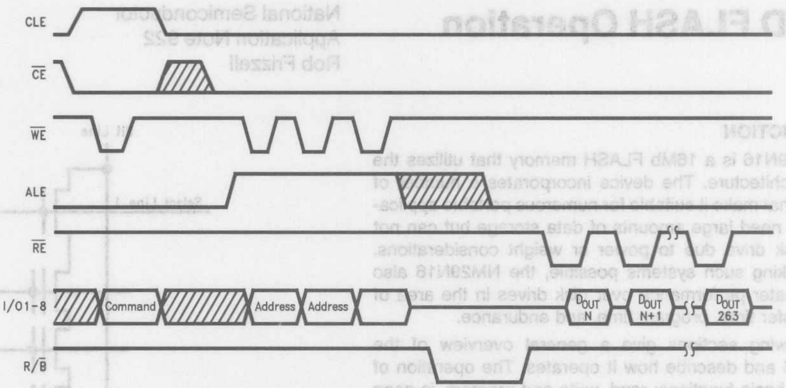
FIGURE 2. NAND Cell Architecture

A block makes up the collection of 16 pages times the 264 bytes per page.

The NM29N16 is not read and written to like normal memory devices. There are no address or data pins for the NAND device as can be seen in Table I. There are only I/O pins,

TABLE I. Pinout of NM29N16

I/O1–8	I/O Port
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{RE}$	Read Enable
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$	Ready/Busy
V_{CC}/V_{SS}	Power Supply/Ground



TL/D/11953-3

FIGURE 3. General Timing Sequence

similar to peripheral ICs used in PC's before the advent of chip sets. Like the peripheral ICs, commands are sent to the NAND device to initialize it for the desired operation, be it a read, erase, or program. Address information follows the command to tell the device on which page or block the operation should take place. *Figure 3* shows the basic timing sequence of most operations.

In the following sections each of the main operations and their command sequence will be discussed.

READ

The NM29N16 offers a number of different Read modes. These enhance the ease with which the device may fit into numerous designs. Table II lists the different Read modes for the NM29N16 along with the other command modes. These will now be explained in detail.

The default mode of the NM29N16 is Read Mode 1. This mode uses the command 00H. A Read is initiated by writing the 00H command to the device followed by an address. The address tells the device what page to pull from the array and at what point within the page to set the pointer. On the rising edge of $\overline{WE}$, the page will be pulled out of the array and into an on-chip buffer. During this time the R/$\overline{B}$ pin goes low. This allows the system to do other operations while polling the R/$\overline{B}$ pin to return high. The time to pull the page from the array into the buffer is typically 25 μs. Once the page is stored in the buffer it can be read out sequentially. Sending consecutive $\overline{RE}$ pulses will read out sequential bytes of data starting at the byte set by the address inputted. For example, sending in address 05H-5FH-1FH would result in reading block 501 (1F5H), page 16(FH) starting at byte 6(05H) of 264 bytes. *Figure 4* graphically shows this example.

TABLE II. NM29N16 Command Modes

Mode	First Cycle	Second Cycle	Acceptable Command during Busy
Serial Data Input	80		
Read Mode (1)	00		
Read Mode (2)	50		
Reset	FF		Yes
Auto Program	10		
Auto Block Erase	60	D0	
Auto Multi Block Erase	60...60	D0	
Suspend in Erasing	B0		Yes
Resume	D0		
Status Read	70		Yes
Register Read	E0		
ID Read	90		

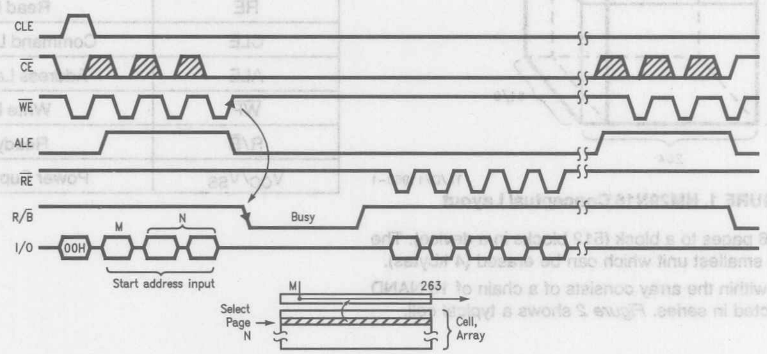


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FIGURE 4. Read Mode 1 Operation

mately 25 μs until the next page is in the on-chip buffer. In this manner the entire device can be read out, page after page. *Figure 5* depicts this wraparound feature.

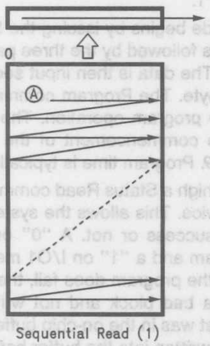

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FIGURE 5. Read Mode 1 Wraparound

Upon reaching the final byte in the final page, additional $\overline{RE}$ pulses will only read out the last byte over and over. In other words, the device will not wrap around to the first page of the array.

The NM29N16 provides eight additional bytes at the end of each page to be used for various functions. A special command, 50H, is used to read out only these last eight bytes from the page. This is achieved by writing the 50H command to the device followed by the three part address. The first byte determines the pointer location but in this case only the first three bits (I/O1–3) are recognized. The remaining bits (I/O4–8) are ignored. Again, the device will go through a 25 μs delay before the data can be read out with strobes of $\overline{RE}$.

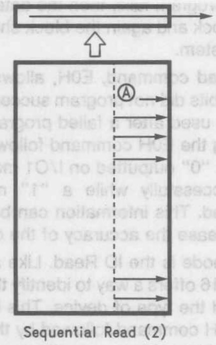

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FIGURE 6. Read Mode 2 Wraparound

A method of checking the status of the NM29N16 is provided via the 70H command. This command provides automatic program and erase verification. No software is needed to check each of the bytes individually to see if they have been programmed or erased properly. The 70H command offers the end user the ability to check if the program or erase operation was carried out successfully. This is accomplished after the R/$\overline{B}$ pin has returned high during a program/erase operation. By issuing the 70H command following R/$\overline{B}$ going high, the status of the device will be outputted on I/O1–8. *Figure 7* shows this operation for a page program operation.

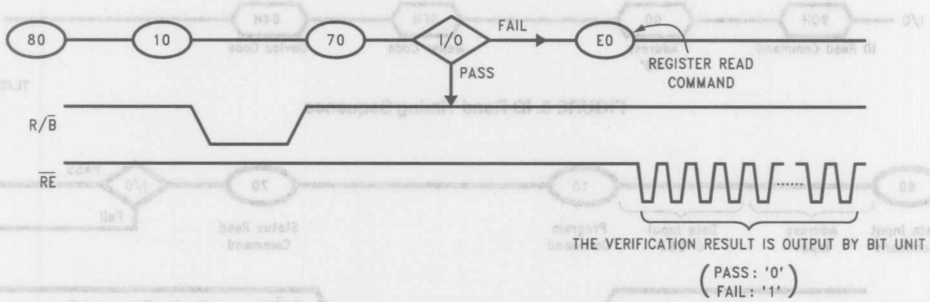

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FIGURE 7. Auto Page Program Verify

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If I/O 1 is a "0", the operation was successful. If a "1" is outputted on I/O1, then the program or erase failed. If an erase failed, then the block that was erased should be mapped by the system as bad and should not be used again. If a page program fails, then the data should be written to another block and again the block should be mapped as bad by the system.

The Register Read command, E0H, allows the system to determine which bits did not program successfully. The E0H command is only used after a failed program attempt. This is done by writing the E0H command followed by consecutive $\overline{RE}$ pulses. A "0" outputted on I/O1 means the bit was programmed successfully while a "1" means the programmed bit failed. This information can be used for error correction to increase the accuracy of the data stored.

The final Read mode is the ID Read. Like all FLASH products, the NM29N16 offers a way to identify the manufacturer of the device and the type of device. This is accomplished by issuing the 90H command followed by the 00H address. This is a single address input, not a three part input like the other commands. Issuing two $\overline{RE}$ pulses will output the manufacture code (8FH for National Semiconductor) followed by the device code (64H for the 16 Mb NAND). *Figure 8* shows the timing sequence. Applications such as PCMCIA cards will use this data to identify the card and determine which driver to use for the interface.

PROGRAM

The NM29N16 implements an automatic programming algorithm which greatly simplifies the system software. The software for programming the device consists of writing three commands and the data. Programming must be done from the lowest page in the block to the highest. For example, page 16(1FH) in block 1 must be programmed before page 15(1EH) in block 1.

The program mode begins by issuing the 80H command to the device. This is followed by the three part address of the page and block. The data is then input sequentially starting with the lowest byte. The Program command, 10H, is then input to start the program operation. The R/$\overline{B}$ line will go low to signal the commencement of the programming as shown in *Figure 9.* Program time is typically around 300 μs.

Upon R/$\overline{B}$ going high a Status Read command, 70H, can be written to the device. This allows the system to verify if the program was a success or not. A "0" on I/O1 reports a successful program and a "1" on I/O1 means a failed program attempt. If the program does fail, the block should be mapped out as a bad block and not written to anymore. Also, the data that was in the on-chip buffer will be lost and will have to be rewritten into the buffer before programming it into a different block. *Figure 10* shows this sequence of commands.

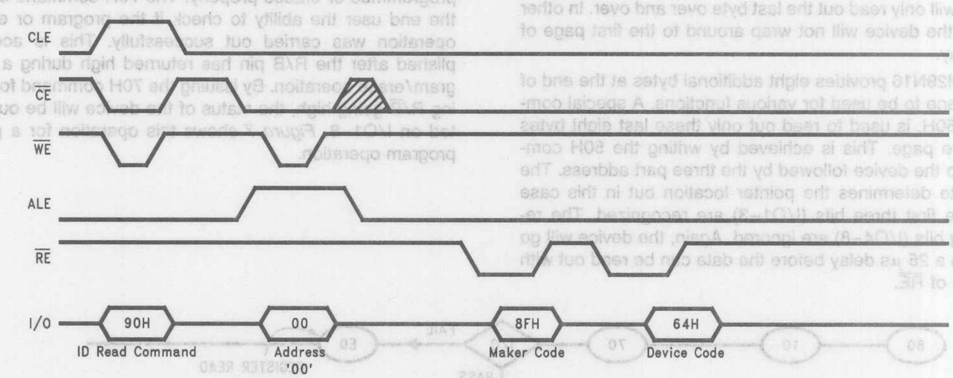

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FIGURE 8. ID Read Timing Sequence

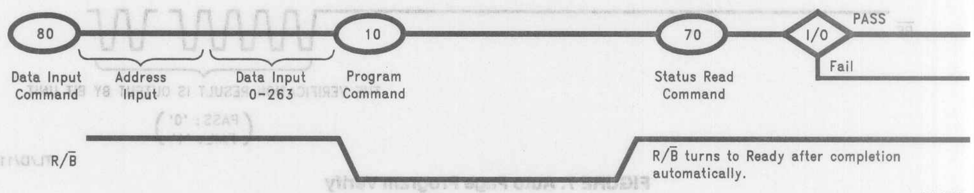

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FIGURE 9. Auto Page Program Sequence

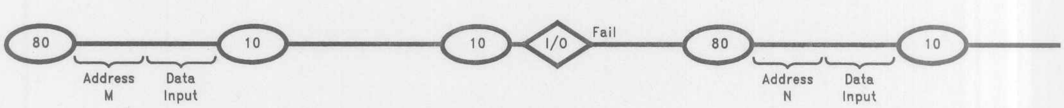

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FIGURE 10. Program Fail Sequence

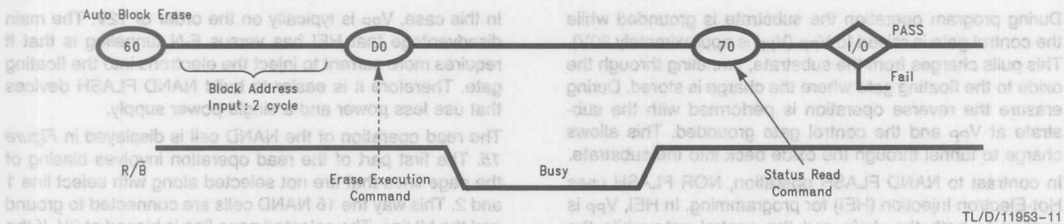

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FIGURE 11. Auto Block Erase Command Sequence

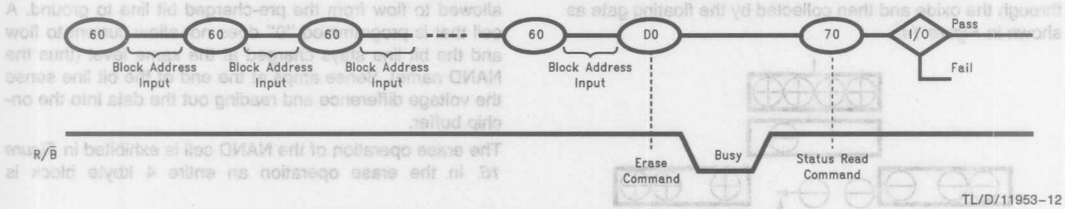

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FIGURE 12. Auto Multi-Block Erase Command Sequence

The NM29N16 allows data to be written to a page when there is less than 264 bytes. Up to 10 sections of the same page may be written to at different times. For example, the system may write 25 bytes to the first part of the page, call them D0–D24. The rest of the page of filled with "1" (FFH) and then programmed. A second 25 bytes can then be stored at D24–D49. Again the rest of the page is filled with "1" along with D0–D24. In this manner, the data that was previously programmed into D0–D24 is masked out from being reprogrammed. The benefit to the system designer is the ability to be able to store small amounts of data in a page and not to waste memory space.

Finally, the NM29N16 allows page to page transfers. However, when this is done the data that is reprogrammed into the new page is inverted ("0" → "1" and "1" → "0").

ERASE

The NM29N16 has two modes for block erasure. These are Auto Block Erase and Auto Multi-Block Erase. Two different commands are used in the erase procedure to prevent accidental erasure. These are 60H to set up the Auto Block Erase and D0H to execute the Erase command. The NM29N16 provides one of the smallest erase block sizes in the industry at 4 kbytes.

The Auto Block Erase, like the Program command, uses an algorithm to handle the entire erase procedure. This helps minimize the work load on the processor. The command sequence for a single block erase is shown in *Figure 11.*

It starts by writing the 60H command to the device followed by the two cycle address, which represents the block to be erased. The Erase Execution (D0H) command is then written to confirm the erasure. The R/B̄ signal line will drop low for approximately 6 ms while the erase operation is in progress. When the R/B̄ line returns high, the status of the erasure can be checked by issuing the Status Read (70H) command. If the erasure fails (I/O1 outputs "1") then the block should be marked as bad and no further operations should take place on this block.

The Auto Multi-Block Erase operation allows the system to mark multiple random blocks to be erased. A similar sequence as the single block erasure is followed as seen in *Figure 12.*

After the first address is inputted, it is followed by another 60H command and a second two cycle block address. This process can be repeated to mark as many blocks for erasure as is desired. When all the blocks have been marked the D0H command is finally inputted and the erasure commences (R/B̄ goes low). The total erase time will be 6 ms plus 15 μs times the number of blocks that have been marked for erasure.

PHYSICS OF OPERATION

The NM29N16 utilizes a different architecture and programming method than the traditional NOR FLASH devices. The main difference in the programming method is the use of Fowler-Nordhiem tunneling for both programming and erasure of the cells. The physical operation behind reading, writing and erasing the NAND device at the cell level is explained in the following sections.

First an explanation of how Fowler-Nordhiem (F-N) tunneling operates is necessary. *Figure 13* shows a typical cross-section of a single NAND FLASH cell.

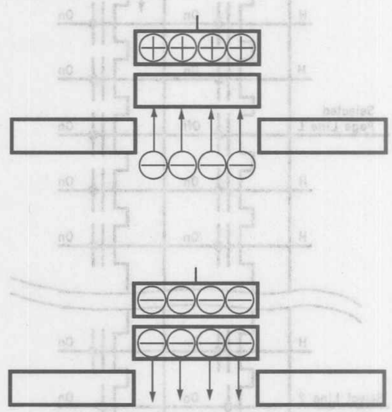

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FIGURE 13. NAND Cell Program/Erase

During program operation the substrate is grounded while the control gate is raised to V_{PP} (V_{PP} is approximately 20V). This pulls charges from the substrate, tunneling through the oxide to the floating gate where the charge is stored. During erasure the reverse operation is performed with the substrate at V_{PP} and the control gate grounded. This allows charge to tunnel through the oxide back into the substrate.

In contrast to NAND FLASH operation, NOR FLASH uses Hot-Electron Injection (HEI) for programming. In HEI, V_{PP} is applied to both the drain and the control gate while the source is grounded. In this case the charge is injected through the oxide and then collected by the floating gate as shown in *Figure 14.*

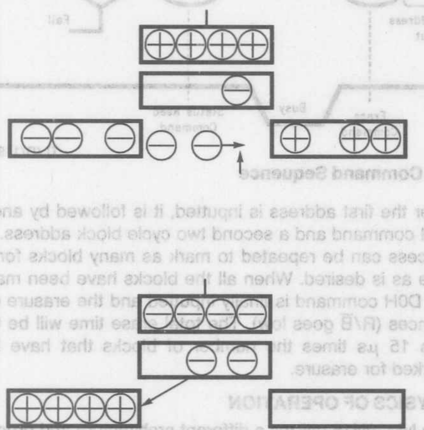

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FIGURE 14. NOR FLASH Cell Program/Erase

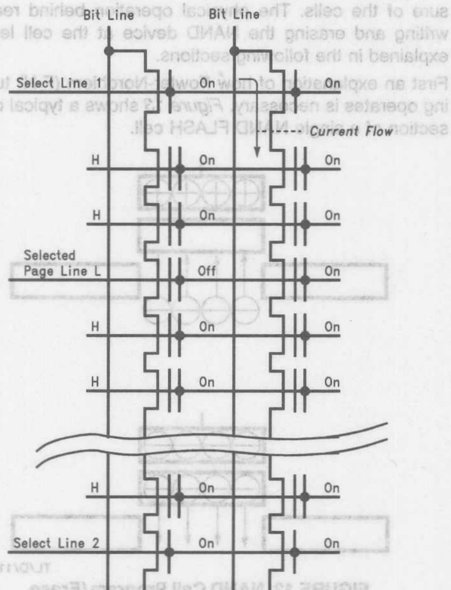

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FIGURE 15. NAND FLASH Read Operation

In this case, V_{PP} is typically on the order of 12V. The main disadvantage that HEI has versus F-N tunneling is that it requires more current to inject the electrons into the floating gate. Therefore it is easier to build NAND FLASH devices that use less power and a single power supply.

The read operation of the NAND cell is displayed in *Figure 15.* The first part of the read operation involves biasing of the page lines that are not selected along with select line 1 and 2. This way the 16 NAND cells are connected to ground and the bit line. The selected page line is biased at 0V. If the floating gate transistor cell is programmed "1", current is allowed to flow from the pre-charged bit line to ground. A cell that is programmed "0" does not allow current to flow and the bit line stays charged at the same level (thus the NAND name). Sense amps at the end of the bit line sense the voltage difference and reading out the data into the on-chip buffer.

The erase operation of the NAND cell is exhibited in *Figure 16.* In the erase operation an entire 4 kbyte block is

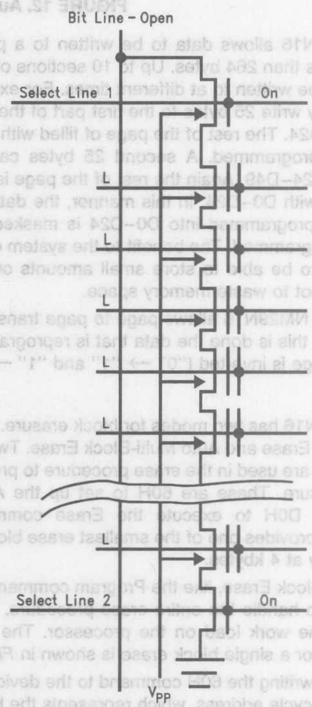

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FIGURE 16. NAND FLASH Erase Operation

The NAND FLASH program operation also uses an algorithm to monitor the procedure. *Figure 17* shows the operation. First, select line 1 is turned on connecting the 16 NAND cells to the bit line while select line 2 is set low disconnecting the line from ground. Next, a high voltage (approximately 10V) is applied to all the page lines of the block except the page line that is to be programmed. The page line that is to be programmed is set at V_{PP} (approximately 20V). If data is to be programmed into the cell, the bit line is set low. This causes a differential of approximately 20V between the control gate and the substrate, allowing for tunneling into the floating gate. If the cell is not to be programmed, the bit line is set at approximately 10V. This causes the differential between the control gate and channel to be only 10V which is not enough to cause tunneling. Again the automatic program algorithm monitors the process for complete programming of the cells.

POTENTIAL APPLICATIONS

It should be clear from the above description of the NM29N16 that the device is very flexible in the manner in which it may be used. This makes it an ideal device for numerous applications that require large amounts of bulk data storage or secondary memory storage. Systems that need to store audio, visual or data files, and need to be portable are prime candidates to use NAND FLASH.

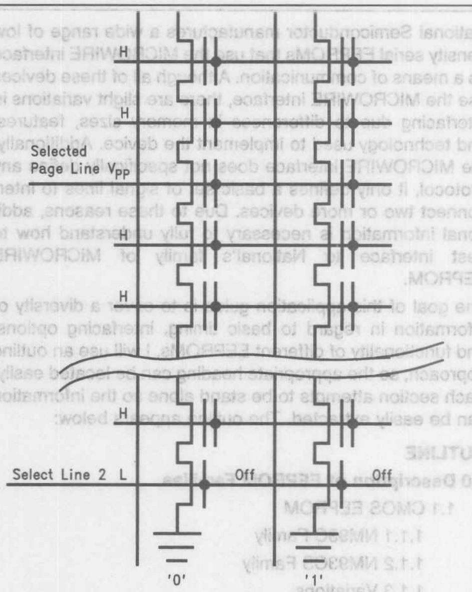


FIGURE 17. NAND FLASH Program Operation

Using National's MICROWIRE™ EEPROM

National Semiconductor
Application Note 758
Paul Lubeck

National Semiconductor manufactures a wide range of low density serial EEPROMs that use the MICROWIRE interface as a means of communication. Although all of these devices use the MICROWIRE interface, there are slight variations in interfacing due to differences in memory sizes, features, and technology used to implement the device. Additionally, the MICROWIRE interface does not specifically define any protocol, it only defines a basic set of signal lines to interconnect two or more devices. Due to these reasons, additional information is necessary to fully understand how to best interface to National's family of MICROWIRE EEPROM.

The goal of this application guide is to cover a diversity of information in regard to basic timing, interfacing options, and functionality of different EEPROMs. I will use an outline approach, so the appropriate heading can be located easily. Each section attempts to be stand alone so the information can be easily extracted. The outline appears below:

OUTLINE

1.0 Description of EEPROM Families

1.1 CMOS EEPROM

National builds a range of MICROWIRE CMOS EEPROMs in memory sizes ranging from 256-bit to 4906-bit. The NM93C family is the base family and the NM93CS is a similar family with additional features, there are also other devices with slight variations on the interface. All these devices are available with certain "standard" options such as operating temperature ranges and operating voltage ranges, packaging options and test options. These options being fairly standard variations for semiconductor devices, will not be addressed beyond this. The purpose of this article is to address basic functionality and interfacing, including various tricks to simplify or modify the interface.

1.1.1 NM93C Family

The NM93C family of EEPROM is available in 256-, 1024-, 2048-, and 4096-bit sizes. All of these are internally organized in 16-bit words, therefore all data transactions deal with 16 bits. This family of EEPROMs has 7 instructions that deal with read, write, and a basic level of data protection. The instructions are listed in Table I. It is important to note that there is a basic difference in length of the instruction between the NM93C06 or NM93C46 and the NM93C56 or NM93C66. This is due to the larger devices needing additional address bits.

The NM93C family of EEPROM, like all of National's serial EEPROMs have a basic level of write protection that can be turned on or off by the use of the ERASE/WRITE DISABLE (EWDS) and ERASE/WRITE ENABLE (EWEN) instructions. Although there are two erase instructions included in the NM93C family, these are included only for compatibility with older EEPROMs that require erase before write. These EEPROMs don't require erase before write and it is recommended that in application the erase not be used as this adversely affects endurance.

1.1.2 NM93CS Family

The NM93CS EEPROMs are identical to the NM93C family in memory sizes and organization. Making them different, they have two additional functions, sequential read and user configurable write protection, and don't have either of the erase functions, ERASE and ERASE-ALL as they are not needed. Like all of the CMOS EEPROMs, these have self timed programming cycles and operate from a single external supply of either 4.5V to 5.5V or 2.0V to 5.5V. In these devices it is necessary to eliminate the erase cycles from the code as they may adversely affect the performance of the device.

As these have additional functions, the instruction set includes a total of 10 instructions, 3 that operate on the memory array, 2 that deal with the basic write protection and 5 that deal with the user configurable write protection. Refer

to the NM93CS instruction set table (Table II) for definitions of these instructions. As with the NM93C family, there is a basic difference in instruction length depending on memory size.

To further increase data security in these EEPROMs there are also two additional input signals defined, Program Enable (PE) and Protect Register Enable (PRE). These signals are on pins that are unused on the NM93C family providing upward compatibility to the NM93CS devices.

TABLE I. NM93C Family Instruction Set Table

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7/A5–A0		Reads data stored in memory.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
ERASE	1	11	A5–A0		Erase register A5A4A3A2A1A0.
WRITE	1	01	A5–A0	D15–D0	Writes register.
ERAL	1	00	10XXXX		Erase all registers.
WRAL	1	00	01XXXX	D15–D0	Writes all registers.
EWDS	1	00	00XXXX		Disables all programming instructions.

TABLE II. NM93CS Family Instruction Set Table

Instruction	SB	Op Code	Address	Data	PRE	PE	Comments
READ	1	10	A5–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	1	00	11XXXX		0	1	Write enable must precede all programming modes.
WRITE	1	01	A5–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	1	00	01XXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WDS	1	00	00XXXX		0	X	Disables all programming instructions.
PRREAD	1	10	XXXXXX		1	X	Reads address stored in Protect Register.
PREN	1	00	11XXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	1	11	111111		1	1	Clears the Protect Register so that no registers are protected from WRITE.
PRWRITE	1	01	A5–A0		1	1	Program address into Protect Register. Thereafter, memory addresses ≥ the address in Protect Register are protected from WRITE.
PRDS	1	00	000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

hancements. The first enhancement is a Organization (ORG) input that allows the user to select the internal configuration of the memory as either 8 bits wide or 16 bits wide. When the input is high or unconnected, the device is configured as 16 bits wide, when the ORG input is at a low level, the memory is configured as 8 bits wide, but twice as deep. The feature is present on both the NM93C46A and the NM59C11.

The second variation is the STATUS output. This is the Busy/Ready polling to indicate programming status. All other devices have this feature on the Data-Out (DO) output, the NM59C11 alone has status available as a separate output and not on the Data-Out output. This can simplify interfacing to a bidirectional data bus.

2.0 Hardware Connection

2.1 INTERFACE PIN DESCRIPTIONS

In this section, each possible input or output will be described followed by the most popular variations of bus connections. Not all devices have all of the described I/Os. The I/Os are available according to Table III, I/O Functionality.

2.1.1 CHIP SELECT (CS)

Chip Select is used to differentiate between various devices on the same Microwire bus. In the case of EEPROM it cannot be tied high even if it is the only device on the bus as it performs several additional functions. As it applies to any of the Microwire EEPROMs, the rising edge resets the internal circuitry of the device, a function necessary prior to initiating any new cycle. As shown in the functional block diagram *(Figure 1)* chip select also gates the data input and clock input, thus disabling these functions.

the cycle will have to be started again with a new start bit.

During programming cycles chip select initiates the internal programming cycle. The falling edge of chip select will start the internal programming cycle when a programming opcode has been entered (Erase, Write, Erase All, Write All) and then, in conjunction with Data-Out (DO), will indicate if programming is complete (except the NMOS NMC9306). If programming is complete, Data-Out will drive high, if incomplete it will drive low. In the case of the NMC9306, the user must provide the programming time and in this case chip select must be held low for a minimum of 10 ms, then brought high and clocked to end the programming cycle.

Several additional notes in regard to chip select:

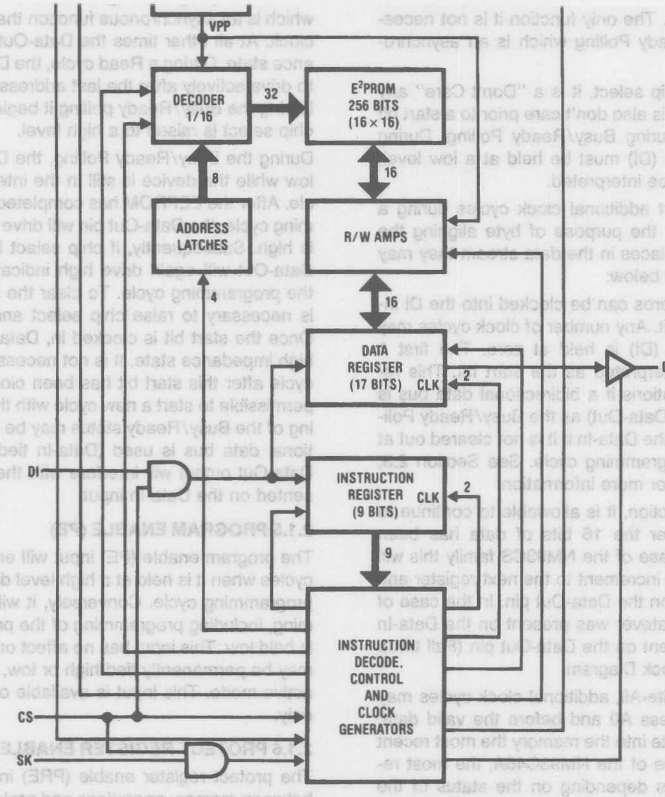
If a programming cycle is partially clocked in and then chip select dropped, the EEPROM may enter into a programming mode. This is determined by how many bits have been clocked in when chip select is dropped. If the start bit, opcode, and all of the address has been clocked in, a programming cycle will be initiated with no or partial data. If less than a complete address has been clocked in, the programming cycle will not be initiated. Refer to *Figure 2*, reference line 1.

In the case of the NM59C11, a programming cycle will not be entered unless a full data field has been clocked in. A full data field may be either 8 or 16 bits depending on the logic level present at the ORG input. A programming cycle will be entered at reference line 2 in *Figure 2* for the NM59C11.

Chip select hold time at the end of a cycle is referenced to the last rising edge of clock (SK). The hold time from the rising edge is the same as the minimum SK high time for the particular device. This is stated in the datasheets as 0 ns hold time from the falling edge of SK which assumes that SK high time is always minimum. In this case SK can be left in the high state or taken low at a later time. Internally chip select gates SK, therefore SK is not critical.

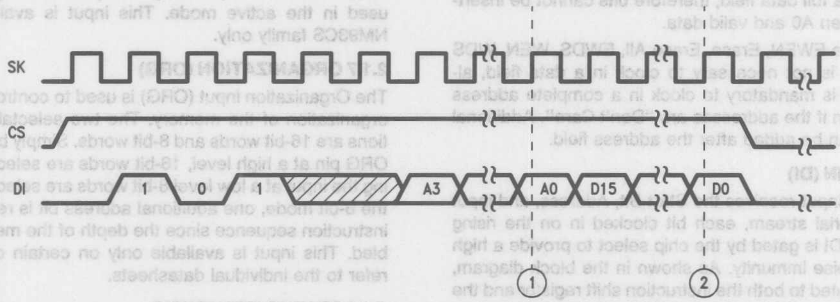
TABLE III. I/O Functionality by Device

	CS	SK	DI	DO	PE	PRE	ORG	STAT
NM93C Family	X	X	X	X				
NM93CS Family	X	X	X	X	X	X		
NM93C46A	X	X	X	X			X	
NM59C11	X	X	X	X			X	X



TL/D/11169–1

FIGURE 1. Block Diagram



TL/D/11169–2

FIGURE 2. Programming Cycle Point of No Return

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2.1.2 SERIAL CLOCK (SK)

The clock input is used to clock all data, address, op-code, and start bits into or out of the EEPROMs. SK clocks both input and output on the rising edge only, the falling edge has no effect on the devices. The only function it is not necessary for is the Busy/Ready Polling which is an asynchronous function.

Since SK is gated by ship select, it is a "Don't Care" any time chip select is low. It is also don't care prior to a start bit being clocked in and during Busy/Ready Polling. During these conditions Data-In (DI) must be held at a low level, otherwise a start bit will be interpreted.

If it is desirable to insert additional clock cycles during a instruction sequence for the purpose of byte aligning the data, there are several places in the data stream they may be inserted as described below:

— On any instruction, zeros can be clocked into the DI input before the start bit. Any number of clock cycles may be added if Data-In (DI) is held at zero. The first 1 clocked in will be interpreted as the start bit. This requires special precautions if a bidirectional data bus is used (Data-In tied to Data-Out) as the Busy/Ready Polling will interfere with the Data-In if it is not cleared out at the end of each programming cycle. See Section 2.3, THREE WIRE BUS, for more information.

— During a Read instruction, it is allowable to continue to clock the device after the 16 bits of data has been clocked out. In the case of the NM93CS family this will cause the memory to increment to the next register and present its contents on the Data-Out pin. In the case of all other devices, whatever was present on the Data-In pin will become present on the Data-Out pin (Fall thru). Refer to *Figure 1,* Block Diagram.

— During a Write or Write-All, additional clock cycles may be added after address A0 and before the valid data. The EEPROM will write into the memory the most recent 16 bits, or in the case of the NM93C46A, the most recent 8 bits or 16 bits depending on the status of the ORG input. Adding additional clocks after the valid data will cause the data to be misaligned. In the case of the NM59C11, the device counts the data bits clocked in and automatically enters the programming mode when it receives a full data field, therefore bits cannot be inserted between A0 and valid data.

— During the EWEN, Erase, Erase All, EWDS, WEN, WDS cycles, it is not necessary to clock in a data field, although it is mandatory to clock in a complete address field, even if the addresses are "Don't Care". Additional clocks can be added after the address field.

2.1.3 DATA-IN (DI)

The Data-In input receives the Start-Bit, Address, and input data in a serial stream, each bit clocked in on the rising edge of SK. DI is gated by the chip select to provide a high degree of noise immunity. As shown in the block diagram, Data-In is routed to both the instruction shift register and the data shift register. When the start bit is clocked into the last bit of the instruction register, the clock is switched to the data register to receive input data and clock data out simultaneous. The Data-Out remains in high impedance unless a read cycle or Busy/Ready status is being done. The safest state is to keep the Data-In pin in a low level as a start bit is a high level.

2.1.4 DATA-OUT (DO)

The Data-Out (DO) output sends read data onto the microwire bus and is clocked out on the rising edge of SK. It also carries the programming status after a programming cycle which is an asynchronous function that does not require the clock. At all other times the Data-Out is in the high impedance state. During a Read cycle, the Data-Out output begins to drive actively after the last address bit (A0) is clocked in. During the Busy/Ready polling it begins to drive active after chip select is raised to a high level.

During the Busy/Ready Polling, the Data-Out output drives low while the device is still in the internal programming cycle. After the EEPROM has completed the internal programming cycle, the Data-Out pin will drive high when chip select is high. Subsequently, if chip select is brought high again, Data-Out will again drive high indicating it has completed the programming cycle. To clear the Busy/Ready Polling it is necessary to raise chip select and clock in a start bit. Once the start bit is clocked in, Data-Out will return to the high impedance state. It is not necessary to continue with a cycle after this start bit has been clocked in, although it is permissible to start a new cycle with this start bit. This clearing of the Busy/Ready status may be necessary if a bidirectional data bus is used (Data-In tied to Data-Out) as the Data-Out output will interfere with the new data being presented on the Data-In input.

2.1.5 PROGRAM ENABLE (PE)

The program enable (PE) input will enable all programming cycles when it is held at a high level during the duration of a programming cycle. Conversely, it will disable all programming, including programming of the protect register, while it is held low. This input has no affect on any other cycle, so it may be permanently tied high or low, or may be used in an active mode. This input is available on the NM93CS family only.

2.1.6 PROTECT REGISTER ENABLE (PRE)

The protect register enable (PRE) input is used to switch between memory operations and protect register operations since the same op-codes are used for both. With the PRE input high, the op-codes define operations in the protect register, with the PRE input low, the op-codes define operations in the memory. This pin may be tied high or low, or used in the active mode. This input is available on the NM93CS family only.

2.1.7 ORGANIZATION (ORG)

The Organization input (ORG) is used to control the internal organization of the memory. The two selectable organizations are 16-bit words and 8-bit words. Simply by holding the ORG pin at a high level, 16-bit words are selected, by holding the input at a low level 8-bit words are selected. When in the 8-bit mode, one additional address bit is required in the instruction sequence since the depth of the memory is doubled. This input is available only on certain device types, refer to the individual datasheets.

2.1.8 STATUS (RDY/BUSY)

The status output indicates the programming cycle status after a programming cycle. When the device is in the programming mode and therefore cannot accept any other cycles, this pin will be low. After completion of the cycle the STATUS pin will be driven high. When this function is present, the Busy/Ready Polling is not available on the Data-Out

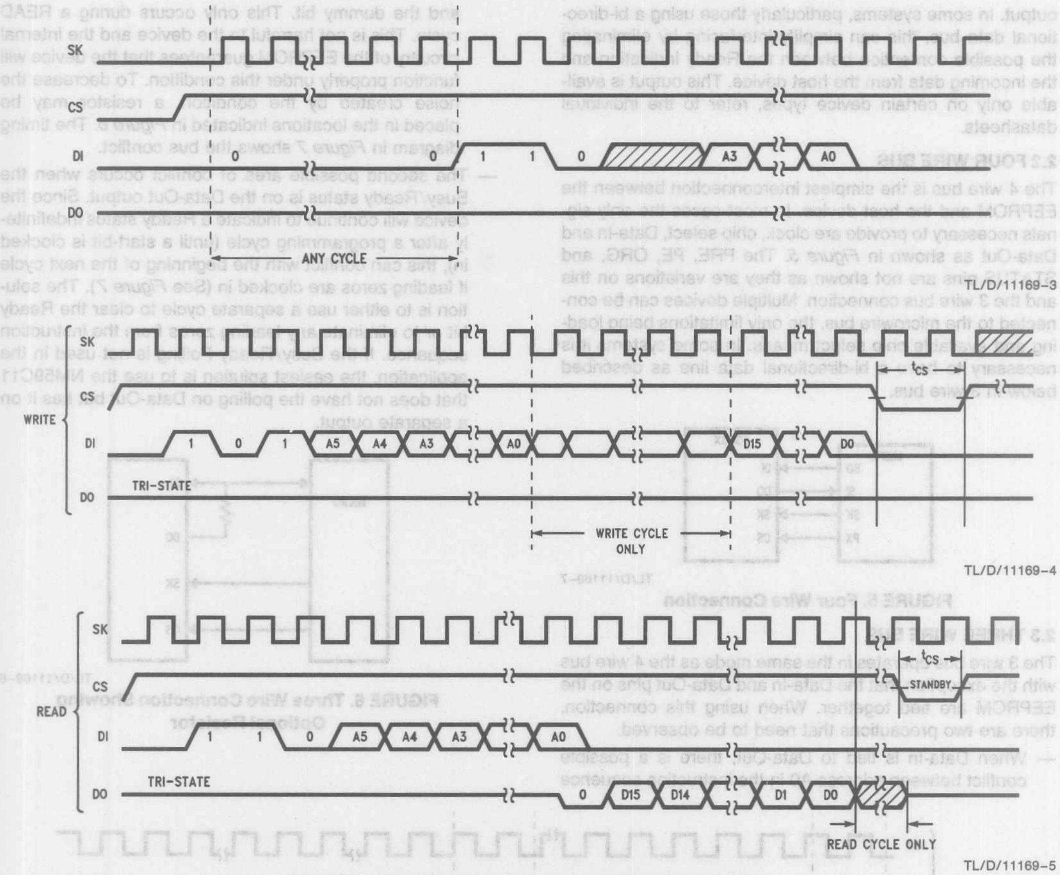

FIGURE 3. Possible Locations for Additional SK Cycles

output. In some systems, particularly those using a bi-directional data bus, this can simplify interfacing by eliminating the possible contention between the Ready indication and the incoming data from the host device. This output is available only on certain device types, refer to the individual datasheets.

2.2 FOUR WIRE BUS

The 4 wire bus is the simplest interconnection between the EEPROM and the host device. In most cases the only signals necessary to provide are clock, chip select, Data-In and Data-Out as shown in *Figure 5*. The PRE, PE, ORG, and STATUS pins are not shown as they are variations on this and the 3 wire bus connection. Multiple devices can be connected to the microwire bus, the only limitations being loading and available chip select means. In some systems it is necessary to have a bi-directional data line as described below in 3 wire bus.

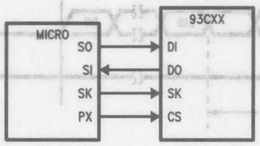

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FIGURE 5. Four Wire Connection

2.3 THREE WIRE BUS

The 3 wire bus operates in the same mode as the 4 wire bus with the exception that the Data-In and Data-Out pins on the EEPROM are tied together. When using this connection, there are two precautions that need to be observed.

— When Data-In is tied to Data-Out, there is a possible conflict between address A0 in the instruction sequence and the dummy bit. This only occurs during a READ cycle. This is not harmful to the device and the internal circuitry of the EEPROM guarantees that the device will function properly under this condition. To decrease the noise created by the condition, a resistor may be placed in the locations indicated in *Figure 6*. The timing diagram in *Figure 7* shows the bus conflict.

— The second possible area of conflict occurs when the Busy/Ready status is on the Data-Out output. Since the device will continue to indicate a Ready status indefinitely after a programming cycle (until a start-bit is clocked in), this can conflict with the beginning of the next cycle if leading zeros are clocked in (See *Figure 7*). The solution is to either use a separate cycle to clear the Ready bit or to eliminate any leading zeros from the instruction sequence. If the Busy/Ready Polling is not used in the application, the easiest solution is to use the NM59C11 that does not have the polling on Data-Out but has it on a separate output.

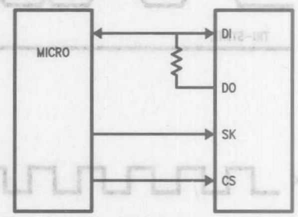

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FIGURE 6. Three Wire Connection Showing Optional Resistor

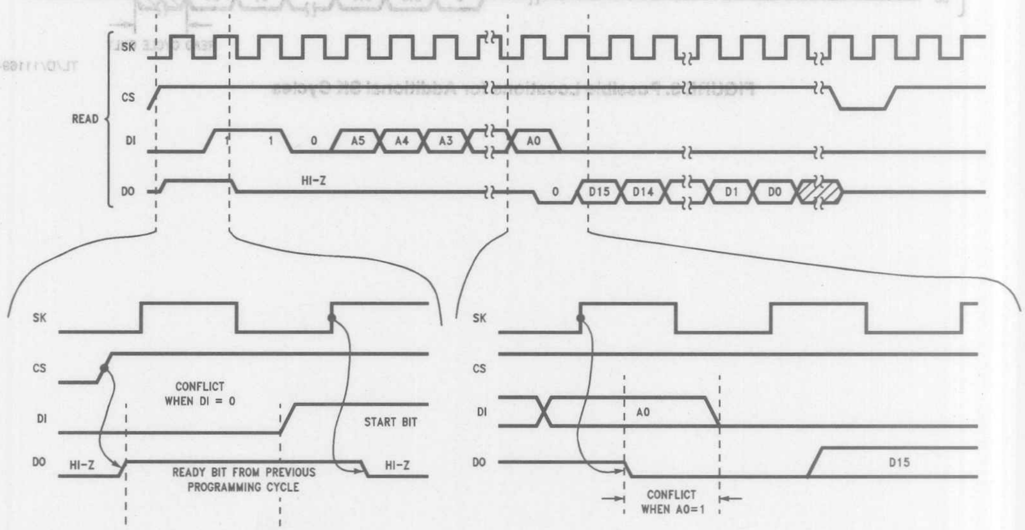

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FIGURE 7. Three Wire Connection Bus Conflict Areas

basic timings with respect to the clock (SK) will be described, followed by instruction sequence timing, and finally, specific information in each instruction sequence.

3.1. BUS TIMING

The synchronous data timing shown in *Figure 8* is similar to that shown in the various datasheets. There is one significant modification to the timing specification though, the chip select (CS) hold time is referenced to the rising edge of the clock rather than the falling edge. With this modification, the hold time specification must be changed to be the same as

— The only time the clock is necessary is when clocking data into or out of the EEPROM. It is not necessary during Busy/Ready Polling.

— The clock may be left in either the high state or low state between cycles. It is safer to leave the clock in the low state.

— When chip select (CS) is high, clock (SK) is a critical signal. With the exceptions noted in Section 2.1.2 tilted SERIAL CLOCK (SK), no additional clock cycles or noise that crosses the V_{IH} or V_{IL} thresholds can be tolerated.

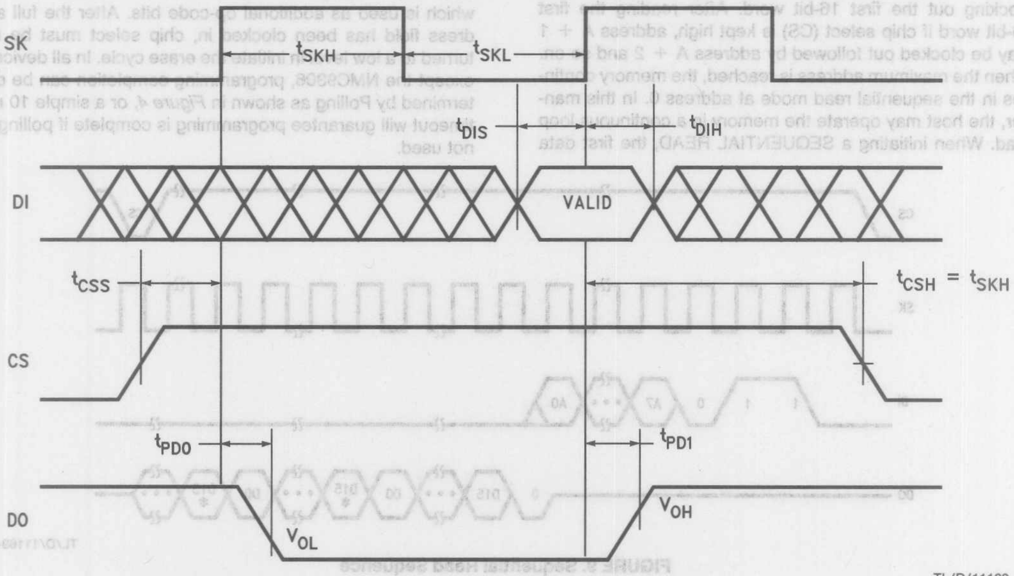

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FIGURE 8. Synchronous Timing

4

3.2 INSTRUCTION SEQUENCE DESCRIPTIONS

3.2.1 READ CYCLE

The READ cycle requires the host to raise chip select (CS) and then clock in thru the Data-In (DI) pin a start-bit, op-code, and address. Following clocking in the last address bit, the Data-Out (DO) output comes out of the high impedance state and drives a low level on the output. This is referred to as the dummy bit and is a good indication that a READ mode has been successfully entered if difficulty is encountered during initial debug of a system. The dummy bit is clocked out of the EEPROM on the same rising edge of SK that clocks in the last address bit, A0. This is shown in *Figure 9.*

3.2.2 SEQUENTIAL READ

Sequential read is a read mode available only on the NM93CS family. It is entered by entering a READ cycle and clocking out the first 16-bit word. After reading the first 16-bit word if chip select (CS) is kept high, address A + 1 may be clocked out followed by address A + 2 and so on. When the maximum address is reached, the memory continues in the sequential read mode at address 0. In this manner, the host may operate the memory in a continuous loop read. When initiating a SEQUENTIAL READ, the first data word is proceeded by a dummy bit as in a standard READ, although the dummy bit is supressed in all subsequent data words as shown in *Figure 9.*

3.2.3 ERASE AND ERASE ALL

The ERASE cycles return the contents of the EEPROM to a clear state which is read as 1's. It is not necessary for any of the CMOS EEPROM described in this article, and is included in the NM93C family, NM93C46A, and NM59C11 only for compatibility with older devices that require erasing. It is recommended that the erase cycles be eliminated from the instructions to simplify the code, speed up writing and to improve the endurance obtained in the application. These modes are entered by clocking in a start-bit, op-code, and address. It is not necessary to clock in the data field as it is assumed to be all 1's. It is necessary to clock in the address, even in the case of ERASE-ALL where it is "don't care" in all except the first two bits of the address field which is used as additional op-code bits. After the full address field has been clocked in, chip select must be returned to a low level in initiate the erase cycle. In all devices, except the NMC9306, programming completion can be determined by Polling as shown in *Figure 4,* or a simple 10 ms timeout will guarantee programming is complete if polling is not used.

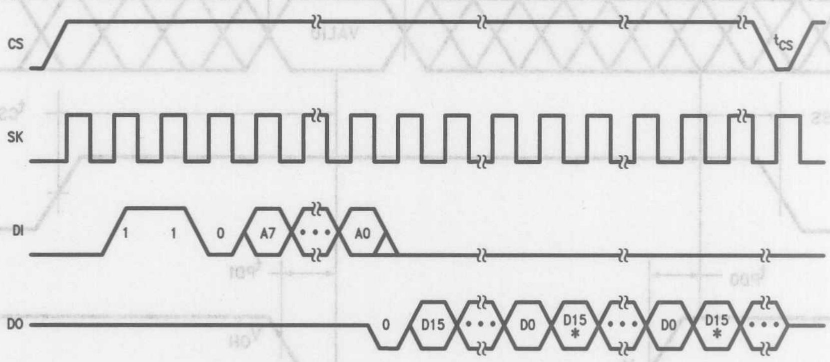

FIGURE 9. Sequential Read Sequence

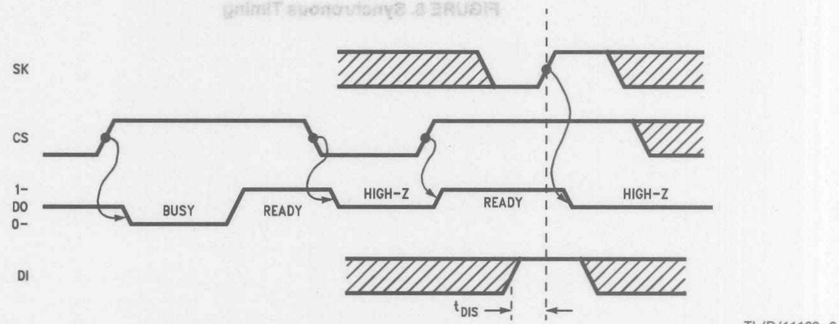

FIGURE 4. Busy/Ready Polling Sequence

3.2.4 WRITE AND WRITE ALL

The Write and Write All cycles will write a specified data word into the specified address, or in the case of Write All, the same data pattern will be written into all locations. In all devices a new data pattern may be directly written over an existing data pattern without erasing the first data pattern. The write mode is entered by clocking in a start-bit, op-code, address, and data. The full address field must be clocked in for the Write All even though it is don't care in all but the first 2 bits. It is also necessary to clock in a full data field to assure correct alignment of data. The write cycle will be initiated after 8- or 16-bit have been clocked into the device in some of the devices and in other devices after chip select is brought low regardless of how many data bits have been clocked in. Refer to the specific datasheets to determine which method is used.

3.2.5 PROGRAM ENABLE AND PROGRAM DISABLE

Program enable and program disable are the instructions that enable or disable writing and, where included, erasing. The instruction name varies depending on the specific device but includes EWEN, EWDS, WEN, and WDS. These instructions enable or disable the entire memory array with a single instruction. All devices power up in the disable mode and once placed in the enabled mode remain enabled until a disable instruction is performed or V_{CC} is cycled. These instructions provide the most basic level of data protection. Although since most lost data is the result of the host device becoming uncontrolled and performing the "Program Subroutine" it may be helpful to structure the software such that the enable command is not included in the "Program Subroutine" but is in a separate subroutine. If a greater degree of data security is needed, a NM93CS family device is recommended, or other more elaborate schemes involving redundant data storage and polling.

3.2.6 PROTECT REGISTER READ

The protect register read (PRREAD) command is the same as a word read command except the input PRE must be held at a high level and the address is don't care. In spite of the address being don't care, the entire address field must be clocked in. On the Data-Out pin the contents of the protect register will be clocked out MSB first descending to LSB.

3.2.7 PROTECT REGISTER ENABLE

Similar to the programming enable instructions described above, the PREN instruction is necessary to perform any programming instruction the affects the Protect Register. Unlike the enable instructions described above, a PREN must immediately proceed each programming instruction that involves the protect register. The Protect Register programming instructions are PRCLEAR, PRWRITE, and PRDS.

3.2.8 PROTECT REGISTER DISABLE

The protect register disable instruction permanently disables any further programming instructions to the protect register. Therefore it can only be performed once in the lifetime of a NM93CS device. The purpose of it is to permanently configure a portion of the EEPROM as true ROM and a portion as Read/Write EEPROM. Great caution should be exercised prior to executing this instruction as there is no second chance. It is performed by sending a start-bit, op-code and an address field of all 0's while both the PRE and PE inputs are at a high level. This instruction must be immediately proceeded by a PREN instruction.

3.2.9 PROTECT REGISTER CLEAR

The protect register clear instruction will clear the contents of the Protect Register making the entire contents of the EEPROM alterable only if the PRDS instruction has not previously been executed. This is done by clocking in a start-bit, op-code, and address field of all ones. This instruction must be immediately proceeded by PREN instruction and requires that both PRE and PE inputs be held at a high level.

3.2.10 PROTECT REGISTER WRITE

The Protect Register write command (PRWRITE) allows the host to write the protect register with the address where the memory is to be segmented into ROM and EEPROM. The defined address is the first ROM address and the ROM field then continues to the top of memory. To execute this command a start-bit, op-code, and address must be clocked in, the address field containing the memory address that defines the ROM/EEPROM boundary. The PRE and PE inputs must be held at a high level.

3.3 INTERFACING SOLUTIONS

When interfacing serial microwire EEPROMs to microcontrollers there is an apparent conflict that occurs when selecting clock polarity and phase. This can be easily overcome in most situations, although when using some microcontrollers that do not allow selection of either clock polarity or clock phase, the only solution may be to resort to bit set and bit reset instructions to interface to the EEPROM rather than use of the serial interface provided on the microcontroller.

In the instance where there is a dedicated serial interface provided, the conflict typically occurs as follows. *Figure 10* demonstrates an EEPROM READ as this involves data being transferred from the micro to the EEPROM (Start bit, op-code, and address) and data transferred from the EEPROM to the micro (address contents). The conflict occurs in this example when the micros clock sets data up on the falling edge of SK and expects the EEPROM to accept it on the rising edge, but then expects the EEPROM to do the same when it sends data back to the micro.

1. The micro sets up a data bit. A propagation delay after the falling edge the data bit is valid at the EEPROM DI pin.
2. The EEPROM uses the rising edge of SK to clock the data bit into its internal register.
3. When the data direction changes the EEPROM sets the data up starting at the rising edge of SK.
4. The micro attempts to clock the data bit in that was set up on clock edge 3.

This example will work if the micro requires 20 ns or less data hold time after edge 4. If greater than 20 ns is required, an alternate strategy is needed.

1a. The micro sets up the data bit on the rising edge and a propagation delay later it is valid at the EEPROM.

2a. The EEPROM clocks the data into its internal register. The EEPROM requires only 10 ns data hold time, which can normally be guaranteed.

and hold time is guaranteed for the micro based on the minimum high and low time of the SK clock used in the application.

It should be noted that in the second example, CS (chip select) is asserted when SK is low. If this cannot be done, the DI input should be low when CS is asserted. If both DI and SK are high when CS is asserted the EEPROM will

4.0 Conclusion

The serial EEPROM offered by National all share a common structure. Separating them are various features that give benefit to various applications such as the need for a bi-directional data bus or need for one byte word width. There are a number of "tricks" that may simplify interfacing to these which can easily be understood with the help of a functional block diagram. Given this information the overall job of using a serial interface EEPROM will be simpler.

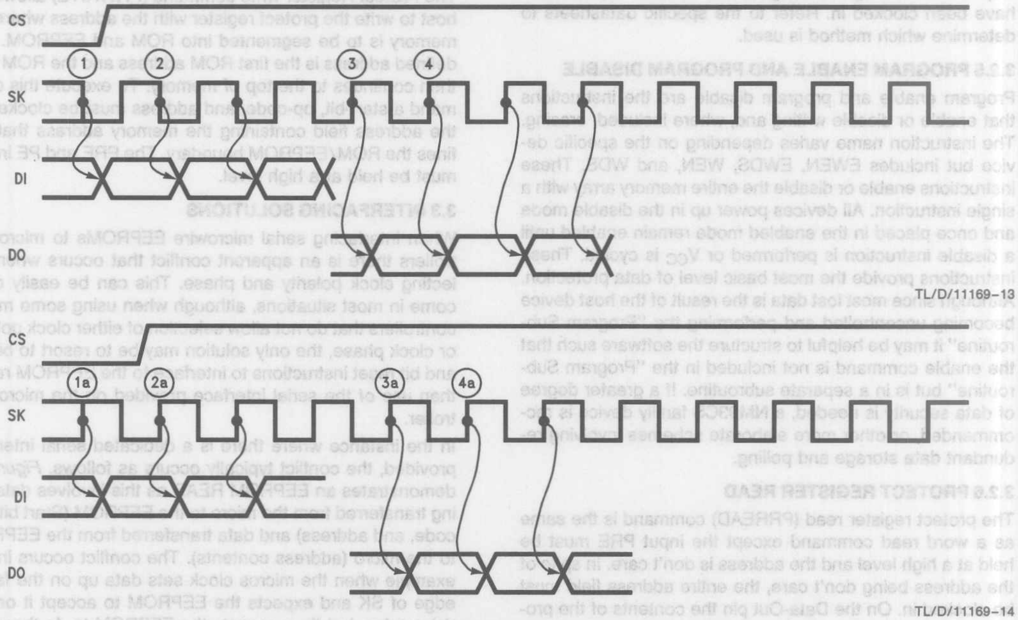

FIGURE 10

Microcontrollers to National's MICROWIRE™ EEPROMs

ABSTRACT

National's NM93Cxx and NM93CSxx family of serial EEPROMs have MICROWIRE "slave" interfaces that directly connect to the MICROWIRE "master" interfaces on the COP800 family of 8-bit microcontrollers. Peak data transfer rates are as high as 1 MB on the 4 wire MICROWIRE bus. This application note includes the essential assembly language software to address MICROWIRE EEPROMs.

HARDWARE INTERFACE

A schematic for connecting a COP800 family microcontroller to one of Nationals NM93Cxx family MICROWIRE EEPROMs via the microcontrollers dedicated MICROWIRE port is shown in *Figure 1.* National makes two basic families of MICROWIRE EEPROMs, the classic NM93**C**xx series and the newer full featured NM93**CS**xx series. The NM93CSxx series EEPROMs have a sequential read capability and the "S" in "CS" stands for sequential (the "C" implies CMOS). As can be seen the "CS" series devices have two additional pins which control write protect features (consult a data sheet for information on their function). By connection these pins to V_{CC} and GND as shown in *Figure 2*, it becomes possible to use either "C" or "CS" family parts in the same physical socket. This would be desirable if a change from a "C" series part to a "CS" series part is possible for reasons of product upgrades or simply manufacturing inventory control. Pins 6 and 7 on the "C" series parts are true no connects and thus can be tied to V_{CC} or ground harmlessly.

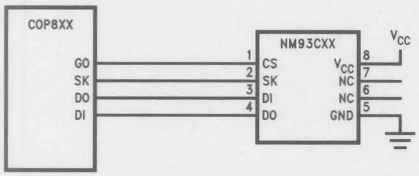

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FIGURE 1. Basic National MICROWIRE Interconnection to a COP800 Family Part

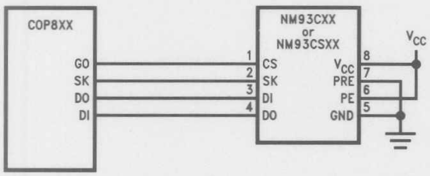

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FIGURE 2. This schematic allows either a NM93Cxx or NM93CSxx part to be used in the same socket. Software can then be adjusted to take advantage of the "CS" series advantages without making changes to the board.

If it's desirable to use both types in the same socket without being forced to make software changes, one must be careful not to use the sequential read capability of the "CS" series. Both types of parts should be tested in the socket before the software is frozen.

NM93C06 to COP8XX Family Software Details

Always consult the latest data sheets for information about timing variables mentioned in the text that follows. These numbers were correct at the time that this application note was written but are subject to change.

1. The SK clock frequency must not exceed 1 MHz. Consult the processor data sheet for details.
2. The CS low time following a write must exceed 250 ns. This starts the internally timed write operation. The DO line will leave the high impedance state if CS goes high again and will drive low until the internal write cycle is complete. After DO returns high, indicating "ready" the first rising edge of SK with CS high and DI high will return the DO pin to the high impedance condition. This condition is normally the start bit of the next instruction.

   The DO pin will be low for up to 10 ms and then go high to indicate that the write is complete. If a new instruction is attempted before the DO pin returns high it will be ignored and the DO pin will not go tristate. The DO pin will always go to the tristate condition when CS is low.
3. Opcodes are either 2-bits or 4-bits long depending on the instruction type and are always preceded by a "start-bit" of a logic one. Any number of leading zeros can be clocked in before the start-bit (the sample assembly code inserts seven). Addresses are either 6 or 8-bits long depending on the density of the device. The combined opcode and address field is 8-bits for the smaller devices (93C06 and 93C46) and 10-bits for the larger devices (93C56 and 93C66). On the opcode types that do not use addresses, all of the "dummy" address bits must be clocked anyway (the combined opcode/address field is constant number of clock cycles).
4. On read operations the data out stream starts with a dummy zero. On NM93Cxx family EEPROMs, it is acceptable but not required to have extra clocks after the 16th actual data bit. On NM93CSxx family EEPROMs, extra clocks after the 16th actual data bit will begin to read the next data word.

Notes on the Assembly Code:

The subroutines that follow are adequate to quickly pilot the programmers task of addressing a serial EEPROM of the NM93Cxx family. Additional subroutines can very easily be adapted from these to handle the additional opcode types of the NM93CSxx series parts. Enough code has been included to allow the code to operate in a stand-alone fashion. However, when integrating the routines in to another program, initialization statements affecting global variables such as initializing the stack point or the X or B registers will need to be moved, deleted or replaced by statements in the main program.

The assembly code uses a software timer loop to time out the write time of the EEPROM. The programmer should be aware that it is possible to use the EEPROMs own internal timer to accomplish this task. This is done by monitoring the EEPROMs DO line after taking the EEPROMs CS line low to start a write and then setting CS high again to re-enable the DO output. The write is complete when the DO (of the EEPROM) drives high. Using the EEPROMs internal timer will allows the microcontroller time to accomplish some other task in the 10 ms that the write or erase operation requires. If the DO line is to be used to indicate that the write is complete, other MICROWIRE components on the bus must wait for the EEPROM writes to time out before being accessed (the DO line is in use).

The code was tested on a COP820 device via a Metalink In Circuit Emulator. The code should translate to other COP800 devices with little or no modification.

NM93C06 and NM93C46 Opcodes and Address Fields*

WREN	Write Enable	0	0	1	1	X	X	X	X
WRDI	Write Disable	0	0	0	0	X	X	X	X
ERAL	Erase All	0	0	1	0	X	X	X	X
WRAL	Write All	0	0	0	1	X	X	X	X
READ	Read	1	0	A5	A4	A3	A2	A1	A0
WRITE	Write	0	1	A5	A4	A3	A2	A1	A0

NM93C56 and NM93C66 Opcodes and Address Fields*

WREN	Write Enable	0	0	1	1	X	X	X	X	X	X
WRDI	Write Disable	0	0	0	0	X	X	X	X	X	X
ERAL	Erase All	0	0	1	0	X	X	X	X	X	X
WRAL	Write All	0	0	0	1	X	X	X	X	X	X
READ	Read	1	0	A7	A6	A5	A4	A3	A2	A1	A0
WRITE	Write	0	1	A7	A6	A5	A4	A3	A2	A1	A0

*Note: All Opcode/Address Fields must be preceded with a leading "1" as a start-bit.

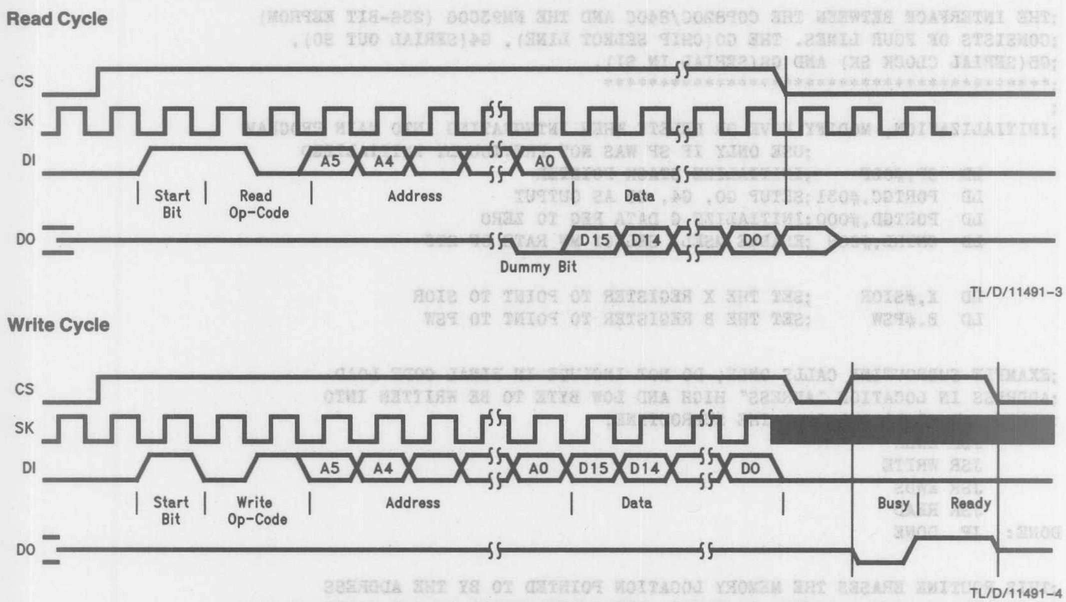


FIGURE 3. Read and Write cycle waveforms. Notice that one leading zero is shown before the start-bit. The actual code inserts seven.

```
;*******************************************************
; THIS PROGRAM PROVIDES SUBROUTINES TO HANDLE COP820 OPERATIONS ON
; THE NM93C06 EEPROM I.E., WRITES, READS, ERASES, ENABLES AND DISABLES
;*******************************************************
;
 .INCLD COP820.INC
;Reserving RAM locations for key variables
 RDATL = 1   ;LOWER BYTE OF THE NM93C06 MEMORY DATA READ
 RDATH = 2   ;UPPER BYTE OF THE NM93C06 MEMORY DATA READ
 WDATL = 3   ;LOWER BYTE OF THE DATA TO BE WRITTEN TO NM93C06
 WDATH = 4   ;UPPER BYTE OF THE DATA TO BE WRITTEN TO NM93C06
 ADRESS = 5  ;THE LOWER 4-BITS OF THIS LOCATION CONTAINS THE ADDRESS
             ;OF THE NM93C06 MEMORY LOCATIONS TO BE READ/WRITTEN
             ;THE UPPER NIBBLE MUST BE ZEROS
 SNDBUF = 0  ;USED FOR THE COMMAND BYTE TO BE WRITTEN (Local Scratch Pad)
 DLYH = 0F0  ;LOCATIONS RESERVED FOR WRITE TIMEOUT VALUES
 DLYL = 0F1
 FLAGS = 6   ;USED FOR PROGRAM FLAGS (Local Scratch Pad)
             ;
             ;FLAG VALUE DEFINITIONS
             ;00        ERASE, ENABLE, DISABLE, ERASE ALL
             ;01        READ CONTENTS OF NM93C06 REGISTER
             ;03        WRITE TO NM93C06 REGISTER
             ;OTHERS    ILLEGAL COMBINATION
```

4

```
;THE INTERFACE BETWEEN THE COP820C/840C AND THE NM93C06 (256-BIT EEPROM)
;CONSISTS OF FOUR LINES. THE G0(CHIP SELECT LINE), G4(SERIAL OUT SO),
;G5(SERIAL CLOCK SK) AND G6(SERIAL IN SI).
;****************************************
;
;INITIALIZATION, MODIFY MOVE OR DELETE WHEN INTEGRATING INTO MAIN PROGRAM
                        ;USE ONLY IF SP WAS NOT PREVIOUSLY INITIALIZED
       LD  SP,#02F      ;INITIALIZE STACK POINTER
       LD  PORTGC,#031;SETUP G0, G4, G5 AS OUTPUT
       LD  PORTGD,#000;INITIALIZE G DATA REG TO ZERO
       LD  CNTRL,#008  ;ENABLE MSEL, SELECT MW RATE OF 2TC

       LD  X,#SIOR     ;SET THE X REGISTER TO POINT TO SIOR
       LD  B,#PSW      ;SET THE B REGISTER TO POINT TO PSW

;EXAMPLE SUBROUTINE CALLS ONLY, DO NOT INCLUDE IN FINAL CODE LOAD
;ADDRESS IN LOCATION "ADRESS" HIGH AND LOW BYTE TO BE WRITTEN INTO
;WDATH AND WDATL AND CALL THE SUBROUTINE,
       JSR EWEN
       JSR WRITE
       JSR EWDS
       JSR READ
DONE:  JP  DONE

;THIS ROUTINE ERASES THE MEMORY LOCATION POINTED TO BY THE ADDRESS
;CONTAINED IN THE LOCATION "ADRESS". THE LOWER NIBBLE OF THE VALUE
;IN THE LOCATION "ADRESS" IS THE NM93C06 REGISTER ADDRESS. THE UPPER
;NIBBLE SHOULD BE SET TO ZERO.
;

ERASE: LD  A,ADRESS
       OR  A,#0C0
       X   A,SNDBUF
       LD  FLAGS,#00
       JSR INIT
       RET
;
;THIS ROUTINE ENABLES PROGRAMMING THE NM93C06 (EWEN).
;
EWEN:  LD  SNDBUF,#030
       LD  FLAGS,#00
       JSR INIT
       RET
;
;THIS ROUTINE DISABLES PROGRAMMING OF NM93C06.
;
EWDS:  LD  SNDBUF,#00
       LD  FLAGS,#00
       JSR INIT
       RET
;
;THIS ROUTINE ERASES ALL REGISTERS OF NM93C06.
;
ERAL:  LD  SNDBUF,#020
       LD  FLAGS,#00
       JSR INIT
       RET
```

```
;
;THIS ROUTINE READS THE CONTENTS OF THE NM93C06 REGISTER. THE ADDRESS
;IS SPECIFIED IN THE LOWER NIBBLE OF LOCATION "ADRESS". THE UPPER
;NIBBLE SHOULD BE SET TO ZERO. THE 16-BIT CONTENTS OF NM93C06 REGISTER ARE
;STORED IN RDATL AND RDATH.
;
READ:  LD     A,ADRESS
       OR     A,#080
       X      A,SNDBUF
       LD     FLAGS,#01
       JSR    INIT
       RET
;
;THIS WRITES A 16-BIT VALUE STORED IN WDATL AND WDADTH TO THE EEPROM
;REGISTER WHOSE ADDRESS IS CONTAINED IN THE LOWER NIBBLE OF THE
;LOCATION "ADRESS". THE UPPER NIBBLE OF THE ADDRESS SHOULD BE SET TO ZERO.
;
WRITE: LD     A,ADRESS
       OR     A,#040
       X      A,SNDBUF
       LD     FLAGS,#03
       JSR    INIT
       RET
;
;THIS ROUTINE SENDS OUT THE START BIT AND COMMAND BYTE. IT ALSO
;DECIPHERS THE CONTENTS OF THE FLAG LOCATION AND MAKES A DECISION
;REGARDING WRITE, READ OR RETURN TO THE CALLING ROUTINE.
;
INIT:  SBIT   0,PORTGD     ;SET CHIP SELECT HIGH
       LD     SIOR,#001    ;LOAD SIOR WITH START BIT
       SBIT   BUSY,[B]     ;SEND OUT THE START BIT
PUNT1: IFBIT  BUSY,[B]
       JP     PUNT1
       LD     A,SNDBUF
       X      A,[X]        ;LOAD SIOR WITH COMMAND BYTE
       SBIT   BUSY,[B]     ;SEND OUT COMMAND BYTE
PUNT2: IFBIT  BUSY,[B]
       JP     PUNT2
       IFBIT  0,FLAGS      ;ANY FURTHER PROCESSING?
       JP     NOTDON       ;YES
       RBIT   0,PORTGD     ;NO, RESET CS AND RETURN
       RET
;
NOTDON:IFBIT  1,FLAGS      ;READ OR WRITE?
       JP     WR93C        ;JMP TO WRITE ROUTINE
       LD     SIOR,#000    ;NO READ NM93C06
       SBIT   BUSY,PSW     ;DUMMY CLOCK TO READ ZERO
       RBIT   BUSY,[B]
       SBIT   BUSY,[B]
PUNT3: IFBIT  BUSY,[B]
       JP     PUNT3
       X      A,[X]
       SBIT   BUSY,[B]
       X      A,RDATH
```

4

```
PUNT4: IFBIT BUSY,[B]
       JP    PUNT4
       LD    A,[X]
       X     A,RDATL
       RBIT  0,PORTGD
       RET
WR93C: LD    A,WDATH
       X     A,[X]
       SBIT  BUSY,[B]
PUNT5: IFBIT BUSY,[B]
       JP    PUNT5
       LD    A,WDATL
       X     A,[X]
       SBIT  BUSY,[B]
PUNT6: IFBIT BUSY,[B]
       JP    PUNT6
       RBIT  0,PORTGD
       JSR   TOUT
       RET
;
;ROUTINE TO GENERATE DELAY FOR WRITE
;****************************************
;
TOUT:  LD    DLYH,#007     ;CHECK YOUR OSCILLATOR--PROCESSOR COMBINATION
                           ;TUNE FOR 10 MS DELAY
WAIT:  LD    DLYL,#0FF
WAIT1: DRSZ  DLYL
       JP    WAIT1
       DRSZ  DLYH
       JP    WAIT
       RET
       .END
```

Designing with the NM93C06 A Versatile Simple to Use E2 PROM

National Semiconductor
Application Note 338
Masood Alavi

This application note outlines various methods of interfacing an NM93C06 with the COPS™ family of microcontrollers and other microprocessors. *Figures 1–6* show pin connections involved in such interfaces. *Figure 7* shows how parallel data can be converted into a serial format to be inputted to the NM93C06; as well as how serial data outputted from an NM93C06 can be converted to a parallel-format.

The second part of the application note summarizes the key points covering the critical electrical specifications to be kept in mind when using the NM93C06.

The third part of the application note shows a list of various applications that can use a NM93C06.

GENERIC CONSIDERATIONS

A typical application should meet the following generic criteria:

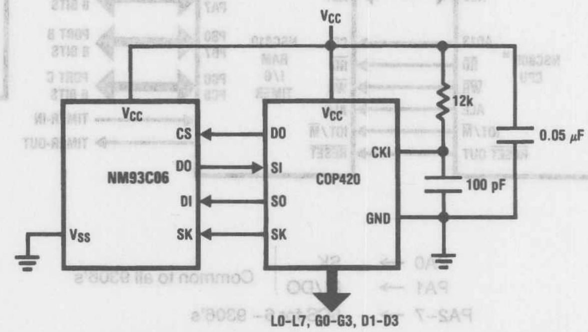
1. Allow for no more than 10,000 E/W cycles for optimum and reliable performance.
2. Allow for any number of read cycles.
3. Allow for an erase or write cycle that operates in the 10–30 ms range, and not in the tens or hundreds of ns range as used in writing RAMs. (Read vs write speeds are distinctly different by orders of magnitude in E2PROM, not so in RAMs.)
4. No battery back-up required for data-retention, which is fully non-volatile for at least 10 years at room-ambient.

SYSTEM CONSIDERATIONS

When the control processor is turned on and off, power supply transitions between ground and operating voltage may cause undesired pulses to occur on data, address and control lines. By using WEEN and WEDS instructions in conjunction with a LO-HI transition on CS, accidental erasing or writing into the memory is prevented.

The duty cycle in conjunction with the maximum frequency translates into having a minimum Hi-time on the SK clock. If the minimum SK clock high time is greater than 1 μs, the duty cycle is not a critical factor as long as the frequency does not exceed the 250 kHz max. On the low side no limit exists on the minimum frequency. This makes it superior to the COP499 CMOS-RAM. The rise and fall times on the SK clock can also be slow enough not to require termination up to reasonable cable-lengths.

Since the device operates off of a simple 5V supply, the signal levels on the inputs are non-critical and may be operated anywhere within the specified input range.



TL/D/5286-1

FIGURE 1. NM93C06—COP420 Interface

4

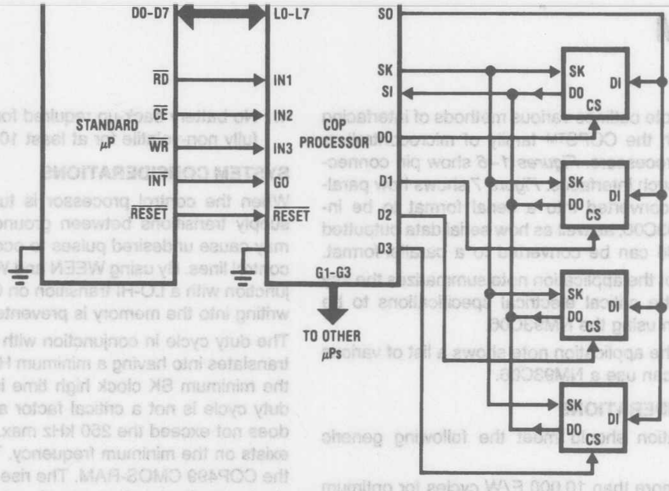
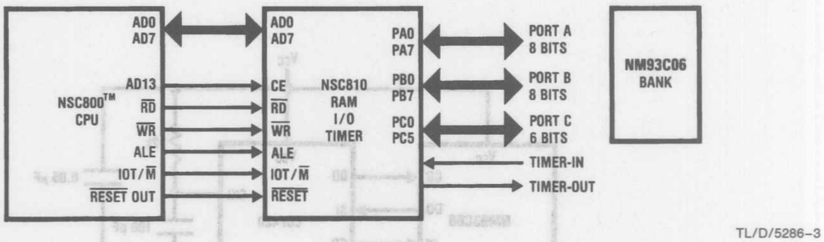


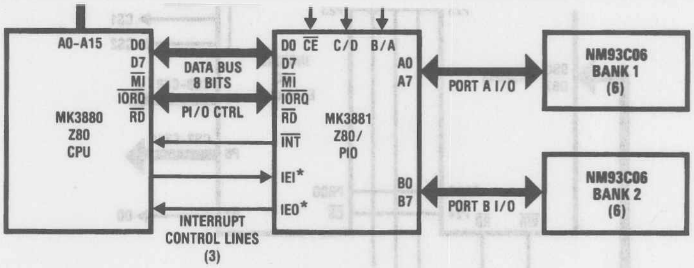
FIGURE 2. NM93CO6—Standard μP Interface Via COP Processor



PA0 → SK
PA1 → DI/DO
Common to all 9306's
PA2-7 → 6CS for 6- 9306's

* **SK is generated on port pins by bit-set and bit-clear operations in software. A symmetrical duty cycle is not critical.**
* **CS is set in software. To generate 10–30 ms write/erase the timer/counter is used. During write/erase. SK may be turned off.**

FIGURE 3. NSC800™ to NM93C06 Interface (also Valid for 8085/8085A and 8156)



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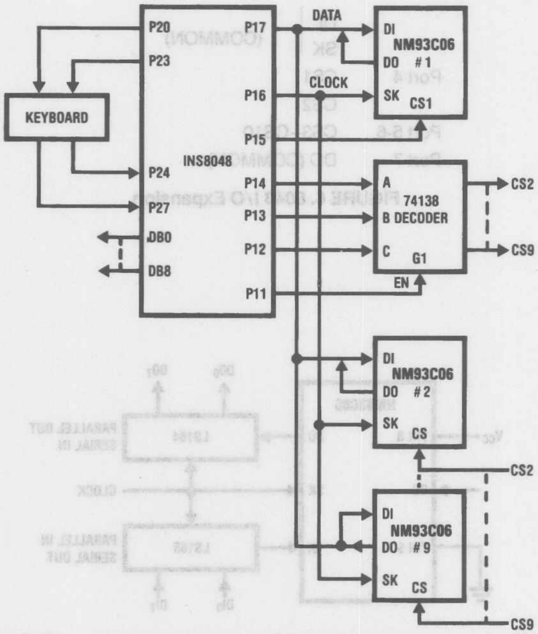
Z80-P10	9306	
A0	SK	Common to all 9306's (Bank 1)
A1	DI/DO	
A2-A7	CS1-CS6	

* Only used if priority interrupt daisy chain is desired
* Identical connection for Port B

FIGURE 4. Z80—NM93C06 Interface Using Z80-PIO Chip



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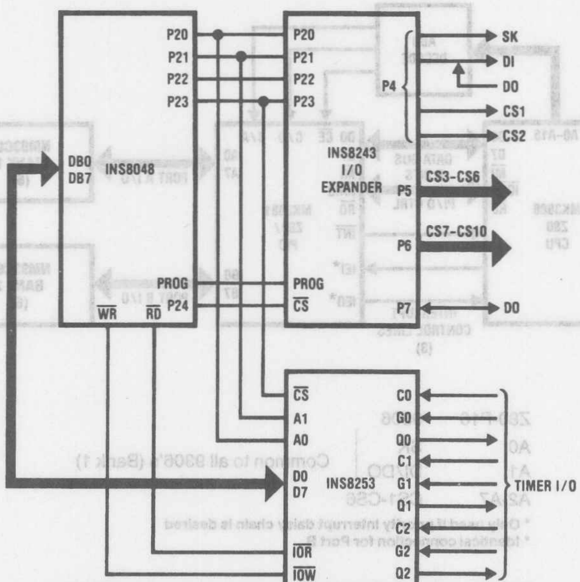
* SK and DI are generated by software. It should be noted that at 2.72 μs/instruction. The minimum SK period achievable will be 10.88 μs or 92 kHz, well within the NM93C06 frequency range.

* DO may be brought out on a separate port pin if desired.

FIGURE 5. 48 Series μP—NM93C06 Interface

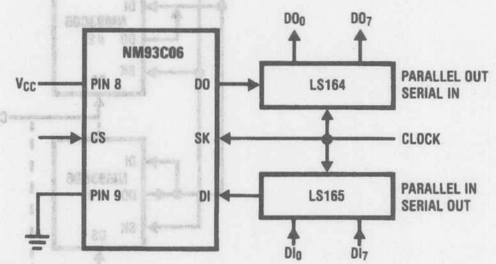


TL/D/5286-6

Expander outputs

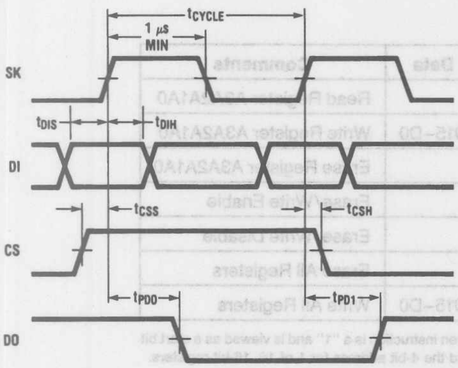
	DI	(COMMON)
	SK	
Port 4	CS1	
	CS2	
Port 5-6	CS3–CS10	
Port 7	DO (COMMON)	

FIGURE 6. 8048 I/O Expansion



TL/D/5286-7

FIGURE 7. Converting Parallel Data into Serial Input for NM93C06



	Min	Max
t_{CYCLE}	0	250 kHz
t_{DIS}	400	ns
t_{D1H}	400	ns
t_{CSS}	200	ns
t_{CSH}	0	ns
t_{PD0}		2 µs
t_{PD1}		2 µs

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FIGURE 8. NM93C06 Timing

THE NM93C06A

Extremely simple to interface with any µP or hardware logic. The device has six pins for the following functions:

Pin 1	CS*	HI enabled
Pin 2	SK	Serial Clock input
Pin 3	DI	For instruction or data input
Pin 4	DO**	For data read, TRI-STATE® otherwise
Pin 5	GND	
Pin 8	V_{CC}	For 5V power
Pins 6–7	No Connect	No termination required

*Following an E/W instruction feed, CS is also toggled low for 10 ms (typical) for an E/W operation. This internally turns the VPP generator on (HI-LO on CS) and off (LO-HI on CS).

**DI and DO can be on a common line since DO is TRI-STATED when unselected DO is only on in the read mode.

USING THE NM93C06

The following points are worth noting:

1. SK clock frequency should be in the 0–250 kHz range. With most µPs this is easily achieved when implemented in software by bit-set and bit-clear instructions, which take 4 instructions to execute a clock or a frequency in the 100 kHz range for standard µP speeds. Symmetrical duty cycle is irrelevant if SK HI time is ≥ 2 µs.
2. CS low period following an E/W instruction must not exceed the 30 ms max. It should best be set at typical or minimum spec of 10 ms. This is easily done by timer or a software connect. The reason is that it minimizes the 'on time' for the high V_{PP} internal voltage, and so maximizes endurance. SK-clock during this period may be turned off if desired.
3. All E/W instructions must be preceded by EWEN and should be followed by an EWDS. This is to secure the stored data and avoid inadvertent erase or write.
4. A continuously 'on' SK clock does not hurt the stored data. Proper sequencing of instructions and data on DI is essential to proper operation.
5. Stored data is fully non-volatile for a minimum of ten years independent of V_{CC}, which may be on or off. Read cycles have no adverse effects on data retention.
6. Up to 10,000 E/W cycles/register are possible. Under typical conditions, this number may actually approach 1 million. For applications requiring a large number of cycles, redundant use of internal registers beyond 10,000 cycles is recommended.
7. Data shows a fairly constant E/W Programming behavior over temperature. In this sense E^2PROMs supersede EPROMs which are restricted to room temperature programming.
8. As shown in the timing diagrams, the start bit on DI must be set by a ZERO - ONE transition following a CS enable (ZERO - ONE), when executing any instruction. ONE CS enable transition can only execute ONE instruction.
9. In the read mode, following an instruction and data train, the DI can be a don't care, while the data is being outputted i.e., for next 17 bits or clocks. The same is true for other instructions after the instruction and data has been fed in.
10. The data-out train starts with a dummy bit 0 and is terminated by chip deselect. Any extra SK cycle after 16 bits is not essential. If CS is held on after all 16 of the data bits have been outputted, the DO will output the state of DI till another CS LO-HI transition starts a new instruction cycle.
11. When a common line is used for DI and DO, a probable overlap occurs between the last bit on DI and start bit on DO.
12. After a read cycle, the CS must be brought low for 1 SK clock cycle before another instruction cycle can start.

All commands, data in, and data out are shifted in/out on rising edge of SK clock.

Write/erase is then done by pulsing CS low for 10 ms.

All instructions are initiated by a LO-HI transition on CS followed by a LO-HI transition on DI.

READ — After read command is shifted in DI becomes don't care and data can be read out on data out, starting with dummy bit zero.

WRITE — Write command shifted in followed by data in (16 bits) then CS pulsed low for 10 ms minimum.

INSTRUCTION SET

Instruction	SB	Opcode	Address	Data	Comments
READ	01	10xx	A3A2A1A0		Read Register A3A2A1A0
WRITE	01	01xx	A3A2A1A0	D15–D0	Write Register A3A2A1A0
ERASE	01	11xx	A3A2A1A0		Erase Register A3A2A1A0
EWEN	01	0011	XXXX		Erase/Write Enable
EWDS	01	0000	XXXX		Erase/Write Disable
ERAL	01	0010	XXXX		Erase All Registers
WRAL	01	0001	XXXX	D15–D0	Write All Registers

NM93C06 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

The following is a list of various systems that could use a NM93C06

A. Airline terminal
Alarm system
Analog switch network
Auto calibration system
Automobile odometer
Auto engine control
Avionics fire control

B. Bathroom scale
Blood analyzer
Bus interface

C. Cable T.V. tuner
CAD graphics
Calibration device
Calculator—user programmable
Camera system
Code identifier
Communications controller
Computer terminal
Control panel
Crystal oscillator

D. Data acquisition system
Data terminal

E. Electronic circuit breaker
Electronic DIP switch
Electronic potentiometer
Emissions analyzer
Encryption system
Energy management system

F. Flow computer
Frequency synthesizer
Fuel computer

G. Gas analyzer
Gasoline pump

H. Home energy management
Hotel lock

I. Industrial control
Instrumentation

J. Joulemeter

K. Keyboard -softkey

L. Laser machine tool

M. Machine control
Machine process control
Medical imaging
Memory bank selection
Message center control
Mobile telephone
Modem
Motion picture projector

N. Navigation receiver
Network system
Number comparison

O. Oilfield equipment

P. PABX
Patient monitoring
Plasma display driver
Postal scale
Process control
Programmable communications
Protocol converter

Q. Quiescent current meter

R. Radio tuner
Radar dectector
Refinery controller
Repeater
Repertory dialer

S. Secure communications system
Self diagnostic test equipment
Sona-Bouy
Spectral scanner
Spectrum analyzer

T. Telecommunications switching system
Teleconferencing system
Telephone dialing system
T.V. tuner
Terminal
Test equipment
Test system
TouchTone dialers
Traffic signal controller

U. Ultrasound diagnostics
Utility telemetering

V. Video games
Video tape system
Voice/data phone switch

W. Winchester disk controller

X. X-ray machine
Xenon lamp system

Y. YAG—laser controller

Z. Zone/perimeter alarm system

Using the NM93CS EEPROM Family Features

National Semiconductor
Application Note 716
Paul Lubeck

The NM93CS Family consists of four members as shown in Table I. Each of these members is available in a variety of temperature ranges, operating voltage ranges, and packaging options. These EEPROMs are a superset of the industry standard NM93C Family. The differentiating features of the NM93CS Family are the Sequential Register Read and the Memory Protect Register. The purpose of this application note is to more fully describe these features.

TABLE I. NM93CS Family Members

Part Number	Memory Size	Internal Organization
NM93CS06	256-bit	16 x 16
NM93CS46	1024-bit	64 x 16
NM93CS56	2048-bit	128 x 16
NM93CS66	4096-bit	256 x 16

SEQUENTIAL REGISTER READ

This read mode is entered the same way as the standard word read. First a start bit is transmitted, followed by the op code for a read cycle and then the first address to be read. It is always necessary to define the first address to be read since the address register's state is not guaranteed.

Up until this point, the data out (DO) will remain in TRI-STATE®, but beginning with the same rising edge of the clock (SK) that clocks in address bit A0, the data out will drive a low level. This first bit is always a zero. Starting with the next clock, valid data will appear on the data out pin. The leading zero in the data field will only appear in the first word read in a sequential read sequence, all subsequent data words will be clocked out on the data out pin in an uninterrupted stream. Refer to Figure 1 for the timing sequence.

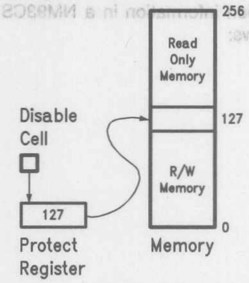
Any number of data words may be read with a single sequential read instruction. When the top of memory is reached it will automatically wrap around to address 0 and continue in the sequential read mode. Using this feature it would be possible to read the entire memory in an endless loop if desired.

The Memory Protect Register has no effect on Sequential Read. The Sequential Read will cross the write protection boundary and read to the top of the memory and cycle back to address 0 (possibly in the unprotected field) regardless of the Protect Register status.

To terminate a sequential read operation, the host must drop chip select (low). At any time CS is transitioned to a low, the current instruction will be terminated. It is not necessary to observe word boundaries when terminating a read or sequential read operation. It may be terminated at any time without affect on the EEPROM.

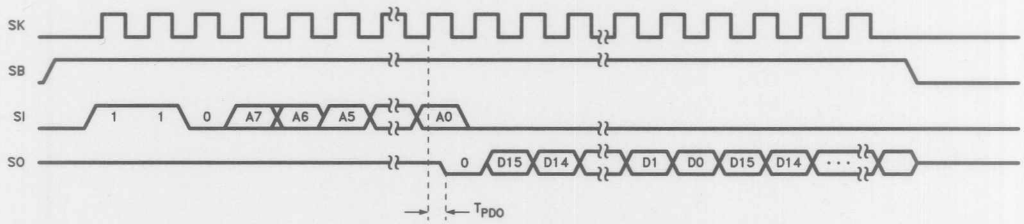
MEMORY PROTECT REGISTER

The protect register is a unique method of write protecting the contents of a variable number of memory registers. The basic concept is shown in Figure 2 using the NM93CS66 4096-bit EEPROM. For the other family members everything remains the same except the memory size and the corresponding maximum address that can be set in the protect register. One other difference that needs to be noted is the address length for the NM93CS06 and NM93CS46 is 6 bits and for the NM93CS56 and NM93CS66, 8 bits. The difference in address length produces a corresponding difference in length of the protect register.



TL/D/11056–2

FIGURE 2. Memory Protect Register



TL/D/11056–1

FIGURE 1. Sequential Read Instruction Sequence

There are two basic elements to the protection scheme, the Protect Register and the Disable Cell. Both the Protect Register and the Disable Cell are implemented in EEPROM latches, therefore do not require the introduction of additional technologies onto the die. The purpose of the Protect Register is to contain the address of the first write protected location in memory. The location in memory defined by the address written into the protect register and all others above that location, to the maximum address in memory are write protected.

The Protect Register is writable from the serial bus in a manner similar to writing a memory register, the only difference being the input PRE (Protect Register Enable) must be high and the instruction immediately preceding the write to the protect register must be a Protect Register Enable (PREN) instruction. By requiring this specific sequence and set of conditions, both hardware and software oriented, the chances of inadvertently changing the contents of the protect register or an unauthorized user changing the data without specific knowledge of the operation of the EEPROM are very remote.

The Disable Cell is a single EEPROM latch that may be set via a Protect Register Disable (PRDS) instruction. Like the Protect Register Write (PRWRITE) instruction, it must be executed with the input PRE high and immediately preceded by a PREN instruction. Once the Disable Cell is written, it cannot be cleared because the PRDS instruction is a one time only instruction. Once the PRDS instruction has been executed, the Protect Register cannot be updated again in the life of the part and the defined portion of memory is permanently protected.

A typical instruction sequence for storing manufacturing and factory calibration information in a NM93CS family part is shown as follows:

Instruction	Description
1.	Power On
2. WEN	Enable all programming instructions.
3. WRITE A(max)	Write maximum address location.
4. WRITE A(max-1)	Write maximum address location -1.
5. WRITE A(max-2)	Write max. address location -2.
:	:
:	:
6. WRITE A(max-y)	Write maximum address location -y.
7. PREN	Enable programming of Protect Register.
8. PRWRITE (A(max-y))	Write address (max-y) to Protect Register.
9. PREN	Enable programming of the Disable Cell.
10. PRDS	Disable all future programming of the protect register and protected memory.
11. WDS	Disable all programming instructions.

It is not necessary to do steps 9 and 10. The PRDS instruction makes the protection permanent. Without executing the PRDS instruction the option remains to remove the write protection thus allowing changing the data in the formerly protected portion of memory. The following sequence will remove the write protection and clear the contents of the Protect Register:

Instruction	Description
1. WEN	Enable all programming instruction.
2. PREN	Enable programming of the Protect Register.
3. PRCLEAR	Enable writing of all memory locations and clear the Protect Register.
4. WDS	Disable all programming instruction.

In both examples above the final step is a Write Disable (WDS) instruction. This instruction would normally be delayed until all programming is complete, but should be included as a minimal level of data protection for otherwise unprotected memory locations.

Upgrade to National's Wide Voltage Range, Zero Standby Current EEPROMs

National Semiconductor
Application Note 870
Robert Stodieck

ABSTRACT

National's NM93C06L, NM93C46L, and NM93C56L EEPROMs and the new NM93C06/46/56LZ series devices operate across a 2.0V to 5.5V range suitable for unregulated battery powered operation. In addition, the new NM93C06/46/56LZ devices have ultra-low standby currents ideal for portable applications using very small batteries.

PERSONAL ELECTRONICS GAIN SOPHISTICATION

Many personal electronic items have moved from being perceived as trendy novelties to being viewed as mainstream personal or business appliances. Consumer familiarity, in turn, produces sophistication in the market for features. The ability to retain memory through battery changes and other types of power failure is highly desirable. Implementation of such sophisticated features requires RAM with battery back up or EEPROM memory.

Battery backed up RAM is usually far more expensive and functionally less attractive than EEPROM memory. Battery backed up RAM requires:

1. RAM
2. Battery holder
3. Battery
4. A door or other method to allow the battery to be replaced
5. New batteries to be located and replaced by the owner

EEPROM on the other hand requires:

1. EEPROM.

Serial EEPROM is invariably the cheapest and most compact solution for memory requirements up to 16 kbits.

CORDLESS PHONES

Memory dialing, noise reduction signal processing, and multi-channel operation with low noise channel selection capability, are now standard features for better quality cordless phones. Cordless phones are now moving to serial EEPROMs which can retain memory dial phone numbers and other parameters even through the inevitable dead battery and line power outage events.

Cordless phones have limited battery life. Memory dial data and other feature settings stored in RAM are subject to loss from dead batteries if implemented in the hand unit, or line power outages if maintained in the base unit. Reprogramming ten or more numbers for a memory dialer each time this happens is not desirable. Implementation of memory dialing and other features in the environment of a cordless phone requires RAM with a battery back up or EEPROM memory.

The length of time a phone can be left off its charger when not in use without the battery going dead is called standby. The cordless phone in standby normally leaves the radio receiver on to listen for incoming calls so that it can ring locally.

Standby and off hook time power consumption are dominated by the linear circuitry of the radio transmitter and receiver. Furthermore, the batteries in this application are relatively large and are frequently recharged. Thus, this application does not usually require the extremely low standby currents that can be achieved with the "LZ" series serial EEPROMs. But a broad range of V_{CC} voltages are encountered in this application. Most cordless phones use a stack of three Ni-Cad batteries for power. This produces a nominal voltage of 3.6V, but during charging this may go as high as 4.0V, and may drop into the 2.7V range in use. Some types of cordless phones use other battery technologies and battery counts. For example, stacks of 2 lead acid cells are also used producing a 4V nominal V_{CC}. The 2.0V to 5.5V V_{CC} range allowed by the "L" series of serial EEPROMs accommodates all the common V_{CC} ranges.

PAGERS

Paging units are a second example of high technology electronics gone blasé. Unlike cordless phones, pagers use regulated batteries for power and thus, do not need wide V_{CC} range EEPROMs. Since the batteries are small and power is a concern, low voltage operation is an advantage, as are very low standby currents used by the "LZ" series.

ELECTRONIC CAMERAS

All electronic cameras also make use of the NM93C46LZ and NM93C56LZ devices. This application generally uses regulated batteries to guarantee a constant 5V. But the batteries tend to be small and the camera spends much of its life on the shelf. Parameters stored in the electronic memory on these new cameras include shutter speed and focus calibrations that must never be lost in the life of the camera, and the frame counts and other details that change in service but which must not be lost when the battery dies.

The parameters connected with the many features found on these cameras are best retained in EEPROM. The small batteries and the long periods of inactivity involved require an EEPROM with very low standby currents to avoid running down the battery when not in use. With a standby current of less than 1 μA, the "LZ" series parts handle these applications with ease.

LEARNING REMOTE CONTROL UNITS

Alas, you have taught your new remote control unit to control the volume on your TV, it has mastered the slow advance on the video cassette recorder, it turns on and off the CD player, and your local soap opera is recorded daily

thanks to VCR Plus™ function. If the designer hasn't stored the critical information required in an EEPROM, one had better hope the battery never dies, or one will again become a slave to his "personal assistant" while retraining the beast. Owners of many first generation VCRs and televisions with digital random access tuners know the feeling well. Random access tuners allow their owners to skip over all the channels that could not be accessed in the area or that the owner simply did not like. But, if the power cord was even briefly disturbed or if the power went down, the tuner had to be retrained, a time consuming operation.

Both learning remote controls and digital tuners are more likely now to cure these problems by using EEPROM. TV and VCRs do not need low voltage, wide V_{CC} range, or low standby current parts, but the remote control units frequently do. The scenario is familiar:

1. Unregulated batteries are used.
2. The batteries are not large or frequently recharged.
3. The units spend relatively little time actually in use.
4. Long battery life is desirable.

Smart remote controls benefit from the wide V_{CC} range and low standby characteristics of the NM93C46LZ and NM93C56LZ serial EEPROMs.

SUMMARY

Serial EEPROMs offer by far the most compact and low cost non-volatile memory solutions for common consumer applications. The need for serial EEPROMs continues to grow with increasing consumer sophistication and growth of the personal electronics market. National's LZ products have wide operating voltage ranges and very low standby power and are particularly appropriate for battery powered applications of all types.

EEPROMs to High Volume OEMs

ABSTRACT

National's 93CSxx family of serial EEPROMs offer sophisticated protection against accidental overwrite. Unfortunately, understanding why and when this protection is needed often requires an equally sophisticated design engineer. This application note sheds light on the causes of accidental overwrite and the solutions that the "CS" series provide for controlling the problem.

GETTING SOPHISTICATED

EEPROMs are an important refinement to digital electronic products of many types. As consumers become more sophisticated about features, the advantages of non-volatile and cost effective serial EEPROMs frequently become important. Digital systems from cordless phones to VCRs, and from keyless entry systems to thermostats, benefit from the ability to store small stashes of data that do not go away when the power goes down or the batteries die.

The designers first reflex is to grab the cheapest generic solution on the market and run with it. After all, serial EEPROMs are all really the same aren't they?

NO!

In the beginning National Semiconductor married its MICROWIRE™ serial bus to a small EEPROM and created a classic 8-pin device that has since been copied by dozens of makers and has become the industry standard. Its descendants are available now from National in densities from 256 bits to 16 kbits.

So buy the industry standard device (every one else does) and run with it right?

NO!

National Semiconductor's classic 8-pin device is clearly the correct choice for some, but not all systems, and not knowing the difference can be expensive. Designs that shine through prototyping and test may fail in the field.

Serial EEPROMs are connected to microprocessors, microcontrollers and ASICs. Under a variety of error conditions the controlling system can accidentally overwrite data in the EEPROM. Application environments vary widely as does the importance of the data the EEPROMs are used to retain. The bit of information retained in the non-volatile memory may control the shape of the graphic sprite used in a child's game or something of importance to a nuclear power plant. It is be to expected that there is a need for more than one type of EEPROM.

The economy of serial EEPROMs and their utility explains why they are often used in high volume consumer items. Quality here is paramount because a flaw in the design can lead to very expensive returns and even recalls.

WHAT'S THE PROBLEM?

Volatile DRAM and SRAM memory forget past mistakes on reset or power down. A malfunctioning computer or video game can usually be fixed by turning the unit off and back on again. In contrast, non-volatile memories retain data even after the power goes off. They also retain memory of past single event mistakes such as unintended write operations.

Accidental overwrites to EEPROM can be caused by power supply noise, electrical interface noise, errant software, or "crashing" microcontrollers and processors. Such an event may be rare indeed but needs to occur ONLY ONCE in a product's lifetime to cause a problem and . . . such events are not always so rare.

Overwrite problems are well understood in the parallel EEPROM world. Overwrite protection schemes have long been central to the parallel EEPROM's architecture. Parallel EEPROMs usually have V_{CC} voltage sensing circuitry that helps to prevent unintended write events on power-up or power-down and V_{CC} transients. In addition, fairly complex write protection algorithms are used to reduce the probability of accidental overwrite.

Serial EEPROMs are far less susceptible to accidental overwrites than are parallel devices. The long sequence of serial data required to trigger a write in a serial device makes many of the precautions used on parallel devices unnecessary. Random noise on power-up is not likely to imitate the 19 plus serial bit sequence required to initiate a write operation.

However, the difficult problem of overwrite protection during a processor "crash" remains. There are some applications where there is no definitive solution to this problem. However, in many other situations the write protect features of the NM93CSxx can limit or cleanly eliminate the problem.

SO WHAT IS THE PROBLEM?

The fact that a long serial bit sequence is required to initiate a write operation into a serial non-volatile memory solves most accidental overwrite problems. But there is one persistent type of failure pathology that remains and can defeat this type of protection. It is particularly likely to occur in applications using small microcontrollers.

The problem is that no matter what input sequence is required to trigger a write operation, it has to be known to and be embedded in the software. The code segment that "knows" the write input sequence can be executed by unplanned jumps in the program sequencing induced by electrical noise, in practice usually V_{CC} noise or low V_{CC}. It can also be caused by imperfect software.

DOES THAT REALLY HAPPEN?

Yes. Understanding the problem requires a little reflection on how a processor works. A program counter is the device that generates addresses for program memory accesses. Remember that the program counter in a processor is basically a re-loadable binary counter. As long as V_{CC} is steady, and the clock and control signals to the control are noise free and within specified timing, the count (and program execution) normally advances one step at a time (see *Figure 1a*).

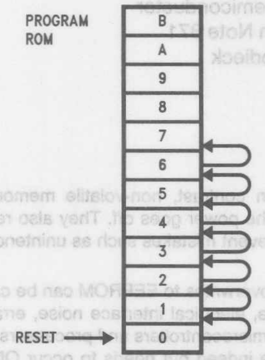


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FIGURE 1a. Normal Program Flow after Power-On Reset

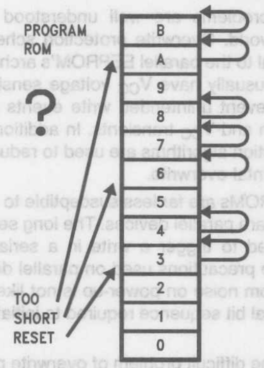

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FIGURE 1b. Disturbed Reset Operation Following a Too Short Reset Pulse. This is a Common Scenario after a Short Interruption of V_{CC}.

If V_{CC} is not steady or is too low, and the clock or control signals are not noise free or are not within specified timings, the count may skip randomly. If V_{CC} or the offending control signals then return to normal, the count (and program execution) again begins to advance one increment at a time. But now the program is at a completely random location. If the program counter has skipped to the program segment that writes to the EEPROM, it will tend to write garbage to random locations. This is a particularly serious problem for microcontrollers which have relatively small program memory spaces. Thus, any skipping that occurs is more likely to overrun the serial write code.

THE SHORT RESET EXAMPLE

Normal processor reset is illustrated in *Figure 1a.* Faulty reset, possibly caused by short V_{CC} interruptions, is illustrated in *Figure 1b.* If the processor starts operation near the "WRITE_EEPROM" code segment it may trigger an accidental overwrite. It is difficult to prevent this type of missequencing in all cases because of the large spectrum of V_{CC} transients that may be experienced in the products lifetime. Some combination of low V_{CC} and V_{CC} interruption timing can usually be found that prevents the power up reset circuit from resetting correctly.

The slowly decaying V_{CC} level resulting from a discharging battery will also cause the program counter to begin skipping at some point. This is a common problem with the myriad of small electronic devices powered by unregulated batteries. Learning remote control units are a practical example of a system that uses EEPROM and suffers from this problem.

In large microprocessors with large memory spaces and various traps to stop errant operation, the possibility of accidental overwrite is not particularly high. But, in microcontrollers that may have only 1 kbyte to 2 kbytes of program code and few trapping techniques, this is a serious problem. Furthermore, in some applications conditions that can trigger this type of problem are repetitive and frequent.

FOR EXAMPLE

Room thermostats and refrigerators have historically used bi-metallic switches to maintain temperature control. If the line power dipped or dropped out there was no problem. Operating temperatures would soon return to normal when the power came back on. These kinds of controls are, of course, frequently being replaced with digital units, but these have a few problems. The temperature setting must be stored in battery backed-up RAM, or it must be stored in EEPROM. If not it will be volatile and lost after a power outage.

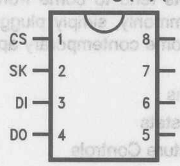
Serial EEPROM is by far the most desirable and cost effective way of providing non-volatility for this type of application, but care must be taken to guarantee data integrity in the EEPROM to prevent a change in temperature settings caused by an accidental overwrite.

Fortunately, the write security features of the NM93CSxx family of EEPROMs can not only guarantee security for the temperature data under the worst conditions, but at the same time has space for temperature calibration data, a serial number, and a date of manufacture, if required. Furthermore, the temperature calibration and serial number data can be rendered absolutely permanent. *Figure 3* shows how the write Protect Register of a NM93CSxx part can be used to protect a zone of memory from writes. This protection can be made permanent, if desired, by executing a one time only instruction that disables all writes to the protect register itself.

The write protect features are controlled by two new pin functions that replace two no connect pins on the standard MICROWIRE pinout *(Figure 3):* the Program Enable pin, PE, and the Protect Register Enable pin, PRE. The PE pin must be high to enable any write to the EEPROM. The PRE pin must be high to write to allow writes to the internal Write Protect Register.

Note: The words write and program are used interchangably.

Dual-In-Line Package (N)
Small Outline Gull Wing (M) (0.050″ C-C)



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Top View

NM93CXX	NM93CSXX
V_{CC}	→
NC	PRE (Protect Register Enable)
NC	PE (Program Enable)
GND	→

FIGURE 2. The NM93CSxx Series Replaces No Connect Pins on the Standard Serial EEPROM Pinout with Two New Pins to Control Write Enable Functions.

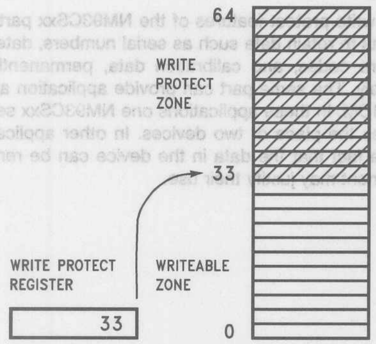

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FIGURE 3. With the Write Protect Register Programmed to 33, EEPROM Locations 33 to the End of Memory are Not Writable.

Figure 4 is a block diagram of a refrigerator controller example. *Figure 5* shows how a factory-only accessible jumper can be used to control the logic level of the Protect Register Enable pin, and a user accessible push button switch can be used to control the logic level of the Program Enable pin.

This arrangement allows the factory to enter and protect temperature calibration data in the EEPROM. The calibration data is located in the area protected by the protect register defined area. This data can only be altered by a trained technician who knows about the jumper.

At the same time, this arrangement allows the user to change the temperature settings which are located in the "writeable" area. Keep in mind though that this area is writeable only when the Program Enable (PE) pin is held high by the "SET" push button. The temperature setting is located in the "unprotected" area, where overwrites are controlled by using the PE pin. This example illustrates the use of two levels of write protection available with the "CS" series EEPROMs.

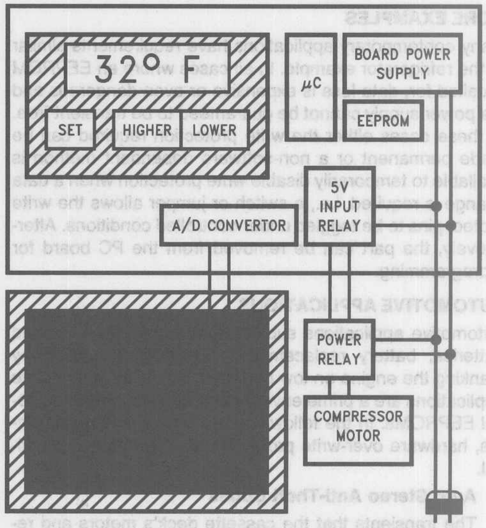

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FIGURE 4. Refrigerator Temperature Controller. The Main Power Relay, Connected Directly to the Same power Line as the Controller, Cycles Off and On Frequently to Maintain Refrigerator Temperature, Creating an Ample Capacity for Generating Short Destructive V_{CC} Transients.

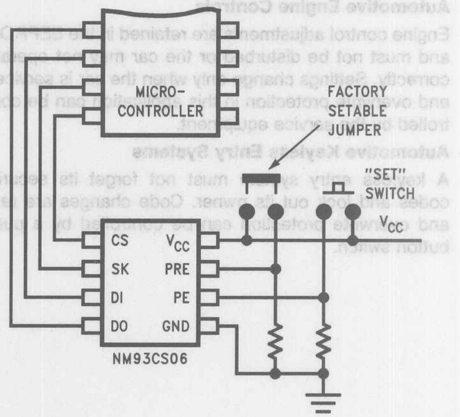

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FIGURE 5. A Combination of a User-Accessible Switch, and a Factory Only Accessible Jumper, Allows Two Different Zones of Over-Write Protection in the Same EEPROM.

Most importantly though, the arrangement of the user accessible switch prevents accidental writes to the EEPROM from any source, and the write protection control is not software dependent. The EEPROM may not be altered in any way except when the user is actually pressing a front panel button labeled SET (*Figures 4* and *5*). This makes the probability of unintended overwrite vanishingly slight.

MORE EXAMPLES

Many contemporary applications have requirements similar to the refrigerator example. In all cases where an EEPROM is called for, data loss is expensive or even dangerous and the power supply cannot be guaranteed to be transient free. In these cases either the write protection required can be made permanent or a non-software dependent method is available to temporarily disable write protection when a data change is required, i.e., a switch or jumper allows the write protect pins to be toggled under controlled conditions. Alternatively, the part can be removed from the PC board for reprogramming.

AUTOMOTIVE APPLICATIONS

Automotive applications subject auto accessories to dead batteries, battery replacements, brown outs caused by cranking the engine on low batteries, etc. Thus, automotive applications are a prime environment for write protected serial EEPROMs. In the following applications and many others, hardware over-write protection is desirable and practical.

— **Auto Stereo Anti-Theft Codes**

The transients that the cassette deck's motors and relays generate in operation contribute to the normal automotive V_{CC} transients that the microcontroller must weather. Unless overwrite protection is provided for the EEPROM, one "crash" event could provoke an unintended overwrite and the deck may fail to work for its correct owner. Code changes are rare and overwrite protection can be controlled by a push button switch.

— **Automotive Engine Controls**

Engine control adjustments are retained in the EEPROM and must not be disturbed or the car may not operate correctly. Settings change only when the car is serviced and overwrite protection in this application can be controlled by the service equipment.

— **Automotive Keyless Entry Systems**

A keyless entry system must not forget its security codes and lock out its owner. Code changes are rare and overwrite protection can be controlled by a push button switch.

HOUSEHOLD APPLICATIONS

Household V_{CC} transients tend to come from brownouts, blackouts, and most commonly, simply plugging in or unplugging an appliance. Some contemporary applications include:

— Keyless Entry Systems

— Digital Room Thermostats

— Refrigerator Temperature Controls

TELECOM SWITCH APPLICATIONS

It is now a requirement that all boards found in common telecom switching systems have an electronically readable serial number. The serial number of any board in a switch must be readable from an operators console. This is an aid to repair. Reliability is a paramount consideration. With the NM93CSxx series serial EEPROMs the serial number can be recorded either permanently or alterably, changeable only by replacing the part in a socket or by a technician fitting a jumper during a rare, factory only, reprogramming event.

IN SUMMARY

The multiple write protect features of the NM93CSxx parts allow the parts to retain data such as serial numbers, date-of-manufacture codes, and calibration data, permanently and unalterably. The same part can provide application alterable EEPROM. In these applications one NM93CSxx series part takes the place of two devices. In other applications, just the fact that the data in the device can be rendered permanent may justify their use.

68HC11 to MICROWIRE™ "Chip Security" EEPROMs

Brian Underwood

ABSTRACT

National's NM93CSxx Family of serial EEPROMs offers sophisticated protection against accidental overwrites from power surges, controller crashes, and other potential noise sources. Utilizing the data protection features in these devices require a few, simple command sequences which may not be familiar to users of standard MICROWIRE™ commands. This application note presents and explains assembly code for Motorola's 68HC11 microcontroller which implements all of the interface command sequences required to control the NM93CSxx Family of EEPROMs.

WHY SHOULD DESIGN ENGINEERS USE NATIONAL SEMICONDUCTOR'S NM93CSxx FAMILY OF EEPROMs?

There has never been a more "data secure" EEPROM available on the market than the NM93CSxx devices. These "Chip Security" EEPROMs enable Design Engineers to bring new products to market quicker than ever before. The Chip Security features prevent the slightest risk of inadvertent writes caused by noise sources, and unplanned jumps in program sequencing that are difficult to "track down." Trial-and-error tactics to determine the cause of accidental overwrites often takes several hours which are not expendable in todays dynamic and fast paced market, so to help prevent data corruption problems that often delay product introduction dates, NM93CSxx devices have software and hardware features that eliminate those potential problems.

Another benefit realized by using the NM93CSxx Family of EEPROMs is preventing field failure returns of the end product. The hardware and software data protection features described in this application note prevent all types of accidental overwrites that could cause a field failure of the end product, such as losing radio stations stored in EEPROM or losing valuable calibration data points that are considered vital to the accuracy of test equipment. As the "Rule of Tens" states, if it cost $10 to find an error at the board level, then it will cost $100 at the system level, and finally $1000 at the field level. Why is the cost incurred exponential in nature? Simple, failures in the field can lose customers and ruin reputations if the product doesn't work.

BACKGROUND INFORMATION ON NATIONAL SEMICONDUCTOR's EEPROMs

National Semiconductor is the market leader in low density serial EEPROMs, and defined the ubiquitous MICROWIRE interface commonly copied by our competitors. We offer standard MICROWIRE EEPROMs from 256 bits up to 16 Kbits (16K available 1st quarter of 1994). And for upscale products that can't afford the slightest risk of data corruption, we invented and brought to market the "Chip Security" MICROWIRE EEPROM Family. With over ten years of EEPROM design and process experience, we have also developed low voltage (1.8V to 6.0V) and Zero Standby (< 1 μA standby current) EEPROMs to meet the battery supported market needs.

BRIEF OVERVIEW OF THE NM93CSxx FEATURES

The "Chip Security" EEPROM Family has data protection features added to the standard MICROWIRE Family that give the ultimate data protection solution in non-volatile, serial memory devices. The assembly code required to read and write the NM93CSxx (Chip Security devices) is the same as that required by the NM93Cxx EEPROMs (standard devices). The difference lays in the added commands and hardwire pins that bring about the data protection.

The first available method of data protection with the NM93CSxx EEPROMs is by using the Program Enable (PE) pin. The PE pin can have a delay signal placed on it via software control, or an external switch for hardware control. Either way reduces the odds of accidental overwrites during voltage transients caused by power outages, unplugging equipment, system noise, unregulated batteries, or when changing batteries.

The second method of data protection with the NM93CSxx EEPROMs is to use the Protect Register which is controlled by the Protect Register Enable (PRE) pin and software commands. This is the best method to prevent overwrites caused by disturbed reset operations and crashing controllers that often write "garbage" to EEPROMs during these periods. "Garbage" gets written to the EEPROM because of the "skipping" binary counter in the controller. Just by having the PRE pin externally controlled, or having extra commands to execute a write command, reduces the odds of overwrites to near zero for the NM93CSxx Family.

The final method of protecting information in the EEPROM is to use the Protect Register Disable (PRDS) command. Once this command is executed after using the Protect Register commands, the user selected portion of the EEPROM array becomes permanently disabled from all future writes. This is the best method for protecting security codes, calibration information and any other information that needs to become ROM once written into the EEPROM.

BRIEF OVERVIEW OF THE 68HC11 MICROCONTROLLER

The MC68HC11 is a high density CMOS microcontroller which contain a microcontroller unit (MCU) and highly sophisticated integrated peripheral capabilities. An eight-channel A/D converter is included on chip. An 8-bit pulse accumulator subsystem on chip can count external events or measure external periods. The main 16-bit, free-running timer system has three input capture lines, five output compare lines, and a real-time interrupt function. An asynchronous serial communications interface (SCI) and a synchronous serial peripheral interface (SPI) are also included.

The SPI is an independent serial communications subsystem which allows the MCU to communicate synchronously with peripheral devices. This application note describes assembly code which interfaces the MC68HC11 to the NM93CSxx Family of EEPROMs through the SPI without any intermediate logic.

TABLE I. Instruction Set for the NM93CSxx Family of EEPROMs

Command	Op Cd	Address NM93CS06 NM93CS46	Address NM93CS56 NM93CS66	Data	Pre	Pe	Comments
READ	10	A5–A0	A7–A0		0	X	Reads data stored in memory, starting at specified address.
WEN	00	11XXXX	11XXXXXX		0	1	Write enable must precede all programming modes.
WRITE	01	A5–A0	A7–A0	D15–D0	0	1	Writes register if address is unprotected.
WRALL	00	01XXXX	01XXXXXX	D15–D0	0	1	Writes all registers. Valid only when Protect Register is cleared.
WRDS	00	00XXXX	00XXXXXX		0	X	Disables all programming instructions.
PRREAD	10	XXXXXX	XXXXXXXX		1	X	Reads address stored in Protect Register.
PREN	00	11XXXX	11XXXXXX		1	1	Must immediately precede PRCLEAR, PRWRITE, and PRDS instructions.
PRCLEAR	11	111111	11111111		1	1	Clears the Protect Register, so that no registers are protected from WRITE. Protect register equals 0000.
PRWRITE	01	A5–A0	A7–A0		1	1	Programs address into Protect Register. Thereafter, memory addresses greater than or equal to the address in Protect Register are protected from WRITE.
PRDS	00	000000	00000000		1	1	One time only instruction after which the address in the Protect Register cannot be altered.

MC68HC11/NM93CSxx INTERFACE HARDWARE DESCRIPTION

A block diagram of the interface between the MC68HC11 microcontroller and the NM93CSxx family of serial EEPROMs is given in *Figure 1*. Straps are inserted in the PRE and PE lines in the schematic (attached) to permit hardware protection from accidental data corruption. By removing the straps, data cannot be written to the EEPROM, but the EEPROM can still be read.

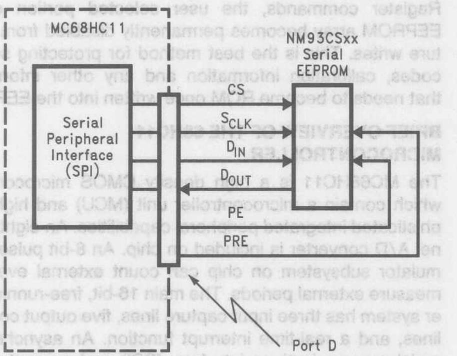

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FIGURE 1. 68HC11 to 93CSxx Block Diagram

MC68HC11/NM93CSxx INTERFACE CODE DESCRIPTION

The assembly code which interfaces the MC68HC11 microcontroller to the NM93CSxx serial EEPROMs is structured as 10 subroutines: one subroutine for each command type. A data flow diagram of the code is shown in *Figure 2*. Each routine pushes the values of the A, B, X, and Y accumulators on a subroutine call and restore their values on return. The routines expect the address of the command being sent (if required) to reside at XADDR, and the data to be sent (if required) to reside at location $XDAT_{HI}$ and $XDAT_{LO}$.

Reads of the serial EEPROM are implemented as *polled reads*; that is, the subroutine which implements the reads goes into a polling mode which checks that the read is complete before control is returned to the calling program. Writes to the EEPROM are implemented as *posted writes*; that is, the first byte of the command message is sent out, then control is returned to the calling program. The rest of the command message is sent out by an interrupt service routine which sends each additional byte as the SPI interrupts the main program when the previous byte is complete. This necessitates that each subroutine check that the previous command write is complete before it allows the next read or write to take place (implemented in subroutine WRPEN). Posted writes are used to improve real-time performance, particularly when the SPI clock rate is low. It also provides an example of implementing the MC68HC11 to NM93CSxx as a polled routine and as an interrupt driven routine.

Two commands: READ and PRRD, read data from the EEPROM; these commands are implemented such that the subroutine does not release control of the microcontroller until the SPI has completed sending and receiving the entire command message. The subroutines pack the READ or PRRD commands to be sent in the transmit buffer (XMESSx), set the count of the number of bytes in the command message (MESSCT), set the PRE and PE bits appropriately, and jump to the POLLRD routine. This routine applies the PRE, PE, and CS signals to the EEPROM and sends the first packet in the transmit buffer. The routine then waits for the SPI to acknowledge that it has completed sending that byte of the command message. The received data is then unloaded into the receive buffer ($RDAT_{HI}$ or $RDAT_{LO}$, whichever is appropriate). The next byte in the transmit buffer is then sent out, the routine waits for the SPI to acknowledge the byte was sent, then the received data is unloaded if necessary. This process is repeated until the entire command message is sent out and all the data is received from the EEPROM, then the subroutine relinquishes control to the main code.

The remainder of the commands (WRITE, PRWRITE, WREN, PREN, WRALL, PRWRITE, WRDIS, and PRD5) only write data to the EEPROM; these commands are implemented such that the subroutine releases control back to the main program immediately after the first byte of the command message is sent. These subroutines pack the commands to be sent in the transmit buffer (XMESSx), set the count of the number of bytes in the command message (MESSGT), set the PRE and PE bits appropriately, and jump to the PSTWR routine.

This routine applies the PRE, PE, and CS signals to the EEPROM and sends the first packet in the transmit buffer and control is returned to the main program. When the byte transfer is complete, the SPI interrupts the microcontroller, and the interrupt service routine sends the next byte of the command message if applicable.

A summary of the command messages, the data structure, and the bytes transmitted for each is given in Table II for NM93CS06 and NM93CS46, and Table III for NM93CS56 and NM93CS66.

TABLE II. SPI Messages for NM93CS06 and NM93CS46

Command	Pre	Pe	XMESS3	XMESS2	XMESS1	XMESS0	$RDAT_{HI}$	$RDAT_{LO}$
READ	0	0	0000 0011	0 a_5 a_4 a_3 a_2 a_1 a_0 0	0000 0000	0000 0000	D_{15}–D_8	D_7–D_0
WEN	0	1			0000 0001	0011 0000		
WRITE	0	1	0000 0001	0 1 a_5 a_4 a_3 a_2 a_1 a_0	D_{15}–D_8	D_7–D_0		
WRALL	0	1	0000 0001	0100 0000	D_{15}–D_8	D_7–D_0		
WRDS	0	1			0000 0001	0000 0000		
PRRD	1	0		0000 0011	0 a_5 a_4 a_3 a_2 a_1 a_0 0	0000 0000	xxxx xxx0	a_5 a_4 a_3 a_2 a_1 a_0 x x
PREN	1	1			0000 0001	0011 0000		
PRCLR	1	1			0000 0001	1111 1111		
PRWRT	1	1			0000 0001	0 1 a_5 a_4 a_3 a_2 a_1 a_0		
PRDS	1	1			0000 0001	0000 0000		

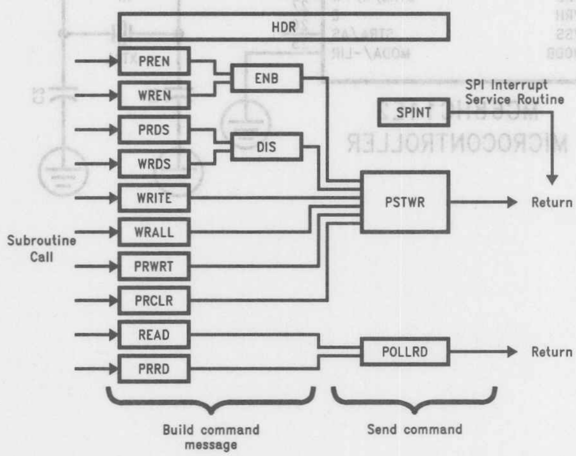

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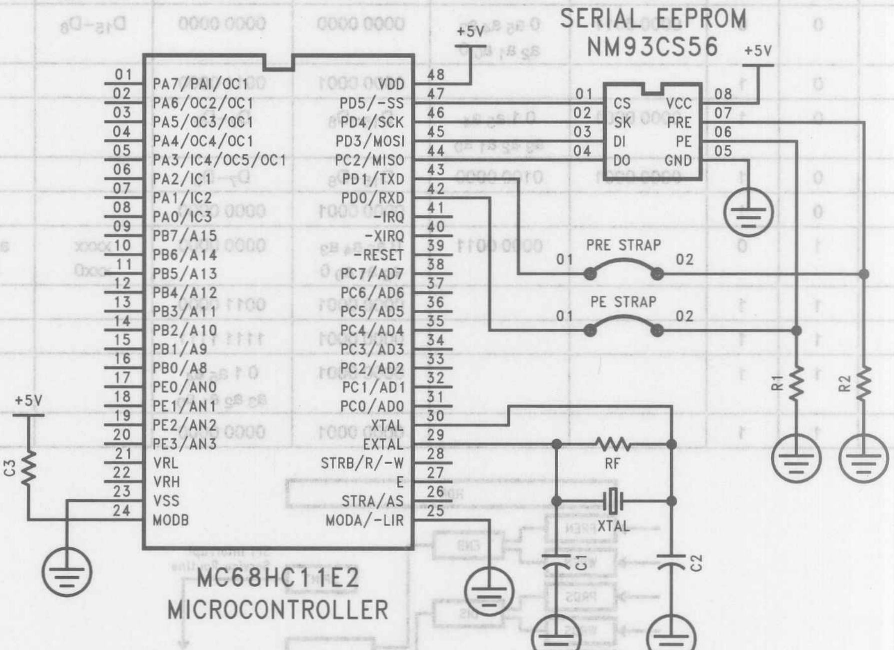
FIGURE 2. 93CSxx Interface Code Flow Diagram

READ	0	0	0000 110a_7	a_6 a_5 a_4 a_3 a_2 a_1 a_0 0	0000 0000	0000 0000	D_{15}–D_8	D_7–D_0
WEN	0	1			0000 0100	1100 0000		
WRITE	0	1	0000 0101	a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0	D_{15}–D_8	D_7–D_0		
WRALL	0	1	0000 0101	0000 0000	D_{15}–D_8	D_7–D_0		
WRDS	0	1			0000 0100	0000 0000		
PRRD	1	0		0000 110a_7	a_6 a_5 a_4 a_3 a_2 a_1 a_0 0	0000 0000	xxxx xxx0	a_5 a_4 a_3 a_2 a_1 a_0 x x
PREN	1	1			0000 0100	1100 0000		
PRCLR	1	0			0000 0111	1111 1111		
PRWRT	1	1			0000 0101	a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0		
PRDS	1	1			0000 0100	0000 0000		



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```
                ;MC68HC11 to NM93CS06/46 interface code
                ;Revision A                 7/28/93
                ;This assembly code implements the serial interface
                ;to the NM93CS06/46 serial EEPROM with Chip Security
                ;through the SPI interface and the rest of Port D.
                ;There are 10 commands:
                ;  WRITE                     Protect Reg WRite (PRWR)
                ;  READ                      Protect Reg ReaD (PRRD)
                ;  WRite ENable (WREN)       Protect Reg ENable (PREN)
                ;  WRite DiSable (WRDS)      Protect Reg DiSable (PRDS)
                ;  WRite ALL (WRALL)         Protect Reg CLeaR (PRCLR)
                ;Each EEPROM command type is implemented as a
                ;subroutine call. Address is passed to the routine
                ;in XADDR, data in XDATLO and XDATHI. Data is
                ;returned from read operations in RDATLO and RDATHI.

0000            $ include "header.asm"
0000            PORTD     equ $1008  ;Port D data Register
0000            DDRD      equ $1009  ;D Data Direction Register
0000            SPCR      equ $1028  ;SPI Control Register
0000            SPSR      equ $1029  ;SPI Status Register
0000            SPDR      equ $102a  ;SPI Data Register
0000            HPRIO     equ $103c  ;Interrupt Priority

0000            XMESS0    equ $00    ;Transmit Message Buffer 0
0000            XMESS1    equ $01    ;Transmit Message Buffer 1
0000            XMESS2    equ $02    ;Transmit Message Buffer 2
0000            XMESS3    equ $03    ;Transmit Message Buffer 3
0000            MESSCT    equ $04    ;Message Byte Count
0000            PREPE     equ $05    ;CS, Pre, Pe Bit settings
0000            EXTWR     equ $0b    ;Set if write takes Extra Time
0000            WRACTV    equ $0c    ;Set if write still active after
                                     ;message count goes to 00

0000            XADDR     equ $06    ;Transmit Address
0000            XDATLO    equ $07    ;Transmit Data low byte
0000            XDATHI    equ $08    ;Transmit Data high bype
0000            RDATLO    equ $09    ;Receive Data low byte
0000            RDATHI    equ $0a    ;Receive Data high byte

0000            $ include "init.asm"
                          ;Init initializes registers critical to SPI
                                                             operation

C000                      org $c000     ;Start code at C000
C000 8E00FF     init1     lds #$00ff    ;Locate Stack at 00FF
C003 863B                 ldaa #$3b     ;Initialize DDRD Register
C005 B71009               staa DDRD
C008 8653                 ldaa #$53     ;Initialize SPCR Register
C00A B71028               staa SPCR
C00D 8600                 ldaa #$00     ;Zero out Port D Outputs
C00F B71008               staa PORTD
C012 8603                 ldaa #$03     ;Set SPI Interrupt to highest
                                                              priority
C014 B7103C               staa HPRIO
C017 C6C0                 ldab #$c0     ;Turn off global interrupt disable
C019 06                   tap
C01A 8600                 ldaa #$00
```

TL/D/11918–4

4

```
C01C 9704                    staa MESSCT  ;Message count is zero
C01E 970C                    staa WRACTV  ;Write not active

C020 86AA        main        ldaa #$aa    ;Main give examples of using
                                          ;a few of the command routines
C022 9706                    staa XADDR   ;Load in transmit address
C024 8633                    ldaa #$33
C026 9707                    staa XDATLO  ;Load in low byte xmit data
C028 86CC                    ldaa #$cc
C02A 9708                    staa XDATHI  ;Load in hi byte xmit data
C02C BDC051                  jsr WREN     ;Call Write Enable
C02F BDC03E                  jsr PREN     ;Call Protect Register Enable
C032 BDC16D                  jsr PRCLR    ;Call Protect Register Clear
C035 BDC0F0                  jsr WRITE    ;Call Write
C038 BDC0A2                  jsr READ     ;Call Read
                                          ;(read back memory)
C03B 7EC020                  jmp main

C03E 36          PrEn        psha
C03F 37                      pshb
C040 3C                      pshx
C041 183C                    pshy
C043 BDC18C                  jsr WrPen    ;Subroutine Write Pending checks
                                          ;whether a previous write is still
                                          ;pending, and waits until it is
                                          ;done if there is.
C046 8623                    ldaa #$23
C048 9705                    staa PREPE   ;Set CS, PRE, and PE bits
C04A 8600                    ldaa #$00
C04C 970B                    staa EXTWR   ;No extra write time required
C04E 7EC061                  jmp Enb

C051 36          WrEn        psha
C052 37                      pshb
C053 3C                      pshx
C054 183C                    pshy
C056 BDC18C                  jsr WrPen
C059 8621                    ldaa #$21
C05B 9705                    staa PREPE   ;Set CS, PRE, and PE bits
C05D 8600                    ldaa #$00
C05F 970B                    staa EXTWR   ;No extra write time required

C061 8602        Enb         ldaa #$02
C063 9704                    staa MESSCT  ;Load message byte count
C065 8630                    ldaa #$30    ;Load last byte, op code=00
C067 9700                    staa XMESS0  ;Data is 110000
C069 8601                    ldaa #$01
C06B 9701                    staa XMESS1  ;Load start bit
C06D 7EC195                  jmp PstWr    ;Jump to Posted Write Routine

C070 36          PrDs        psha
C071 37                      pshb
C072 3C                      pshx
C073 183C                    pshy
C075 BDC18C                  jsr WrPen    ;Check Write still Pending?
C078 8623                    ldaa #$23
C07A 9705                    staa PREPE   ;Set CS, PRE, and PE bits
C07C 8601                    ldaa #$01
```

TL/D/11918–5

```
C07E 970B               staa EXTWR  ;Extra write time required
C080 7EC093             jmp Dis

C083 36        WrDs     psha
C084 37                 pshb
C085 3C                 pshx
C086 183C               pshy
C088 BDC18C             jsr WrPen   ;Check Write still Pending?
C08B 8621               ldaa #$21
C08D 9705               staa PREPE  ;Set CS, PRE, and PE bits
C08F 8600               ldaa #$00
C091 970B               staa EXTWR  ;No extra write time required

C093 8602      Dis      ldaa #$02
C095 9704               staa MESSCT ;Load message byte count
C097 8600               ldaa #$00   ;Load last byte, op code=00
C099 9700               staa XMESS0 ;Data = 000000
C09B 8601               ldaa #$01
C09D 9701               staa XMESS1 ;Load start bit
C09F 7EC195             jmp PstWr   ;jump to Posted Write Routine

C0A2 36        Read     psha
C0A3 37                 pshb
C0A4 3C                 pshx
C0A5 183C               pshy
C0A7 BDC18C             jsr WrPen   ;Check Write still Pending?
C0AA 8620               ldaa #$20
C0AC 9705               staa PREPE  ;Set CS, PRE, and PE bits
C0AE 8600               ldaa #$00
C0B0 970B               staa EXTWR  ;No extra write time required
C0B2 8604               ldaa #$04
C0B4 9704               staa MESSCT ;Load message byte count
C0B6 8600               ldaa #$00
C0B8 9700               staa XMESS0 ;Load low byte data (don't care)
C0BA 9701               staa XMESS1 ;Load hi byte data (don't care)
C0BC 9606               ldaa XADDR
C0BE 48                 asla
C0BF 847E               anda #$7e   ;Mask off bits 0 & 7 of address
C0C1 9702               staa XMESS2 ;Load address byte
C0C3 8603               ldaa #$03
C0C5 9703               staa XMESS3 ;Load start bit and MSB of op code
C0C7 7EC215             jmp PollRd  ;Jump to Polled Read Routine

C0CA 36        PrRd     psha
C0CB 37                 pshb
C0CC 3C                 pshx
C0CD 183C               pshy
C0CF BDC18C             jsr WrPen   ;Check Write still Pending?
C0D2 8622               ldaa #$22
C0D4 9705               staa PREPE  ;Set CS, PRE, and PE bits
C0D6 8600               ldaa #$00
C0D8 970B               staa EXTWR  ;No extra write time required
C0DA 8603               ldaa #$03
C0DC 9704               staa MESSCT ;Load message byte count
C0DE 8600               ldaa #$00
C0E0 9700               staa XMESS0 ;Load low byte (don't care)
C0E2 9606               ldaa XADDR
C0E4 48                 asla
```

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```
C0E5 847E                 anda #$7e   ;Mask off bits 0 & 7 of address
C0E7 9701                 staa XMESS1 ;Load address byte
C0E9 8603                 ldaa #$03
C0EB 9702                 staa XMESS2 ;Load start bit and MSB of op code
C0ED 7EC215               jmp PollRd  ;Jump to Polled Read Routine

C0F0 36          Write    psha
C0F1 37                   pshb
C0F2 3C                   pshx
C0F3 183C                 pshy
C0F5 BDC18C               jsr WrPen   ;Check Write still Pending?
C0F8 8621                 ldaa #$21
C0FA 9705                 staa PREPE  ;Set CS, PRE, and PE bits
C0FC 8601                 ldaa #$01
C0FE 970B                 staa EXTWR  ;Extra write time required
C100 8604                 ldaa #$04
C102 9704                 staa MESSCT ;Load message byte count
C104 9607                 ldaa XDATLO
C106 9700                 staa XMESS0 ;Load low xmit data byte
C108 9608                 ldaa XDATHI
C10A 9701                 staa XMESS1 ;Load high xmit data byte
C10C 863F                 ldaa #$3f
C10E C640                 ldab #$40
C110 9406                 anda XADDR  ;Mask off bits 6 & 7 of address
C112 9702                 staa XMESS2
C114 DA02                 orab XMESS2 ;Add op code=01 to address
C116 D702                 stab XMESS2 ;Load address byte
C118 8601                 ldaa #$01
C11A 9703                 staa XMESS3 ;Load start bit
C11C 7EC195               jmp PstWr   ;Jump to Posted Write Routine

C11F 36          WrAll    psha
C120 37                   pshb
C121 3C                   pshx
C122 183C                 pshy
C124 BDC18C               jsr WrPen   ;Check if Write still Pending?
C127 8621                 ldaa #$21
C129 9705                 staa PREPE  ;Set CS, PRE, and PE bits
C12B 8601                 ldaa #$01
C12D 970B                 staa EXTWR  ;Extra write time required
C12F 8604                 ldaa #$04
C131 9704                 staa MESSCT ;Load message byte count
C133 9607                 ldaa XDATLO
C135 9700                 staa XMESS0 ;Load low xmit data byte
C137 9608                 ldaa XDATHI
C139 9701                 staa XMESS1 ;Load high xmit data byte
C13B 8610                 ldaa #$10
C13D 9702                 staa XMESS2 ;Load op code=00, rest 010000
C13F 8601                 ldaa #$01
C141 9703                 staa XMESS3 ;Load start bit
C143 7EC195               jmp PstWr   ;Jump to Posted Write Routine

C146 36          PrWrt    psha
C147 37                   pshb
C148 3C                   pshx
C149 183C                 pshy
C14B BDC18C               jsr WrPen   ;Check if Write still Pending?
C14E 8623                 ldaa #$23
```

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```
C150 9705                    staa PREPE  ;Set CS, PRE, and PE bits
C152 8601                    ldaa #$01
C154 970B                    staa EXTWR  ;Extra write time required
C156 8602                    ldaa #$02
C158 9704                    staa MESSCT ;Load message byte count
C15A 863F                    ldaa #$3f
C15C C640                    ldab #$40
C15E 9406                    anda XADDR  ;Mask off bits 6 & 7 of address
C160 9700                    staa XMESS0
C162 DA00                    orab XMESS0 ;Add op code=01 to address
C164 D700                    stab XMESS0 ;Load address byte
C166 8601                    ldaa #$01
C168 9701                    staa XMESS1 ;Load start bit
C16A 7EC195                  jmp PstWr   ;Jump to Posted Write Routine
C16D 36             PrClr    psha
C16E 37                      pshb
C16F 3C                      pshx
C170 183C                    pshy
C172 BDC18C                  jsr WrPen   ;Check if Write still Pending?
C175 8623                    ldaa #$23
C177 9705                    staa PREPE  ;Set CS, PRE, and PE bits
C179 8601                    ldaa #$01
C17B 970B                    staa EXTWR  ;Extra write time required
C17D 8602                    ldaa #$02
C17F 9704                    staa MESSCT ;Load message byte count
C181 86FF                    ldaa #$0ff
C183 9700                    staa XMESS0 ;Load address byte of all one's
C185 8601                    ldaa #$01
C187 9701                    staa XMESS1 ;Load start bit
C189 7EC195                  jmp PstWr   ;Jump to Posted Write Routine
C18C 9604           WrPen    ldaa MESSCT ;Write Pending Subroutine:
C18E 26FC                    bne WrPen   ;check if previous message byte
                                         ;count is 0 before preceeding
C190 960C                    ldaa WRACTV ;Check write still active even
C192 26F8                    bne WrPen   ;though last message sent
C194 39                      rts         ;Note that a bad write (ie. WREN
                                         ;has not been set) will not return
                                         ;a ready so this loop will never
                                         ;stop... a timer (approx 10ms)
                                         ;should be implemented to monitor
                                         ;for this situation.
C195 8680           PstWr    ldaa #$80
C197 BA1028                  oraa SPCR
C19A B71028                  staa SPCR   ;Enable SPI Interrupt
C19D D604                    ldab MESSCT ;Message byte count in B
C19F CE0000                  ldx #XMESS0 ;Address of last message byte
C1A2 B61008                  ldaa PORTD  ;Read Port D
C1A5 9A05                    oraa PREPE
C1A7 B71008                  staa PORTD  ;Set CS, PRE, PE lines of PORT D
C1AA 5A                      decb        ;decrement message indexing B
C1AB 3A                      abx         ;index address in X to mess byte
C1AC A600                    ldaa 0,x    ;Load A with message byte data
C1AE B7102A                  staa SPDR   ;Send data packet (start bit)
C1B1 1838                    puly
C1B3 38                      pulx
```

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```
C1B4 33                         pulb
C1B5 32                         pula
C1B6 39                         rts            ;Return to main program...the
                                               ;rest of the message is sent
                                               ;by interrupt routine SpInt

C1B7 F61029        SpInt        ldab SPSR      ;Check that interrupt cause by
C1BA 2A58                       bpl done       ;SPIF (not mode error)
C1BC B6102A                     ldaa SPDR      ;Clear SPIF interrupt
C1BF D604                       ldab MESSCT    ;Load message byte count in B
C1C1 272D                       beq Twp        ;Jump to post write poller
C1C3 5A                         decb           ;Decrement message count
C1C4 D704                       stab MESSCT    ;Store that 1 byte was sent
C1C6 270D                       beq SsOff      ;Branch if last byte was sent
C1C8 CE0000                     ldx #XMESS0    ;Load address of last byte in X
C1CB 5A                         decb           ;Decrement message index B
C1CC 3A                         abx            ;Index address in X to next byte
C1CD A600                       ldaa 0,x       ;Load next message byte
C1CF B7102A                     staa SPDR      ;Send message byte
C1D2 7EC214                     jmp Done       ;Return to Main Program
C1D5 B61008        SsOff        ldaa PORTD
C1D8 84DF                       anda #$dF
C1DA B71008                     staa PORTD     ;Turn off CS
C1DD 84FC                       anda #$fc
C1DF B71008                     staa PORTD     ;Turn off PRE, PE
C1E2 960B                       ldaa EXTWR
C1E4 2716                       beq Off        ;Jump to turn off interrupts
C1E6 B61008                     ldaa PORTD
C1E9 8A20                       oraa #$20
C1EB B71008                     staa PORTD     ;Turn CS on
C1EE 8600                       ldaa #$00
C1F0 81FF          Twp          cmpa #$ff      ;Check if write complete
C1F2 2617                       bne Send       ;No, send another idle byte
C1F4 B61008                     ldaa PORTD
C1F7 84DF                       anda #$df
C1F9 B71008                     staa PORTD     ;Turn off CS
C1FC 867F          Off          ldaa #$7f
C1FE B41028                     anda SPCR
C201 B71028                     staa SPCR      ;Disable SPI interrupt
C204 8600                       ldaa #$00
C206 970C                       staa WRACTV    ;Write complete
C208 7EC214                     jmp Done
C20B 8601          Send         ldaa #$01
C20D 970C                       staa WRACTV    ;Set write active
C20F 8600                       ldaa #$00
C211 B7102A                     staa SPDR      ;Send data
C214 3B            Done         rti            ;Return to main program

C215 D604          PollRd       ldab MESSCT    ;Load message byte count in B
C217 CE0000                     ldx #XMESS0    ;Load address of last byte in X
C21A B61008                     ldaa PORTD
C21D 9A05                       oraa PREPE
C21F B71008                     staa PORTD     ;Set CS, PRE, and PE
C222 3A                         abx            ;Index into address past byte
C223 09            SendX        dex            ;Decrement back to byte
C224 5A                         decb           ;Decrement index B
C225 A600                       ldaa 0,x       ;Load next message byte
C227 B7102A                     staa SPDR      ;Send message byte
```

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```
C232 C100            cmpb #$00    ;Last message byte?
C234 2705            beq StrLo
C236 970A            staa RDATHI  ;Save byte as hi receive byte
C238 7EC223          jmp SendX    ;Send/receive next byte
C23B 9709    StrLo   staa RDATLO  ;Store lo receive byte
C23D D704            stab MESSCT  ;Zero out message byte count
C23F 86DC            ldaa #$dc
C241 B41008          anda PORTD
C244 B71008          staa PORTD   ;Turn off CS, PRE, PE
C247 1838            puly
C249 38              pulx
C24A 33              pulb
C24B 32              pula
C24C 39              rts          ;Return to Main Program

FFD8                 org $ffd8
FFD8 C1B7            fdb SpInt    ;Set SPI interrupt vector to
                                  ;point to SPI interrupt service
                                  ;routine
```

```
Symbol Table

DDRD      1009
DIS       C093
DONE      C214
ENB       C061
EXTWR     000B
HPRIO     103C
INIT1     C000
MAIN      C020
MESSCT    0004
OFF       C1FC
POLLRD    C215
PORTD     1008
PRCLR     C16D
PRDS      C070
PREN      C03E
PREPE     0005
PRRD      C0CA
PRWRT     C146
PSTWR     C195
RDATHI    000A
RDATLO    0009
READ      C0A2
SEND      C20B
SENDX     C223
SPCR      1028
SPDR      102A
SPINT     C1B7
SPSR      1029
SSOFF     C1D5
STRLO     C23B
TWP       C1F0
WAIT      C22A
WRACTV    000C
WRALL     C11F
WRDS      C083
WREN      C051
WRITE     C0F0
WRPEN     C18C
XADDR     0006
XDATHI    0008
XDATLO    0007
XMESS0    0000
XMESS1    0001
XMESS2    0002
XMESS3    0003
```

TL/D/11918–10

TL/D/11918–11

4

```
                  ;MC68HC11 to NM93CS56/66 interface code
                  ;Revision A                 7/28/93
                  ;This assembly code implements the serial interface
                  ;to the NM93CS56/66 serial EEPROM with Chip Security
                  ;through the SPI interface and the rest of Port D.
                  ;There are 10 commands:
                  ;  WRITE                      Protect Reg WRite (PRWR)
                  ;  READ                       Protect Reg ReaD (PRRD)
                  ;  WRite ENable (WREN)        Protect Reg ENable (PREN)
                  ;  WRite DiSable (WRDS)       Protect Reg DiSable (PRDS)
                  ;  WRite ALL (WRALL)          Protect Reg CLeaR (PRCLR)
                  ;Each EEPROM command type is implemented as a
                  ;subroutine call. Address is passed to the routine
                  ;in XADDR, data in XDATLO and XDATHI. Data is
                  ;returned from read operations in RDATLO and RDATHI.

0000              $ include "header.asm"
0000              PORTD     equ $1008   ;Port D data Register
0000              DDRD      equ $1009   ;D Data Direction Register
0000              SPCR      equ $1028   ;SPI Control Register
0000              SPSR      equ $1029   ;SPI Status Register
0000              SPDR      equ $102a   ;SPI Data Register
0000              HPRIO     equ $103c   ;Interrupt Priority

0000              XMESS0    equ $00     ;Transmit Message Buffer 0
0000              XMESS1    equ $01     ;Transmit Message Buffer 1
0000              XMESS2    equ $02     ;Transmit Message Buffer 2
0000              XMESS3    equ $03     ;Transmit Message Buffer 3
0000              MESSCT    equ $04     ;Message Byte Count
0000              PREPE     equ $05     ;CS, Pre, Pe Bit settings
0000              EXTWR     equ $0b     ;Set if write takes Extra Time
0000              WRACTV    equ $0c     ;Set if write still active after
                                        ;message count goes to 00

0000              XADDR     equ $06     ;Transmit Address
0000              XDATLO    equ $07     ;Transmit Data low byte
0000              XDATHI    equ $08     ;Transmit Data high bype
0000              RDATLO    equ $09     ;Receive Data low byte
0000              RDATHI    equ $0a     ;Receive Data high byte

0000              $ include "init.asm"
                            ;Init initializes registers critical to SPI
                                                              operation

C000                        org $c000   ;Start code at C000
C000 8E00FF       init1     lds #$00ff  ;Locate Stack at 00FF
C003 863B                   ldaa #$3b   ;Initialize DDRD Register
C005 B71009                 staa DDRD
C008 8653                   ldaa #$53   ;Initialize SPCR Register
C00A B71028                 staa SPCR
C00D 8600                   ldaa #$00   ;Zero out Port D Outputs
C00F B71008                 staa PORTD
C012 8603                   ldaa #$03   ;Set SPI Interrupt to highest
                                                              priority
C014 B7103C                 staa HPRIO
C017 C6C0                   ldab #$c0   ;Turn off global interrupt disable
C019 06                     tap
C01A 8600                   ldaa #$00
```

TL/D/11918-12

```
C01C 9704               staa MESSCT  ;Message count is zero
C01E 970C               staa WRACTV  ;Write not active

C020 8656    main       ldaa #$56    ;Main give examples of using
                                     ;a few of the command routines
C022 9706               staa XADDR   ;Load in transmit address
C024 8633               ldaa #$33
C026 9707               staa XDATLO  ;Load in low byte xmit data
C028 86CC               ldaa #$cc
C02A 9708               staa XDATHI  ;Load in hi byte xmit data
C02C BDC054             jsr WREN     ;Call Write Enable
C02F BDC041             jsr PREN     ;Call Protect Register Enable
C032 BDC15C             jsr PRCLR    ;Call Protect Register Clear
C035 BDC041             jsr PREN     ;Call Protect Register Enable
C038 BDC13D             jsr PRWRT    ;Call Protect Register Write
C03B BDC0CB             jsr PRRD     ;Call Protect Register Read
                                     ;(read back Protect Register)
C03E 7EC020             jmp main

C041 36      PrEn       psha
C042 37                 pshb
C043 3C                 pshx
C044 183C               pshy
C046 BDC17B             jsr WrPen  ;Subroutine Write Pending checks
                                   ;whether a previous write is still
                                   ;pending, and waits until it is
                                   ;done if there is.
C049 8623               ldaa #$23
C04B 9705               staa PREPE ;Set CS, PRE, and PE bits
C04D 8600               ldaa #$00
C04F 970B               staa EXTWR ;No extra time after command
C051 7EC064             jmp Enb

C054 36      WrEn       psha
C055 37                 pshb
C056 3C                 pshx
C057 183C               pshy
C059 BDC17B             jsr WrPen
C05C 8621               ldaa #$21
C05E 9705               staa PREPE ;Set CS, PRE, and PE bits
C060 8600               ldaa #$00
C062 970B               staa EXTWR ;No extra time after command

C064 8602    Enb        ldaa #$02
C066 9704               staa MESSCT ;Load message byte count
C068 86C0               ldaa #$c0   ;Load last byte
C06A 9700               staa XMESS0 ;Data is 11000000
C06C 8604               ldaa #$04
C06E 9701               staa XMESS1 ;Load start bit & op code=00
C070 7EC184             jmp PstWr   ;Jump to Posted Write Routine

C073 36      PrDs       psha
C074 37                 pshb
C075 3C                 pshx
C076 183C               pshy
C078 BDC17B             jsr WrPen  ;Check Write still Pending?
C07B 8623               ldaa #$23
C07D 9705               staa PREPE  ;Set CS, PRE, and PE bits
```

TL/D/11918-13

```
C07F 8601                 ldaa #$01
C081 970B                 staa EXTWR  ;Extra time after command
C083 7EC096               jmp Dis

C086 36          WrDs     psha
C087 37                   pshb
C088 3C                   pshx
C089 183C                 pshy
C08B BDC17B               jsr WrPen   ;Check Write still Pending?
C08E 8621                 ldaa #$21
C090 9705                 staa PREPE  ;Set CS, PRE, and PE bits
C092 8600                 ldaa #$00
C094 970B                 staa EXTWR  ;No extra time after command

C096 8602        Dis      ldaa #$02
C098 9704                 staa MESSCT ;Load message byte count
C09A 8600                 ldaa #$00   ;Load last byte
C09C 9700                 staa XMESS0 ;Data = 0000 0000
C09E 8604                 ldaa #$04
C0A0 9701                 staa XMESS1 ;Load start bit & op code=00
C0A2 7EC184               jmp PstWr   ;jump to Posted Write Routine

C0A5 36          Read     psha
C0A6 37                   pshb
C0A7 3C                   pshx
C0A8 183C                 pshy
C0AA BDC17B               jsr WrPen   ;Check Write still Pending?
C0AD 8620                 ldaa #$20
C0AF 9705                 staa PREPE  ;Set CS, PRE, and PE bits
C0B1 8600                 ldaa #$00
C0B3 970B                 staa EXTWR  ;No extra time after command
C0B5 8604                 ldaa #$04
C0B7 9704                 staa MESSCT ;Load message byte count
C0B9 8600                 ldaa #$00
C0BB 9700                 staa XMESS0 ;Load low byte data (don't care)
C0BD 9701                 staa XMESS1 ;Load hi byte data (don't care)
C0BF D606                 ldab XADDR
C0C1 8606                 ldaa #$06
C0C3 05                   asld
C0C4 D702                 stab XMESS2 ;Load address
C0C6 9703                 staa XMESS3 ;Load start bit and op code=10
C0C8 7EC204               jmp PollRd  ;Jump to Polled Read Routine

C0CB 36          PrRd     psha
C0CC 37                   pshb
C0CD 3C                   pshx
C0CE 183C                 pshy
C0D0 BDC17B               jsr WrPen   ;Check Write still Pending?
C0D3 8622                 ldaa #$22
C0D5 9705                 staa PREPE  ;Set CS, PRE, and PE bits
C0D7 8600                 ldaa #$00
C0D9 970B                 staa EXTWR  ;No extra time after command
C0DB 8603                 ldaa #$03
C0DD 9704                 staa MESSCT ;Load message byte count
C0DF 8600                 ldaa #$00
C0E1 9700                 staa XMESS0 ;Load low byte (don't care)
C0E3 D606                 ldab XADDR
C0E5 8606                 ldaa #$06
```

TL/D/11918–14

```
COEF 36             Write    psha
C0F0 37                      pshb
C0F1 3C                      pshx
C0F2 183C                    pshy
C0F4 BDC17B                  jsr WrPen   ;Check Write still Pending?
C0F7 8621                    ldaa #$21
C0F9 9705                    staa PREPE  ;Set CS, PRE, and PE bits
C0FB 8601                    ldaa #$01
C0FD 970B                    staa EXTWR  ;Extra time after command
C0FF 8604                    ldaa #$04
C101 9704                    staa MESSCT ;Load message byte count
C103 9607                    ldaa XDATLO
C105 9700                    staa XMESS0 ;Load low xmit data byte
C107 9608                    ldaa XDATHI
C109 9701                    staa XMESS1 ;Load high xmit data byte
C10B 9606                    ldaa XADDR
C10D 9702                    staa XMESS2 ;Load address byte
C10F 8605                    ldaa #$05
C111 9703                    staa XMESS3 ;Load start bit & op code=01
C113 7EC184                  jmp PstWr   ;Jump to Posted Write Routine

C116 36             WrAll    psha
C117 37                      pshb
C118 3C                      pshx
C119 183C                    pshy
C11B BDC17B                  jsr WrPen   ;Check if Write still Pending?
C11E 8621                    ldaa #$21
C120 9705                    staa PREPE  ;Set CS, PRE, and PE bits
C122 8601                    ldaa #$01
C124 970B                    staa EXTWR  ;Extra time after command
C126 8604                    ldaa #$04
C128 9704                    staa MESSCT ;Load message byte count
C12A 9607                    ldaa XDATLO
C12C 9700                    staa XMESS0 ;Load low xmit data byte
C12E 9608                    ldaa XDATHI
C130 9701                    staa XMESS1 ;Load high xmit data byte
C132 8640                    ldaa #$40
C134 9702                    staa XMESS2 ;Load address 0100 0000
C136 8604                    ldaa #$04
C138 9703                    staa XMESS3 ;Load start bit & op code=00
C13A 7EC184                  jmp PstWr   ;Jump to Posted Write Routine

C13D 36             PrWrt    psha
C13E 37                      pshb
C13F 3C                      pshx
C140 183C                    pshy
C142 BDC17B                  jsr WrPen   ;Check if Write still Pending?
C145 8623                    ldaa #$23
C147 9705                    staa PREPE  ;Set CS, PRE, and PE bits
C149 8601                    ldaa #$01
C14B 970B                    staa EXTWR  ;Extra time after command
C14D 8602                    ldaa #$02
C14F 9704                    staa MESSCT ;Load message byte count
```

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```
C151 9606              ldaa XADDR
C153 9700              staa XMESS0 ;Load address byte
C155 8605              ldaa #$05
C157 9701              staa XMESS1 ;Load start bit & op code=01
C159 7EC184            jmp PstWr   ;Jump to Posted Write Routine

C15C 36        PrClr   psha
C15D 37                pshb
C15E 3C                pshx
C15F 183C              pshy
C161 BDC17B            jsr WrPen   ;Check if Write still Pending?
C164 8623              ldaa #$23
C166 9705              staa PREPE  ;Set CS, PRE, and PE bits
C168 8601              ldaa #$01
C16A 970B              staa EXTWR  ;Extra time after command
C16C 8602              ldaa #$02
C16E 9704              staa MESSCT ;Load message byte count
C170 86FF              ldaa #$ff
C172 9700              staa XMESS0 ;Load address byte of all one's
C174 8607              ldaa #$07
C176 9701              staa XMESS1 ;Load start bit & op code=11
C178 7EC184            jmp PstWr   ;Jump to Posted Write Routine

C17B 9604      WrPen   ldaa MESSCT ;Write Pending Subroutine:
C17D 26FC              bne WrPen   ;check if previous message byte
                                   ;count is 0 before preceeding
C17F 960C              ldaa WRACTV ;Check write still active even
C181 26F8              bne WrPen   ;tho last message sent
C183 39                rts         ;Note that a bad write(ie. WREN
                                   ;has not been set) will not return
                                   ;a ready so this loop will never
                                   ;end...a timer (approx 10ms) would
                                   ;normally be implemented to
                                   ;monitor this.

C184 8680      PstWr   ldaa #$80
C186 BA1028            oraa SPCR
C189 B71028            staa SPCR   ;Enable SPI Interrupt
C18C D604              ldab MESSCT ;Message byte count in B
C18E CE0000            ldx #XMESS0 ;Address of last message byte
C191 B61008            ldaa PORTD  ;Read Port D
C194 9A05              oraa PREPE
C196 B71008            staa PORTD  ;Set CS, PRE, PE lines of PORT D
C199 5A                decb        ;decrement message indexing B
C19A 3A                abx         ;index address in X to mess byte
C19B A600              ldaa 0,x    ;Load A with message byte data-
C19D B7102A            staa SPDR   ;Send data packet (start bit)
C1A0 1838              puly
C1A2 38                pulx
C1A3 33                pulb
C1A4 32                pula
C1A5 39                rts         ;Return to main program...the
                                   ;rest of the message is sent
                                   ;by interrupt routine SpInt

C1A6 F61029    SpInt   ldab SPSR   ;Check that interrupt cause by
C1A9 2A58              bpl done    ;SPIF (not mode error)
C1AB B6102A            ldaa SPDR   ;Clear SPIF interrupt
```

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```
C1AE D604              ldab MESSCT ;Load message byte count in B
C1B0 272D              beq Twp     ;Jump to post write poller
C1B2 5A                decb        ;Decrement message count
C1B3 D704              stab MESSCT ;Store that 1 byte was sent
C1B5 270D              beq SsOff   ;Branch if last byte was sent
C1B7 CE0000            ldx #XMESS0 ;Load address of last byte in X
C1BA 5A                decb        ;Decrement message index B
C1BB 3A                abx         ;Index address in X to next byte
C1BC A600              ldaa 0,x    ;Load next message byte
C1BE B7102A            staa SPDR   ;Send message byte
C1C1 7EC203            jmp Done    ;Return to Main Program
C1C4 B61008     SsOff  ldaa PORTD
C1C7 84DF              anda #$dF
C1C9 B71008            staa PORTD  ;Turn off CS
C1CC 84FC              anda #$fc
C1CE B71008            staa PORTD  ;Turn off PRE, PE
C1D1 960B              ldaa EXTWR  ;Zero out Extra Write time
C1D3 2716              beq Off     ;jump to turn off interrupt
C1D5 B61008            ldaa PORTD
C1D8 8A20              oraa #$20
C1DA B71008            staa PORTD  ;Turn on CS
C1DD 8600              ldaa #$00
C1DF 81FF       Twp    cmpa #$ff   ;Check if write complete
C1E1 2617              bne Send    ;No, send another idle byte
C1E3 B61008            ldaa PORTD
C1E6 84DF              anda #$df
C1E8 B71008            staa PORTD  ;Turn off CS
C1EB 867F       Off    ldaa #$7f
C1ED B41028            anda SPCR
C1F0 B71028            staa SPCR   ;Disable SPI interrupt
C1F3 8600              ldaa #$00
C1F5 970C              staa WRACTV ;Write complete
C1F7 7EC203            jmp Done
C1FA 8601       Send   ldaa #$01
C1FC 970C              staa WRACTV
C1FE 8600              ldaa #$00
C200 B7102A            staa SPDR
C203 3B         Done   rti         ;Return to main program

C204 D604       PollRd ldab MESSCT ;Load message byte count in B
C206 CE0000            ldx #XMESS0 ;Load address of last byte in X
C209 B61008            ldaa PORTD
C20C 9A05              oraa PREPE
C20E B71008            staa PORTD  ;Set CS, PRE, and PE
C211 3A                abx         ;Index into address past byte
C212 09         SendX  dex         ;Decrement back to byte
C213 5A                decb        ;Decrement index B
C214 A600              ldaa 0,x    ;Load next message byte
C216 B7102A            staa SPDR   ;Send message byte
C219 B61029     Wait   ldaa SPSR   ;Load SPI Status register
C21C 2AFB              bpl Wait    ;Wait unit SPIF is set
C21E B6102A            ldaa SPDR   ;Load in data to A
C221 C100              cmpb #$00   ;Last message byte?
C223 2705              beq StrLo
C225 970A              staa RDATHI ;Save byte as hi receive byte
C227 7EC212            jmp SendX   ;Send/receive next byte
C22A 9709       StrLo  staa RDATLO ;Store lo receive byte
C22C D704              stab MESSCT ;Zero out message byte count
```

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4

```
C22E 86DC          ldaa #$dc
C230 B41008        anda PORTD
C233 B71008        staa PORTD    ;Turn off CS, PRE, PE
C236 1838          puly
C238 38            pulx
C239 33            pulb
C23A 32            pula
C23B 39            rts           ;Return to Main Program

FFD8               org $ffd8
FFD8 C1A6          fdb SpInt     ;Set SPI interrupt vector to
                                 ;point to SPI interrupt service
                                 ;routine
```

TL/D/11918–18

Symbol Table

```
DDRD      1009
DIS       C096
DONE      C203
ENB       C064
EXTWR     000B
HPRIO     103C
INIT1     C000
MAIN      C020
MESSCT    0004
OFF       C1EB
POLLRD    C204
PORTD     1008
PRCLR     C15C
PRDS      C073
PREN      C041
PREPE     0005
PRRD      C0CB
PRWRT     C13D
PSTWR     C184
RDATHI    000A
RDATLO    0009
READ      C0A5
SEND      C1FA
SENDX     C212
SPCR      1028
SPDR      102A
SPINT     C1A6
SPSR      1029
SSOFF     C1C4
STRLO     C22A
TWP       C1DF
WAIT      C219
WRACTV    000C
WRALL     C116
WRDS      C086
WREN      C054
WRITE     C0EF
WRPEN     C17B
XADDR     0006
XDATHI    0008
XDATLO    0007
XMESS0    0000
XMESS1    0001
XMESS2    0002
XMESS3    0003
```

TL/D/11918–19

National offers a broad line of serial interface EEPROMs which share a common set of features:

- Low cost
- Single supply in all modes (+5V ± 10%)
- TTL compatible interface
- MICROWIRE™ compatible interface
- Read-Only mode or read-write mode

This Application Brief will address protecting data in any of National's Serial Interface EEPROMs by using read-only mode.

Whereas EEPROM is non-volatile and does not require V_{CC} to retain data, the problem exists that stored data can be destroyed during power transitions. This is due to either uncontrolled interface signals during power transitions or noise on the power supply lines. There are various hardware design considerations which can help eliminate the problem although the simplest most effective method may be the following programming method.

All National Serial EEPROMs, when initially powered up are in the Program Disable Mode*. In this mode, the EEPROM will abort any requested Erase or Write cycles. Prior to Erasing or Writing it is necessary to place the device in the Program Enable Mode†. Following placing the device in the Program Enable Mode, Erase and Write will remain enabled until either executing the Disable instruction or removing V_{CC}. Having V_{CC} unexpectedly removed often results in uncontrolled interface signals which could result in the EEPROM interpreting a programming instruction causing data to be destroyed.

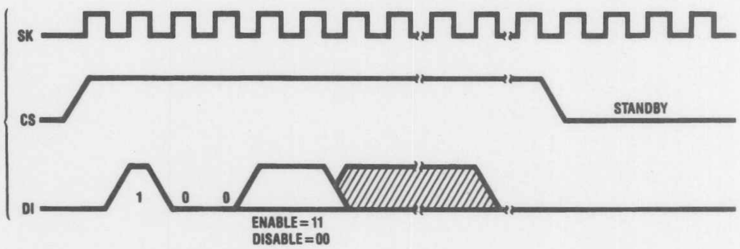
Upon power up the EEPROM will automatically enter the Program Disable Mode. Subsequently the design should incorporate the following to achieve protection of stored data.

1) The device powers up in the read-only mode. However, as a backup, the EWDS instruction should be executed as soon as possible after V_{CC} to the EEPROM is powered up to ensure that it is in the read-only mode.

2) Immediately preceding a programming instruction (ERASE, WRITE, ERAL or WRAL), the EWEN instruction should be executed to enable the device for programming; the EWDS instruction should be executed immediately following the programming instruction to return

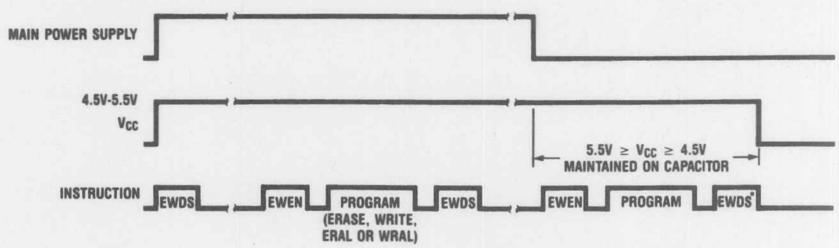
*EWDS or WDS, depending on exact device.

†EWEN or WEN, depending on exact device.



TL/D/7085-1

FIGURE 1. EWEN, EWDS Instruction Timing



TL/D/7085-2

*EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 2. Typical Instruction Flow for Maximum Data Protection

3) Special care must be taken in designs in which programming instructions are initiated to store data in the EEPROM after the main power supply has gone down. This is usually accomplished by maintaining V_{CC} for the EEPROM and its controller on a capacitor for a sufficient amount of time (approximately 50 ms, depending on the clock rate) to complete these operations. This capacitor ately following the last programming instruction. FAILURE TO EXECUTE THE LAST EWDS INSTRUCTION BEFORE V_{CC} DROPS BELOW 4.5 VOLTS MAY CAUSE INADVERTENT DATA DISTURB DURING SUBSEQUENT POWER DOWN AND/OR POWER UP TRANSIENTS.

Electronic Compass Calibration Made Easy with EEPROMs

National Semiconductor
Application Brief 18
Doug Zrebski

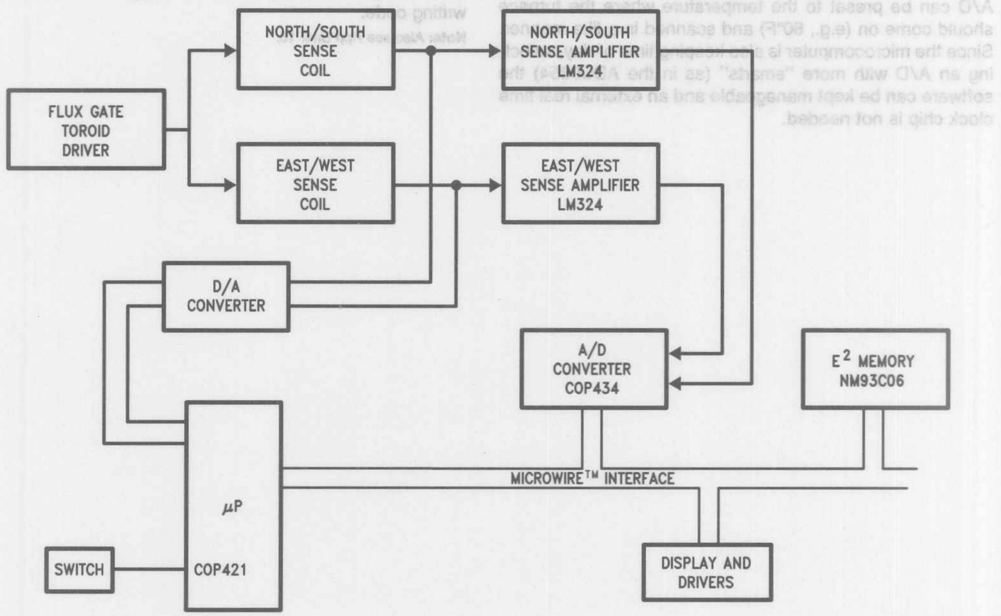
When a compass is first installed in a vehicle, or when new equipment, such as car speakers, are added to a vehicle with a compass, the compass must be compensated for stray magnetic fields. With a magnetic compass, it must be pointed towards magnetic north and then adjusted. This procedure is repeated at all four main points of the compass until the compass is calibrated. This procedure is lengthy and also requires another calibrated compass to point the vehicle in the correct direction.

The block diagram illustrates an electronic compass that, with the aide of an E^2 memory, makes adjusting a compass as easy as pushing a button, and also eliminates the need for another compass. In addition it gives you the ability to adjust for variation between magnetic and true north. This is a major advantage because it is something that even the most expensive magnetic compass cannot do.

The brain of the electronic compass is the COP421 microcontroller. There are two sense coils, one for north/south and one for east/west. The output of each of the sense amplifiers is an analog voltage which is fed into the A to D converter. These voltages are read by the COP421 over the microwire interface. From these voltages, the microcontroller determines the direction and displays the results once again over the microwire interface. To compensate the compass in a new environment the procedure is very simple. Start by pointing the car in any direction and push the switch. The CPU at this time will measure the voltage at the sense amplifiers and store this information in the E^2 memory over the microwire interface. Now the vehicle is turned 180°, and the button is pushed again. The same procedure will be followed internally. The compensation procedures are now complete. During operation the CPU will compensate for stray fields by adding an analog voltage back into the sense amplifiers. This value is stored in E^2 memory and not lost when the power is turned off, but is readjustable if its environment is modified.

Compass variation is the difference between true and magnetic north. This variation differs all over the world and is something that must be taken into consideration when navigating by compass. With the E^2 memory device, a variance can be programmed in for any given location. In California this is approximately 17°, in Michigan approximately 1°. Once again, this cannot be accomplished by a magnetic compass, and would have been impossible to accomplish without an E^2 memory device.

Electronic Compass Block Diagram



TL/D/8613–1

Automatic Low Cost Thermostat

National Semiconductor
Application Brief 22
Kent Brooten

Ths application brief describes the use of the NMC9346 (64 x 16) serial EEPROM. With the advent of the inexpensive COPS™ family from National Semiconductor, heretofore "expensive" applications can now be realized inexpensively. Such an application is a low cost thermostat. Typical features of such a device are:

1) Ability to interface to local and remote temperature sensors,

2) Ability to hold changeable settings,

3) Digital display of present temperature,

4) Inexpensive in high volume.

CIRCUIT DESCRIPTION

The basis of the thermostat is the COP410 microcontroller. This, with the addition of 2 ADC0854 A/D converters, an NMC9346 EEPROM and some logic for LED display, comprise an extremely versatile, yet low cost, system. The ADC0854 allows 4 channels of temperature sensors, 1 local and 3 remote. Temperature sensors used are LM34 (for readings in °F) or LM35 (for readings in °C).

While there are several possible choices for A/D converters that are MICROWIRE™ compatible, the ADC0854 was chosen because of its "settability". By presetting the "cold" temperature (i.e., when the cooling unit should come on—say 80°F) all the microcomputer has to do is to multiplex the inputs and read the data in line. Similarly, the "hot" A/D can be preset to the temperature where the furnace should come on (e.g., 60°F) and scanned in a like manner. Since the microcomputer is also keeping time of day, selecting an A/D with more "smarts" (as in the ADC0854) the software can be kept manageable and an external real time clock chip is not needed.

The EEPROM (NMC9346) holds the presettable temperature ranges (high and low settings) by day of the week. Since data is in EEPROM rather than in mask ROM, it can be changed.

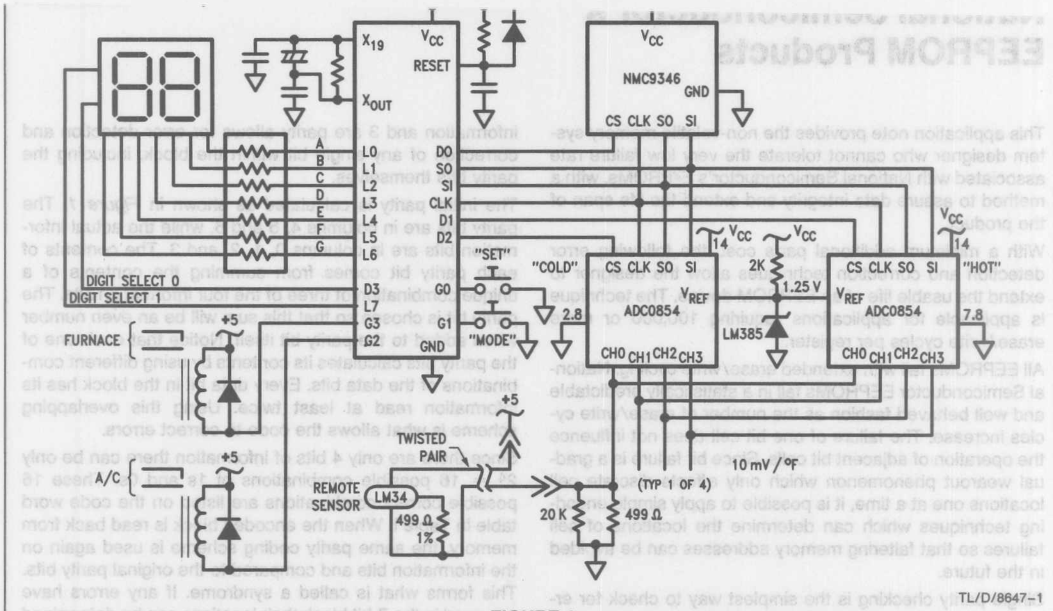
The LED display is multiplexed by the microcomputer. Depending on the type of display selected, external drivers may be necessary.

Input power is typically 24 VAC. Using a linear regulator would cause too much heat to be dissipated, which would upset the local temperature sensors. Thus, a switch mode regulator must be used. Fortunately, National Semiconductor has provided a solution to the problem with the LM3578, a switching regulator in an 8-pin mini-DIP, providing more than enough current for the application, using only a minimum of external components.

SOFTWARE DESCRIPTION

Since a real time clock is implemented in software, all routines must execute the same number of cycles independent of the input. Because of the flexibility of the COPS family instruction set, this is not as difficult a problem as it first appears. Since the EEPROM contains the settings that are periodically sent to the A/D converters, the COPS program merely fetches data from one source and dumps it to another while monitoring the output. Even the SET and MODE keys can be acted upon in a predictable manner IF the software designer carefully plans the program flow BEFORE writing code.

Note: Also see App Brief 15.



NMC9346
VCC
GND
CS CLK SO SI
X19
VCC
RESET
XOUT
A
B
C
D
E
F
G
L0
L1
L2
L3
L4
L5
L6
DO
SO
SI
CLK
D1
D2
DIGIT SELECT 0
DIGIT SELECT 1
D3
L7
G3
G2
G0
G1
GND
"SET"
"MODE"
FURNACE
+5
A/C
"COLD"
"HOT"
ADC0854
VREF
CH0 CH1 CH2 CH3
2.8
7.8
2K
1.25 V
LM385
14
TWISTED PAIR
REMOTE SENSOR
LM34
499 Ω 1%
10 mV / °F
(TYP 1 OF 4)
20 K
499 Ω
TL/D/8647–1

FIGURE 1

Error Detection and Correction Techniques for National Semiconductor's EEPROM Products

National Semiconductor
Application Note 482

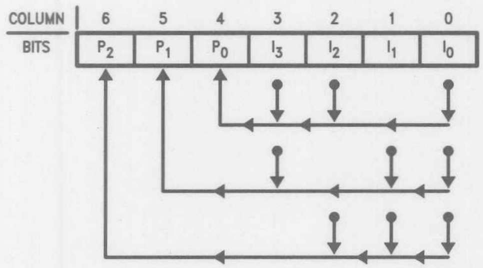
This application note provides the non-volatile memory system designer who cannot tolerate the very low failure rate associated with National Semiconductor's E^2PROMs, with a method to assure data integrity and extend the life span of the product.

With a minimum additional parts cost, the following error detection and correction techniques allow the designer to extend the usable life of an EEPROM device. The technique is applicable for applications requiring 100,000 or more erase/write cycles per register.

All EEPROMs fail with extended erase/write cycling. National Semiconductor EEPROMs fail in a statistically predictable and well behaved fashion as the number of erase/write cycles increase. The failure of one bit cell does not influence the operation of adjacent bit cells. Since bit failure is a gradual wearout phenomenon which only affects discrete cell locations one at a time, it is possible to apply simple encoding techniques which can determine the locations of cell failures so that faltering memory addresses can be avoided in the future.

Single parity checking is the simplest way to check for errors in a binary code. In a parity checking system an extra-parity-bit is chosen so that the number of 1s in the block of data, including the parity bit, is even. In practice this is accomplished using modulo 2 addition (i.e., $0 + 0 = 0$; $0 + 1 = 1$; $1 + 0 = 1$; $1 + 1 = 0$; $0 + 0 + 1 = 1$; etc.). Modulo 2 addition is quickly accomplished through an exclusive OR gate. When the data is read back, the number of ones are counted and the sum is checked to see if it is odd or even. An odd sum is an indication that an error occurred in the data. This method of single parity checking can detect the occurrence of an error in a block but it cannot be used to determine the exact location of the error to correct the bad data.

A natural extension of single parity checking is the Hamming code. A Hamming code uses several parity checks, instead of just one. This allows errors to be corrected as well as detected. Using bits in blocks of 7, where 4 of the bits are



TL/D/9214-1

FIGURE 1. Computation Scheme for Parity Bits Using Hamming Code

information and 3 are parity allows for error detection and correction of any single bit within the block, including the parity bits themselves.

The initial parity is calculated as shown in *Figure 1*. The parity bits are in columns 4, 5 and 6, while the actual information bits are in columns 0, 1, 2, and 3. The contents of each parity bit comes from summing the contents of a unique combination of three of the four information bits. The parity bit is chosen so that this sum will be an even number when added to the parity bit itself. Notice that each one of the parity bits calculates its contents by using different combinations of the data bits. Every data bit in the block has its information read at least twice. Using this overlapping scheme is what allows the code to correct errors.

Since there are only 4 bits of information there can be only $2^4 = 16$ possible combinations of 1s and 0s. These 16 possible correct combinations are listed on the code word table in Table I. When the encoded block is read back from memory, the same parity coding scheme is used again on the information bits and compared to the original parity bits. This forms what is called a syndrome. If any errors have occurred in the 7-bit block their locations can be determined and the errors corrected. Table II shows the decoding matrix which is used on the syndromes to determine the location of an error. If no errors occurred the syndrome will be 000. Table III shows all the combinations of the 7-bit block. Note that there are only 128 possible variations of 1s and 0s in the block: (7 mistake combinations per block + 1 correct combination per block) $\times$ (16 possible block combinations). All these combinations can be stored in a table and called up quickly to check for possible data errors without the need to even create a syndrome upon reading a word. For example, suppose we want to store the data 1000. From Table I we see that the 7-bit block would be 1111000 after the Hamming code had been applied. If information bit 3 for example goes bad, then the new block would read 1110000. This is case number 112 in Table III, and we see that the correct information is 1000. With Table III available in the computer memory, the received codeword can be corrected automatically. An array of 128 bytes can provide both the corrected information and the syndrome information.

The 7-bit codeword works nicely with National Semiconductor's serial EEPROMs because they are organized as arrays of 16-bit registers. Each 16 bit register is modified or accessed with a simple-serial protocol. The 16-bit unit can be partitioned two eight-bit bytes. Each byte can contain a seven-bit codeword and one-bit flag that indicates whether an error has been previously detected in the byte. This scheme provides one byte of error corrected information per 16-bit register. Slightly more elaborate systems can be used which will detect and correct more errors if additional parity bits are added to the data.

TABLE I. Encoding Table for Hamming Code

	Sixteen Code Words						
	Parity Bits			Information Bits			
	P 2	P 1	P 0	I 3	I 2	I 1	I 0
0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	1
2	1	0	1	0	0	1	0
3	0	1	1	0	0	1	1
4	0	1	1	0	1	0	0
5	1	0	1	0	1	0	1
6	1	1	0	0	1	1	0
7	0	0	0	0	1	1	1
8	1	1	1	1	0	0	0
9	0	0	1	1	0	0	1
10	0	1	0	1	0	1	0
11	1	0	0	1	0	1	1
12	1	0	0	1	1	0	0
13	0	1	0	1	1	0	1
14	0	0	1	1	1	1	0
15	1	1	1	1	1	1	1

TABLE II. Syndrome Decoding Table for Hamming Code

Syndrome			Meaning
0	0	0	No error detected
0	0	1	Check bit 0 in error
0	1	0	Check bit 1 in error
0	1	1	Information bit 2 corrected
1	0	0	Check bit 2 in error
1	0	1	Information bit 1 corrected
1	1	0	Information bit 0 corrected
1	1	1	Information bit 3 corrected

With this added data protection the reliability of EEPROMs can be extended because the probability of two or more cells failing on the same codeword is low. To illustrate the Hamming code, an experiment on 16 devices with 1k bits each was conducted. The experiment results are shown in Table IV. While the first bit failure was detected somewhere between 12,589 and 15,849 cycles, the Hamming code just described would have protected against the loss of data until somewhere between 79,433 and 100,000 erase/write cycles. Notice that 55 bit failures were indicated when the first Hamming code failure was detected. This is to be expected because a Hamming failure will not occur until two or more bits within a particular group of seven bits have failed.

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code

	Received Codeword							Syndrome Bits			Corrected Information			
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1	1	1	0	0	0	0	0
2	0	0	0	0	0	1	0	1	0	1	0	0	0	0
3	0	0	0	0	0	1	1	0	1	1	0	1	1	1
4	0	0	0	0	1	0	0	0	1	1	0	0	0	0
5	0	0	0	0	1	0	1	1	0	1	0	1	1	1
6	0	0	0	0	1	1	0	1	1	0	0	1	1	1
7	0	0	0	0	1	1	1	0	0	0	0	1	1	1
8	0	0	0	1	0	0	0	1	1	1	0	0	0	0
9	0	0	0	1	0	0	1	0	0	1	1	0	0	1
10	0	0	0	1	0	1	0	0	1	0	1	0	1	0
11	0	0	0	1	0	1	1	1	0	0	1	0	1	1
12	0	0	0	1	1	0	0	1	0	0	1	1	0	0
13	0	0	0	1	1	0	1	0	1	0	1	1	0	1
14	0	0	0	1	1	1	0	0	0	1	1	1	1	0
15	0	0	0	1	1	1	1	1	1	1	0	1	1	1
16	0	0	1	0	0	0	0	0	0	1	0	0	0	0
17	0	0	1	0	0	0	1	1	1	1	1	0	0	1
18	0	0	1	0	0	1	0	1	0	0	0	0	1	0
19	0	0	1	0	0	1	1	0	1	0	0	0	1	1
20	0	0	1	0	1	0	0	0	1	0	0	1	0	0
21	0	0	1	0	1	0	1	1	0	0	0	1	0	1
22	0	0	1	0	1	1	0	1	1	1	1	1	1	0
23	0	0	1	0	1	1	1	0	0	1	0	1	1	1
24	0	0	1	1	0	0	0	1	1	0	1	0	0	1
25	0	0	1	1	0	0	1	0	0	0	1	0	0	1
26	0	0	1	1	0	1	0	0	1	1	1	1	1	0
27	0	0	1	1	0	1	1	1	0	1	1	0	0	1
28	0	0	1	1	1	0	0	1	0	1	1	1	1	0
29	0	0	1	1	1	0	1	0	1	1	1	0	0	1
30	0	0	1	1	1	1	0	0	0	0	1	1	1	0
31	0	0	1	1	1	1	1	1	1	0	1	1	1	0

32	0	1	0	0	0	0	0	0	1	0	0	0	0	0
33	0	1	0	0	0	0	1	1	0	0	0	0	0	1
34	0	1	0	0	0	1	0	1	1	1	1	0	1	0
35	0	1	0	0	0	1	1	0	0	1	0	0	1	1
36	0	1	0	0	1	0	0	0	0	1	0	1	0	0
37	0	1	0	0	1	0	1.	1	1	1	1	1	0	1
38	0	1	0	0	1	1	0	1	0	0	0	1	1	0
39	0	1	0	0	1	1	1	0	1	0	0	1	1	1
40	0	1	0	1	0	0	0	1	0	1	1	0	1	0
41	0	1	0	1	0	0	1	0	1	1	1	1	0	1
42	0	1	0	1	0	1	0	0	0	0	1	0	1	0
43	0	1	0	1	0	1	1	1	1	0	1	0	1	0
44	0	1	0	1	1	0	0	1	1	0	1	1	0	1
45	0	1	0	1	1	0	1	0	0	0	1	1	0	1
46	0	1	0	1	1	1	0	0	1	1	1	0	1	0
47	0	1	0	1	1	1	1	1	0	1	1	1	0	1
48	0	1	1	0	0	0	0	0	1	1	0	1	0	0
49	0	1	1	0	0	0	1	1	0	1	0	0	1	1
50	0	1	1	0	0	1	0	1	1	0	0	0	1	1
51	0	1	1	0	0	1	1	0	0	0	0	0	1	1
52	0	1	1	0	1	0	0	0	0	0	0	1	0	0
53	0	1	1	0	1	0	1	1	1	0	0	1	0	0
54	0	1	1	0	1	1	0	1	0	1	0	1	0	0
55	0	1	1	0	1	1	1	0	1	1	0	0	1	1
56	0	1	1	1	0	0	0	1	0	0	1	0	0	0
57	0	1	1	1	0	0	1	0	1	0	1	0	0	1
58	0	1	1	1	0	1	0	0	0	1	1	0	1	0
59	0	1	1	1	0	1	1	1	1	1	0	0	1	1
60	0	1	1	1	1	0	0	1	1	1	0	1	0	0
61	0	1	1	1	1	0	1	0	0	1	1	1	0	1
62	0	1	1	1	1	1	0	0	1	0	1	1	1	0
63	0	1	1	1	1	1	1	1	0	0	1	1	1	1
64	1	0	0	0	0	0	0	1	0	0	0	0	0	0
65	1	0	0	0	0	0	1	0	1	0	0	0	0	1
66	1	0	0	0	0	1	0	0	0	1	0	0	1	0
67	1	0	0	0	0	1	1	1	1	1	1	0	1	1
68	1	0	0	0	1	0	0	1	1	1	1	1	0	0
69	1	0	0	0	1	0	1	0	0	1	0	1	0	1
70	1	0	0	0	1	1	0	0	1	0	0	1	1	0
71	1	0	0	0	1	1	1	1	0	0	0	1	1	1
72	1	0	0	1	0	0	0	0	1	1	1	1	0	0
73	1	0	0	1	0	0	1	1	0	1	1	0	1	1
74	1	0	0	1	0	1	0	1	1	0	1	0	1	1
75	1	0	0	1	0	1	1	1	0	0	1	0	1	1
76	1	0	0	1	1	0	0	0	0	0	1	1	0	0
77	1	0	0	1	1	0	1	1	1	0	1	1	0	0
78	1	0	0	1	1	1	0	1	0	1	1	1	0	0
79	1	0	0	1	1	1	1	0	1	1	1	0	1	1

TABLE III. Information Retrieval Table for All Possible Combinations of Single-Bit-Correct Hamming Code (Continued)

	Received Codeword							**Syndrome Bits**			**Corrected Information**			
80	1	0	1	0	0	0	0	1	0	1	0	0	1	0
81	1	0	1	0	0	0	1	0	1	1	0	1	0	1
82	1	0	1	0	0	1	0	0	0	0	0	0	1	0
83	1	0	1	0	0	1	1	1	1	0	0	0	1	0
84	1	0	1	0	1	0	0	1	1	0	0	1	0	1
85	1	0	1	0	1	0	1	0	0	0	0	1	0	1
86	1	0	1	0	1	1	0	0	1	1	0	0	1	0
87	1	0	1	0	1	1	1	1	0	1	0	1	0	1
88	1	0	1	1	0	0	0	0	1	0	1	0	0	0
89	1	0	1	1	0	0	1	1	0	0	1	0	0	1
90	1	0	1	1	0	1	0	1	1	1	0	0	1	0
91	1	0	1	1	0	1	1	0	0	1	1	0	1	1
92	1	0	1	1	1	0	0	0	0	1	1	1	0	0
93	1	0	1	1	1	0	1	1	1	1	0	1	0	1
94	1	0	1	1	1	1	0	1	0	0	1	1	1	0
95	1	0	1	1	1	1	1	0	1	0	1	1	1	1
96	1	1	0	0	0	0	0	1	1	0	0	0	0	1
97	1	1	0	0	0	0	1	0	0	0	0	0	0	1
98	1	1	0	0	0	1	0	0	1	1	0	1	1	0
99	1	1	0	0	0	1	1	1	0	1	0	0	0	1
100	1	1	0	0	1	0	0	1	0	1	0	1	1	0
101	1	1	0	0	1	0	1	0	1	1	0	0	0	1
102	1	1	0	0	1	1	0	0	0	0	0	1	1	0
103	1	1	0	0	1	1	1	1	1	0	0	1	1	0
104	1	1	0	1	0	0	0	0	0	1	1	0	0	0
105	1	1	0	1	0	0	1	1	1	1	0	0	0	1
106	1	1	0	1	0	1	0	1	0	0	1	0	1	0
107	1	1	0	1	0	1	1	0	1	0	1	0	1	1
108	1	1	0	1	1	0	0	0	1	0	1	1	0	0
109	1	1	0	1	1	0	1	1	0	0	1	1	0	1
110	1	1	0	1	1	1	0	1	1	1	0	1	1	0
111	1	1	0	1	1	1	1	0	0	1	1	1	1	1
112	1	1	1	0	0	0	0	1	1	1	1	0	0	0
113	1	1	1	0	0	0	1	0	0	1	0	0	0	1
114	1	1	1	0	0	1	0	0	1	0	0	0	1	0
115	1	1	1	0	0	1	1	1	0	0	0	0	1	1
116	1	1	1	0	1	0	0	1	0	0	0	1	0	0
117	1	1	1	0	1	0	1	0	1	0	0	1	0	1
118	1	1	1	0	1	1	0	0	0	1	0	1	1	0
119	1	1	1	0	1	1	1	1	1	1	1	1	1	1
120	1	1	1	1	0	0	0	0	0	0	1	0	0	0
121	1	1	1	1	0	0	1	1	1	0	1	0	0	0
122	1	1	1	1	0	1	0	1	0	1	1	0	0	0
123	1	1	1	1	0	1	1	0	1	1	1	1	1	1
124	1	1	1	1	1	0	0	0	1	1	1	0	0	0
125	1	1	1	1	1	0	1	1	0	1	1	1	1	1
126	1	1	1	1	1	1	0	1	1	0	1	1	1	1
127	1	1	1	1	1	1	1	0	0	0	1	1	1	1

TABLE IV. Hamming Code Experimental Demonstration on 16 Devices of 1k Bits Each

Erase/Write Cycles	Total Bit Failures	Total Codeword Failures	Percent Bit Failures	Percent Codeword Failures
1000	0	0	0.00%	0.00%
1259	0	0	0.00%	0.00%
1585	0	0	0.00%	0.00%
1995	0	0	0.00%	0.00%
2512	0	0	0.00%	0.00%
3162	0	0	0.00%	0.00%
3981	0	0	0.00%	0.00%
5012	0	0	0.00%	0.00%
6310	0	0	0.00%	0.00%
7943	0	0	0.00%	0.00%
10000	0	0	0.00%	0.00%
12589	1	0	0.01%	0.00%
15849	1	0	0.01%	0.00%
19953	1	0	0.01%	0.00%
25119	1	0	0.01%	0.00%
31623	3	0	0.02%	0.00%
39811	4	0	0.02%	0.00%
50119	10	0	0.06%	0.00%
63096	16	0	0.10%	0.00%
79433	55	1	0.34%	0.05%
100000	103	3	0.63%	0.15%

Question: What has 8 pins, runs on 5V and can store any one of more than 10^{300} unique bit patterns?

Answer: The NM93C46—a 1024-bit serial EEPROM.

Surprised? It is easy to check:

2^{1024} = number of possible combinations

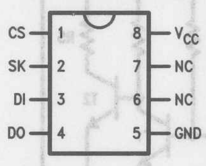
$2^{10} = 10^3$

$2^{1024} \cong (2^{10})^{102} = (10^3)^{102} = 10^{306}$

10^{306} combinations are more than enough for any conceivable security application, serial number, or station I.D. many times over. Although the NM93C46 is a small part both physically and in memory size, its capacity to store unique codes is boundless.

Figure 1 shows the pin assignments and pin names for the NM93C46. Pins 6 and 7 are not connected, leaving only 6 active pins on the device. The DO pin is not active while data is being loaded through the DI pin. DI and DO can be tied together, creating a device that requires a 5-wire interface. This interface may be useful in security applications. The EEPROM could be built into a module that could be used as a "smart key" in electronic security systems. The key would be read whenever it was inserted into a 5-contact keyhole and access would be granted or denied as determined by the stored code. If only 256 bits of the EEPROM were to be used to store the code, this would still provide 10^{77} possible combinations. The remainder of the memory in the key could be used for data collection or to keep a record of where the key had been. It should be noted that ability to write data into the key allows the key to be immediately erased if it is misused.

Dual-In-Line Package



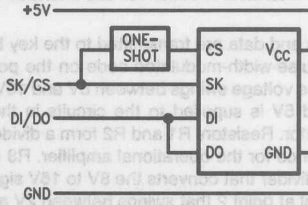
TL/D/8611-1

Pin Names

CS	Chip Select
SK	Serial Clock
DI	Data Input
DO	Data Output
V_{CC}	+5V
GND	Ground
NC	No Connection

FIGURE 1

The 5-contact key is nice, but a 4-contact key is at least 20% better. *Figure 2* shows how the addition of a retriggerable one-shot can achieve this reduction. This circuit puts some timing constraints on the serial clock signal, but these are easily met. The output pulse of the one-shot should remain high for a period that is slightly longer than one serial clock cycle to prevent the NM93C46 from being reset. (The falling edge of CS must occur before the rising edge of the serial clock after the last bit of a write command is transmitted.)

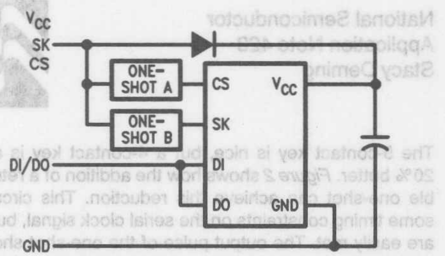


TL/D/8611-2

One-shot is retriggerable MM74HC123

FIGURE 2

A circuit for a 3-contact key is shown in *Figure 3*. A filter capacitor, diode and one-shot have been added. Both one-shots are triggered whenever a pulse to ground occurs on the power supply contact. The capacitor and diode provide power to the NM93C46 and the one-shots during this brief power interruption. An operational amplifier can be used as the power source and can easily generate the required waveform. Both the serial clock and chip select signals are recovered from this waveform.



TL/D/8611–3

One-Shot A—½ MM74HC123

One-Shot B—½ MM74HC123

FIGURE 3

By adding more circuitry to the key, it is possible to achieve a 2-contact interface. A circuit for this interface is shown in *Figure 4*.

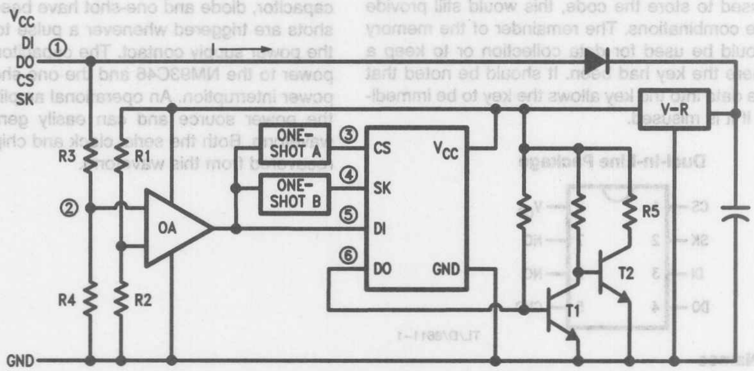
Commands and data are transmitted to the key by superimposing a pulse-width-modulated code on the power supply contact. The voltage swings between 8V and 16V at point 1. A regulated 5V is supplied to the circuits in the key by a local regulator. Resistors R1 and R2 form a divider to create a 3V reference for the operational amplifier. R3 and R4 are used as a divider that converts the 8V to 16V signal at point 1 to a signal at point 2 that swings between 2V and 4V. The output of the operational amplifier now follows the signal at point 1 but swings from 0V to 5V. This signal is used to trigger the one-shots as in the 3-contact circuit, and appears at the DI pin as a pulse-width-modulated signal. Command and data signals may now be entered. Data is read from the key by monitoring the power supply current. When the DO pin is in TRI-STATE® or outputs a one, transistor T2 is turned off. When DO outputs a zero, T2 is turned on and current flows through R5. The value of R5 may be chosen to create whatever current change is needed to detect the state of DO. The current should be tested when the voltage at point 1 is 16V. The resistor in this example will produce a 10 mA change.

Figure 5 shows a typical read sequence for the circuit shown in *Figure 4*.

CONCLUSION

This application note describes a number of circuits that are useful in security and data collection systems. These circuits should be considered only the beginning. It no longer makes sense to install DIP switches to select access codes in garage door openers, cordless and mobile phones, or any other microcontroller-based system. "Smart keys" can be used to gain access to databases and can be invalidated over normal communication lines if they are abused. It boggles the mind to consider what can be done with so many unique codes.

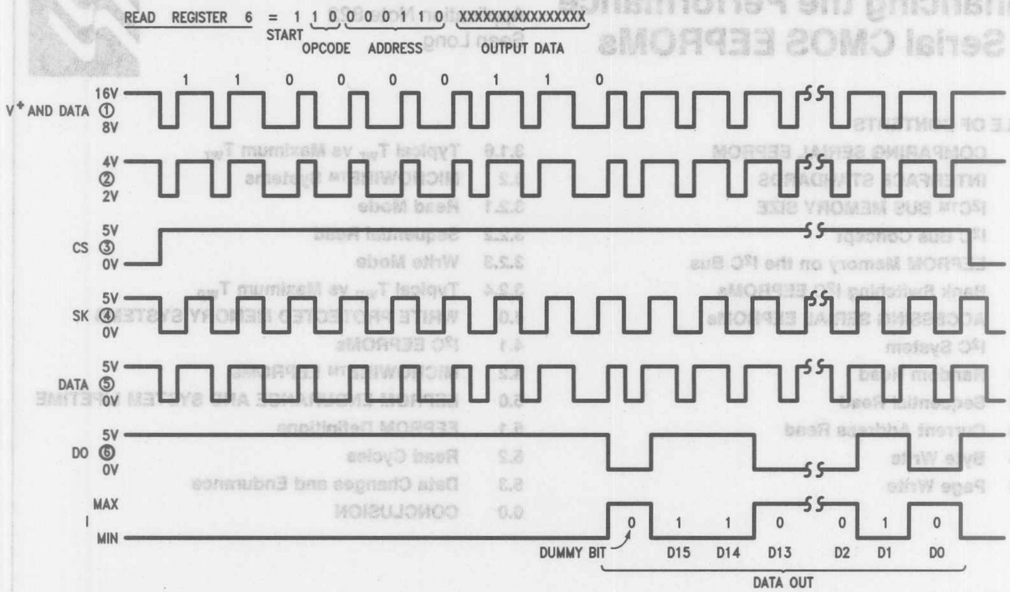
Note: The circuits in this application note feature the NM93C46. The NM93C06 is a pin-compatible part that stores 256 bits.



TL/D/8611–4

R1 = 20K
R2 = 30K
R3 = 15K
R4 = 5K
One-Shot A = ½ MM74HC123
One-Shot B = ½ MM74HC123
V-R = LM2930Z-5.0
OA = LM358
R5 = 1600Ω

FIGURE 4



TL/D/8611-5

FIGURE 5

4

Enhancing the Performance of Serial CMOS EEPROMs

National Semiconductor
Application Note 822
Sean Long

TABLE OF CONTENTS

INTRODUCTION

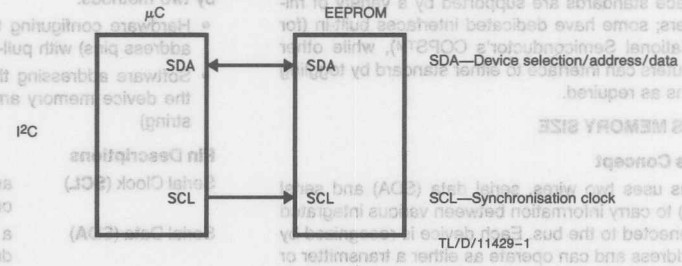
This application note presents a number of solutions to help a system designer overcome some possible limitations of serial Electrically Erasable PROMs (EEPROMs) to obtain greater system performance and flexibility.

This note assumes that the reader is familiar with National Semiconductor's range of MICROWIRE EEPROMs (NM93Cxx and NM93CSxx) and I^{2}C (NM24Cxx) devices.

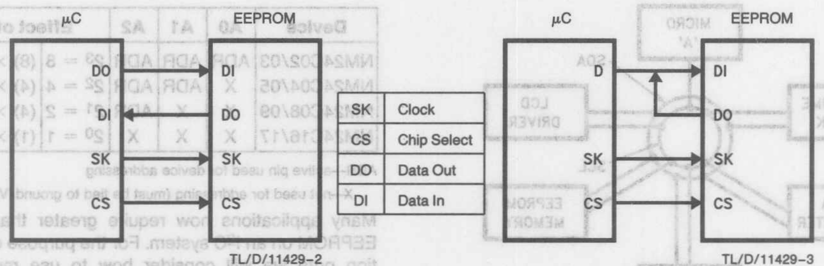
1.0 COMPARING SERIAL EEPROM INTERFACE STANDARDS

The two industry standard serial interfaces for EEPROMs are the MICROWIRE and I^{2}C-bus specifications. The key features of these two interfaces are shown in *Figure 1.*

Serial Interface Standards



MICROWIRE



4 Wire **3 Wire**

	MICROWIRE	I^{2}C
Max Bus Speed	1 MHz	100 kHz
Number of Active Pins	4	2
Maximum Memory	N/A	16 kbit
Acknowledge	No	Yes
Data Size	8- or 16-Bit	8-Bit
Block Write	No	Yes
Sequential Read	Yes	Yes
Number of Devices on Bus	Limited by Port Pins	32 Functions, 256 Total Devices

FIGURE 1. MICROWIRE vs I^{2}C

The key advantages of the MICROWIRE interface compared to the I²C-bus are:

- Higher system speed (1 MHz vs 100 kHz)
- Greater memory size (unlimited vs 16 kbit maximum)
- Address programming pins are not required on peripherals

The key advantages of the I²C-bus are:

- Only requires 2 pins (SDA and SCL)
- Allows easy implementation of a multi-master system

Both interface standards are supported by a variety of microcomputers; some have dedicated interfaces built-in (for example National Semiconductor's COPS™), while other microcomputers can interface to either standard by toggling I/O port pins as required.

2.0 I²C-BUS MEMORY SIZE

2.1 I²C-Bus Concept

The I²C-bus uses two wires, serial data (SDA) and serial clock (SCL) to carry information between various integrated circuits connected to the bus. Each device is recognized by a unique address and can operate as either a transmitter or receiver depending on the function of the individual device. A typical I²C-bus system is shown in *Figure 2*.

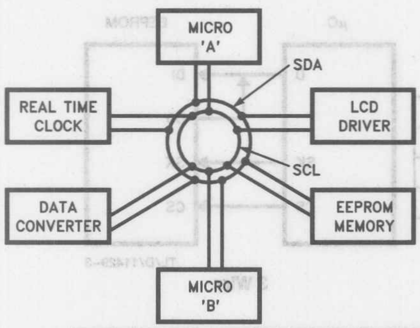


FIGURE 2. A Typical I²C-Bus System

In addition to transmitters and receivers, devices can also be defined as masters or slaves when performing data transfers.

A master is: — the device which initiates data transfer
— generates clock signals
— terminates a data transfer
— e.g., a microcomputer

A slave is: — the device addressed by a master
— e.g., a memory

Note: The I²C-bus is a multi-master bus; each master generates its own clock signals when transferring data on the bus.

2.2 EEPROM Memory on the I²C-Bus

The I²C-bus specification allows a maximum of 16 kbits of EEPROM. The 4-bit device type identifier string which follows the START condition is 1010 for EEPROMs. National Semiconductor manufactures a range of different size I²C EEPROMs (2k, 4k, 8k, and 16 kbits) to allow a system designer to select the amount of memory required.

EEPROMs on the I²C-bus may be configured in any manner required, providing the total memory addressed does not exceed 16 kbits. EEPROM memory Addressing is controlled by two methods:

- Hardware configuring the A0, A1, and A2 pins (device address pins) with pull-up or pull-down resistors
- Software addressing the required PAGE BLOCK within the device memory array (as sent in the slave address string)

Pin Descriptions

Serial Clock (**SCL**)	an input used to clock data into and out of the memory
Serial Data (**SDA**)	a bidirectional pin used to transfer data into and out of the device
Device Address Inputs	connected to V_{CC} or V_{SS} to configure EEPROM address

Device	A0	A1	A2	Effect of Address	
NM24C02/03	ADR	ADR	ADR	$2^3 = 8$	(8) × (2k) = 16k
NM24C04/05	X	ADR	ADR	$2^2 = 4$	(4) × (4k) = 16k
NM24C08/09	X	X	ADR	$2^1 = 2$	(4) × (8k) = 16k
NM24C16/17	X	X	X	$2^0 = 1$	(1) × (16k) = 16k

ADR—active pin used for device addressing

X—not used for addressing (must be tied to ground/V_{SS})

Many applications now require greater than 16 kbits of EEPROM on an I²C system. For the purpose of this application note we will consider how to use multiple 16 kbit (NM24C16/17) devices in an I²C bus system to increase the total memory size.

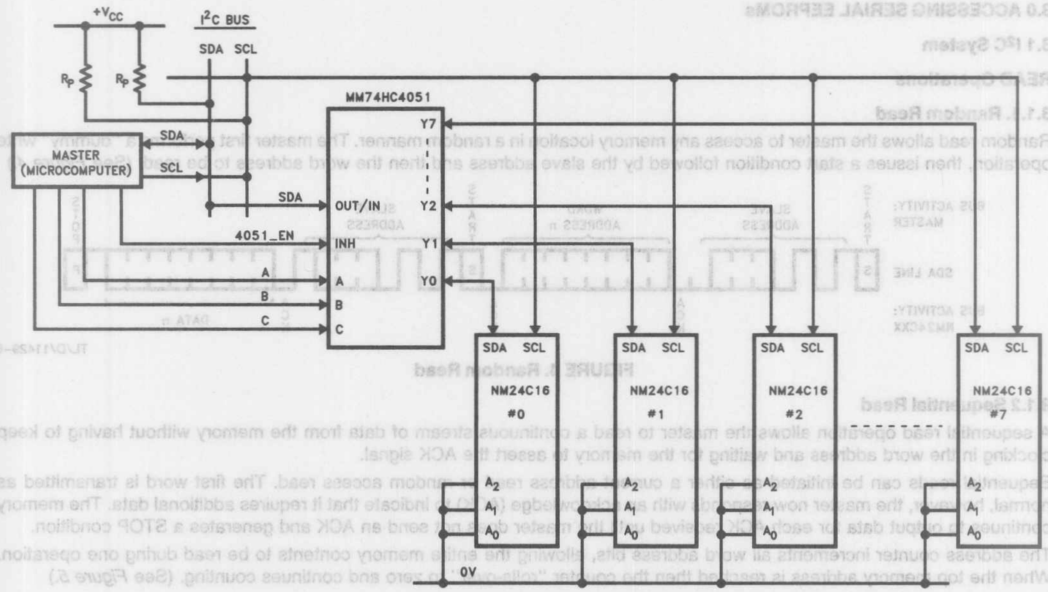


FIGURE 3. Increasing I²C-Bus EEPROM → 16 kbits

2.3 Bank Switching I²C EEPROMs

A circuit to increase the EEPROM memory size of the I²C bus, while still maintaining full software and hardware compatibility, is shown in *Figure 3*.

The circuit connects the serial clock (SCL) to each memory device, but the serial data (SDA) is connected by a multiplexed, bidirectional analog switch (MM74HC4051). The MM74HC4051 is an 8-channel analog multiplexer which connects together the outputs of 8 digitally controlled analog switches, thus achieving an 8-channel multiplexer. These switches are bidirectional, allowing any analog input to be used as an output and vice-versa. They have a low "on" resistance, typically 50Ω or less.

The MM74HC4051 is controlled by four inputs; INH which enables the switches to be "on" and inputs A, B and C which select one of the eight switches. The master (microcontroller) generates these four control signals to the MM74HC4051 directly.

In this case a typical software flow would be:

— set microcontroller port pins to select the NM24C16/17 required

— [DEVICE TYPE] → [DEVICE ADDRESS] → [PAGE BLOCK ADDRESS] → [BYTE ADDRESS]

This means that this low cost solution still maintains full I²C-bus compatibility.

Worst Case Analysis

I²C-Bus Specification	MM74HC4051 Solution Specification
C_{max} = 400 pF (Note 1) f_{max} = 100 kHz (Note 2) = 10 µs Period I_{OL} max = 3 mA	C_{IN} = 90 pF max t_{PD} = 15 ns max = 5 ns typical R_{ON} max = 140Ω

Note 1: The maximum number of devices connected to the I²C-bus is controlled by the maximum allowable capacitance which is 400 pF per line.

Note 2: The maximum I_2C system clock is 100 kHz. The propagation delay through the MM74HC4051 is small enough to ensure that data set-up time of 250 ns min is not violated.

3.1.1. Random Read

Random read allows the master to access any memory location in a random manner. The master first performs a "dummy" write operation, then issues a start condition followed by the slave address and then the word address to be read. (See *Figure 4*.)

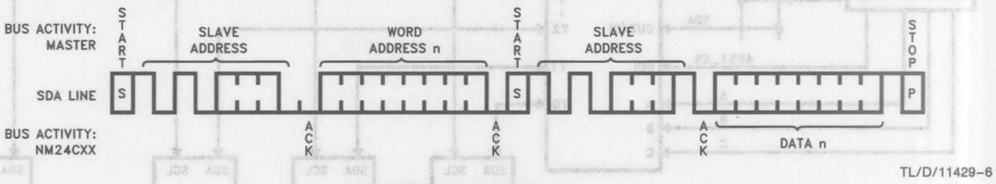


FIGURE 4. Random Read

3.1.2 Sequential Read

A sequential read operation allows the master to read a continuous stream of data from the memory without having to keep clocking in the word address and waiting for the memory to assert the ACK signal.

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as normal, however, the master now responds with an acknowledge (ACK) to indicate that it requires additional data. The memory continues to output data for each ACK received until the master does not send an ACK and generates a STOP condition.

The address counter increments all word address bits, allowing the entire memory contents to be read during one operation. When the top memory address is reached then the counter "rolls-over" to zero and continues counting. (See *Figure 5*.)

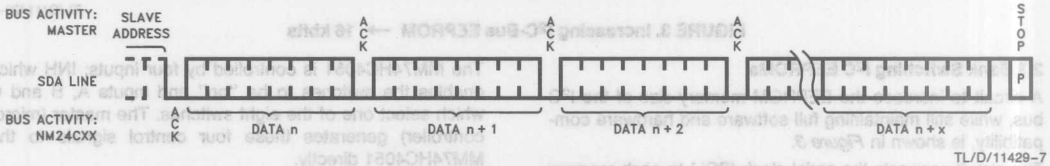


FIGURE 5. Sequential Read

3.1.3. Current Address Read

Internally the NM24Cxx devices contain an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address *n*, the next read operation would access data from address $n + 1$, without the need for the master to transmit the 8-bit word address and then wait for the NM24Cxx acknowledge signal before transmitting the data. (See *Figure 6*.)

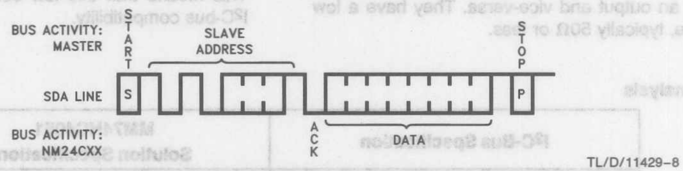


FIGURE 6. Current Address Read

Write Operations

3.1.4 Byte Write

The normal write sequence is shown in *Figure 7*.

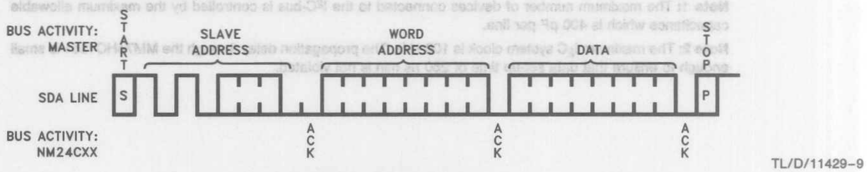


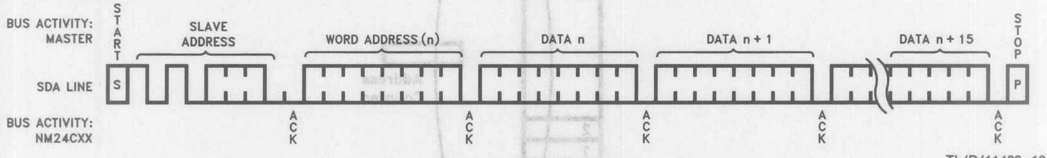
FIGURE 7. Byte Write

The master clocks the data into the NM24Cxx, and upon receipt of the ACK generates a STOP condition, at which time the NM24Cxx begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the NM24Cxx inputs are disabled, and the device will not respond to any requests from the master.

All NM24Cxx EEPROMs have a Write cycle time of $T_{wr} = 10$ ms MAXIMUM for 5V systems.

cycle in the usual way when an internal write cycle occurs in the memory.

This method results in a single T_{wr} delay instead of sixteen. This is useful for applications such as saving data after detecting a power failure when speed of writing is critical.



TL/D/11429–10

FIGURE 8. Page Write

3.1.6 Typical T_{wr} vs Maximum T_{wr}

Good design practice recommends using "worst-case" timing calculations rather than typical figures. After a master had initiated an internal write cycle in the memory there are two options before the next cycle can begin:

1. Master waits T_{wr} MAX = 10 ms

   — this ensures that all "worst-case" write cycles will be finished

   or

2. Master "polls" memory to detemine if the write cycle is complete T_{wr} TYP = 5 ms

With option 2 the master can start polling immediately after starting the internal memory write cycle as follows:

[STOP] ⟶ [START] ⟶ [SLAVE ADDRESS FOR WRITE OPERATION] ⟶ [POLL ACK]

IF no ACK then NM24Cxx still BUSY doing internal write
else NM24Cxx completed write cycle
master can proceed with next read or write operation.

This method can make significant improvements to overall system performance.

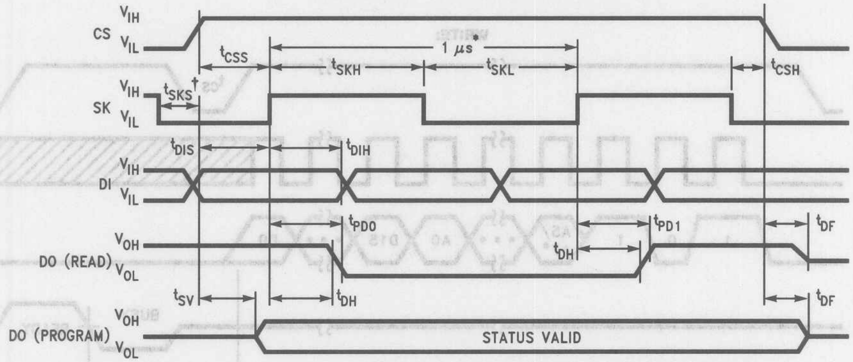
Note: After receiving a no acknowledge the master should output a stop condition to free the I²C-bus for other operations.

3.2 MICROWIRE Systems

3.2.1 Read Mode

A typical Read access is shown in *Figure 9*. The rising edge of CS is used to select and reset the EEPROM. Then the microcomputer clocks in the start bit and opcode for a read cycle using serial clock (SK) and Data In (DI pins). This is followed by the address where data is to be read from, after which the data is output via Data Out (DO) pin.

SYNCHRONOUS DATA TIMING



TL/D/11429–11

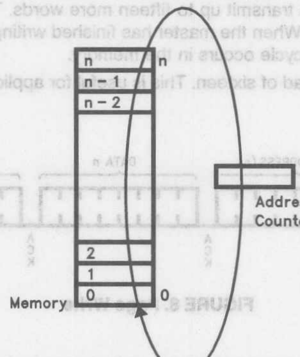
— Chip Select (CS) used to differentiate between various devices on bus.
— Rising edge of CS resets internal circuitry of EEPROM.
— Low-to-High transition of shift clock (SK) shifts all data in and out.
— CS brought low before next rising edge of SK to initiate self-timed programming cycle.

FIGURE 9. Read Mode

4

3.2.2. Sequential Read

All National's NM93CSxx devices support sequential read allowing the complete memory array to be read in a single operation.



TL/D/11429–12

CMOS: Sequential Read

Allows the user to obtain an endless loop of data simply by entering the read mode.

→ Reduces overhead

→ 50% faster read

Note: The NM93Cxx devices do NOT support sequential read.

FIGURE 10. Sequential Read

3.2.3 Write Mode

A write cycle is entered in a similar way to a read cycle; first the start bit and opcode for a write cycle are clocked in via DI, followed by the address and data to be written. The self timed programming cycle is initiated by bringing CS low before the next rising edge of SK as shown in *Figure 11*.

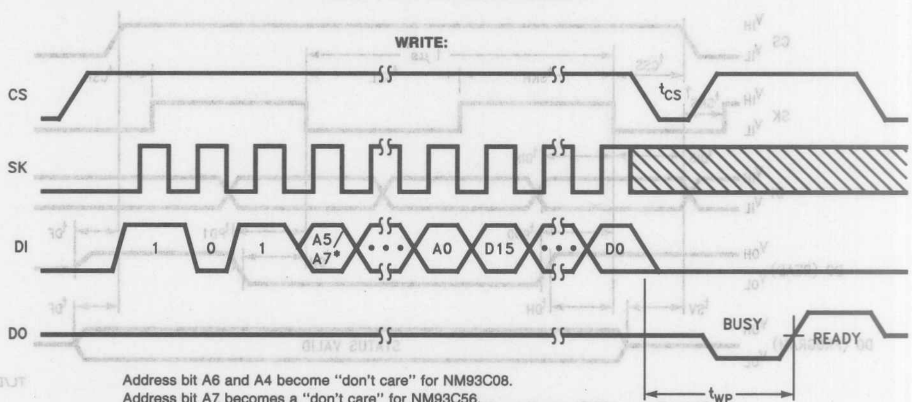
3.2.4 Typical T_{wp} vs Maximum T_{wp}

When the MICROWIRE EEPROMs the designer has three options to determine when the device has finished a programming cycle (either a write or erase instruction) as shown in *Figure 11*.

Option 1: μprocessor/μcontroller waits for $\mathbf{T_{wp(max)} = 10\ ms}$

Option 2: μprocessor/μcontroller polls Data-Out (DO) for Busy/Ready status $\mathbf{T_{wp(typ)} = 3\ ms}$

Option 3: if using the NM59C11 there is a separate RDY/BUSY pin: $\mathbf{T_{wp(typ)} = 3\ ms}$



TL/D/11429–13

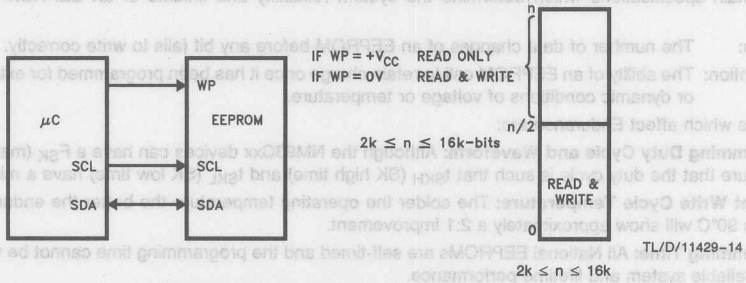
FIGURE 11. BUSY/READY Polling Options

All MICROWIRE EEPROMs can use options 1 or 2, and in the case of the NM59C11 there is a separate RDY/BUSY pin which the microcontroller/microprocessor can poll to determine the programming status.

4.0 WRITE PROTECTED MEMORY

4.1 I²C EEPROMs

National Semiconductor manufactures two versions of I²C EEPROMs: a "standard" version (NM24C02/04/08/16) and a "secure" version (NM24C03/05/09/17). The "secure" devices are fully software compatible with the standard devices plus they use one of the unused pins to implement a hardware write protect for the upper half block of the memory array.



TL/D/11429–14

FIGURE 12. I²C Secure Memory System

If the master does attempt to write to the protected memory, then the NM24C03/05/09/17 will accept the slave and word addresses, but will not generate an ACK, thus the programming cycle will not be started when the STOP condition is asserted.

4.2 MICROWIRE EEPROMs

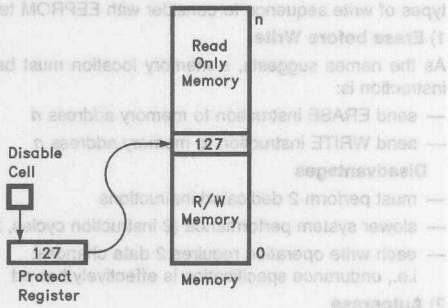
All NM93CSxx devices have the security feature which allows the user to define a portion of the memory to be write protected, either permanently or temporarily. This is useful for storing secure information in a system, such as calibration data. To control the secure memory involves a combination of setting a hardware pin and various software instructions as shown in *Figure 13*.

— Protect Register:
  Input PRE must be high and PREN instruction executed before a write to protect register

— Disable Cell:
  Set via PRDS instruction, input PRE must be high and PREN instruction executed
  PRDS is a one time only instruction

— Address in register defines first location to be protected

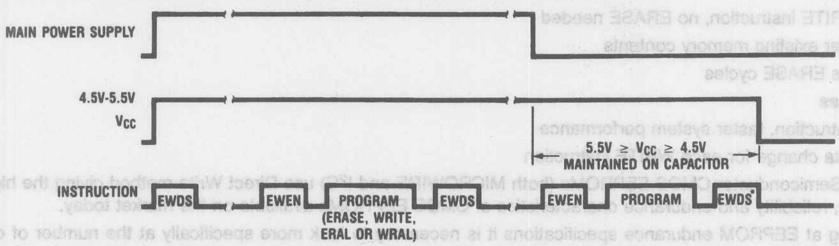
— Protect register may be altered unless PRDS is executed



TL/D/11429–15

FIGURE 13. Memory Protect Register

Data in serial MICROWIRE EEPROMs is further protected from spurious write cycles (especially during power transitions) by including a program disable mode which will automatically abort any requested Erase or Write cycles. *Figure 14* shows the suggested instruction flow for maximum data integrity with National's MICROWIRE EEPROMs.



TL/D/11429–16

*EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 14. Protecting Data in Serial EEPROMs

Typical Instruction flow for Maximum Data Protection

— Although EEPROM in non-volatile, the problem exists that stored data can be destroyed during power transitions.

— All National Semiconductor serial EEPROMs when initially powered up are in Program Disable Mode. In this mode it will abort any requested Erase or Write cycles.

5.0 EEPROM ENDURANCE AND SYSTEM LIFETIME

5.1 EEPROM Definitions

The two main specifications which determine the system reliability and lifetime of an EEPROM are Endurance and Data Retention.

Endurance: The number of data changes of an EEPROM before any bit fails to write correctly.

Data Retention: The ability of an EEPROM cell to retain charge once it has been programmed for extended periods under static or dynamic conditions of voltage or temperature.

Parameters which affect Endurance are:

- **Programming Duty Cycle and Waveform:** Although the NM93Cxx devices can have a F_{SK} (max) 1 MHz, it is important to make sure that the duty cycle is such that t_{SKH} (SK high time) and t_{SKL} (SK low time) have a minimum value of 250 ns.
- **Ambient Write Cycle Temperature:** The colder the operating temperature the better the endurance will be. For example 25°C vs 90°C will show approximately a 2:1 improvement.
- **Programming Time:** All National EEPROMs are self-timed and the programming time cannot be varied by the user, guaranteeing reliable system and lifetime performance.
- **Programming Voltage:** The lower the programming voltage V_{PP} the longer the required timing period T_{WP}. All National's EEPROMs operate from a single V_{CC} supply and have an on-board V_{PP} generator which is V_{CC} independent. This ensures that all National EEPROMs are both easy to use and highly reliable. The programming voltage cannot be varied by the user.

5.2 Read Cycles

Read cycles are non-destructive so all EEPROMs have the capability for an infinite number of reads.

5.3 Data Changes

With an EEPROM it is important to look at the endurance or number of write cycles the device can support. There are three types of write sequence to consider with EEPROM technology:

1) **Erase before Write**

As the names suggests, a memory location must be erased before it can be written to. A typical software flow for a write instruction is:

— send ERASE instruction to memory address *n*

— send WRITE instruction to memory address *n*

Disadvantages

— must perform 2 dedicated instructions

— slower system performance (2 instruction cycles, 2 $\mathbf{T_{WP}}$ delays)

— each write operation requires 2 data changes;
i.e., endurance specification is effectively halved

2) **Autoerase**

— send WRITE instruction

— EEPROM automatically performs ERASE instruction, then performs the WRITE operation

Disadvantages

— still need 2 data changes for each WRITE cycle, thus reducing system performance and halving endurance rating

3) **Direct Write**

— single WRITE instruction, no ERASE needed

— writes over existing memory contents

— eliminates ERASE cycles

Advantages

— single instruction, faster system performance

— single data change for each WRITE instruction

All National Semiconductor CMOS EEPROMs (both MICROWIRE and I^2C) use Direct Write method giving the highest system performance, reliability and endurance characteristics of CMOS EEPROMs available on the market today.

When looking at EEPROM endurance specifications it is necessary to look more specifically at the number of data changes (ERASE & WRITE) per write cycle. National specifies 1 write cycle to be 2 data changes (to be consistent with other manufacturer's datasheets whose products are either Erase before Write or Auto Erase), so the figure of 500k Write cycles is actually equivalent to an endurance figure of 1 Million (10^6) data changes.

National Semiconductor produce full product qualification booklets giving process performance and reliability characteristics; for a copy contact your local National Sales representative.

6.0 CONCLUSION

National Semiconductor offer the widest range of serial EEPROMs covering two main industry standard serial interfaces;

MICROWIRE:
- e.g. NM93Cxx, NM93CSxx
- size: 256-bit ⟶ 4 kbit (16 kbit coming)

I^2C:
- e.g. NM24Cxx
- size: 2k ⟶ 16 kbits

All these EEPROMs offer the same high specifications of:

Endurance:	10^6 data changes
Direct Write:	no erase cycle required
Data Retention:	greater than 40 years
Self-Timed Write Cycle:	typical write cycle time 5 ms
Sequential Read:	NM93CSxx, NM24Cxx devices
Memory Protect:	NM93CSxx, NM24C03/05/09/17

These features make them easy to use, allowing the system designer to achieve high performance, highly reliable systems.

REFERENCES

National Semiconductor Memory Databook
National Semiconductor CMOS Logic Databook

Programmable Switches

INTRODUCTION

National's NM95C12 is a 1024-bit Serial EEPROM with 8 programmable switches. These outputs can provide logic and analog switch inputs and outputs on a parallel bus, allowing this device to perform functions such as polling via the serial bus, interrupts via the serial bus and converting parallel data onto the serial bus.

FUNCTIONAL DESCRIPTION

Figure 1 is a block diagram of the NM95C12. It consists of a 61-word x 16-bit EEPROM array, a 16-bit Initial Switch Register (ISR), a 16-bit Switch Configuration Register (SCR), a 16-bit Switch Readback Register (SRR), four identical blocks of switch logic, programming and power-up circuits and control logic.

Addresses 0–60 of the EEPROM are available to the user as general purpose non-volatile memory. Data may be read or programmed into this memory using the appropriate instructions.

Address 61 is also an EEPROM location, but it is used as the ISR to provide the initial switch configuration information automatically on power-up.

Address 62 is the location of the SCR, which controls the switch logic of the output terminals. This address contains a volatile memory and therefore does not have endurance or programming time limits associated with it, allowing the outputs to be reconfigured an unlimited number of times.

Address 63 contains the SRR. This is a read-only register that reads back the logic levels present on the switch terminals. Only 8-bits of the SRR are used.

The NM95C12 also includes a Sequential Register Read function that allows the user to obtain an endless loop of data by entering the read mode and leaving the CS high.

SWITCH CONFIGURATIONS

The 16-bit SCR format is shown in *Figure 2*. It consists of four 4-bit fields. Each field controls its corresponding switch control logic. The individual bits in each field are labelled W, X, Y and Z. Table I shows the relationship between these bit values and the resulting behavior of the terminals.

Each switch pair can be individually configured to 1 of 14 modes. Therefore both logic and analog switches can be implemented simultaneously.

The logic switch configurations are at standard TTL levels.

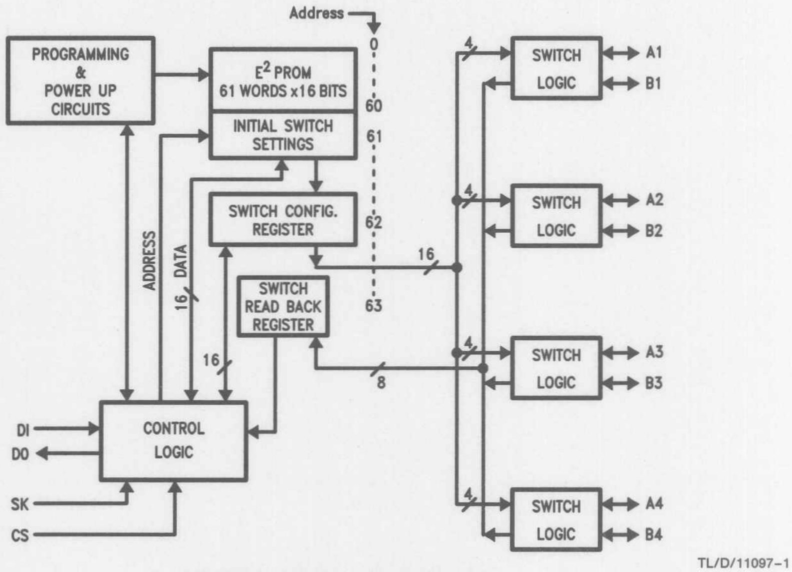
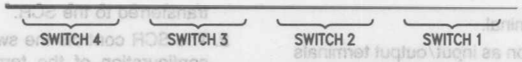


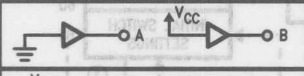
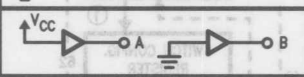
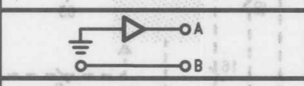
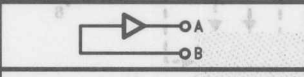
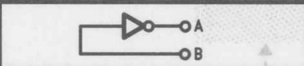
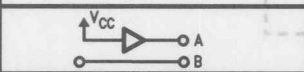
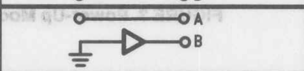
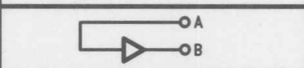
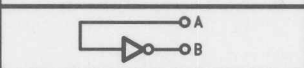
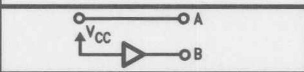
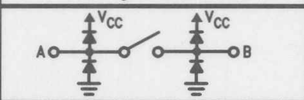
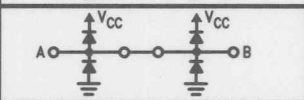
FIGURE 1. NM95C12 Block Diagram



TL/D/11097–2

FIGURE 2. Switch Configuration Register (SCR)

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = Tristate
5	0	1	0	1		A = B
6	0	1	1	0		A = $\bar{B}$
7	0	1	1	1		A = 1 , B = Tristate
8	1	0	0	0		A = Tristate , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = $\bar{A}$
11	1	0	1	1		A = Tristate , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

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For example, in Mode 1, Terminal A would be driving V_{OL} and Terminal B would be driving V_{OH}. In Mode 5, where an input and output structure exists, Terminal A would be driving V_{IL} or V_{IH}. The switches also include a TRI-STATE® mode to represent an open terminal.

Each switch pair can also function as input/output terminals in Modes 5, 6, 9, 10 and 13. Modes 4, 7, 8, 11 and 12 represent the same input/output functions, but with the switch in the "open" configuration.

POWER-UP MODE

When the NM95C12 is powered-up:

1. The data previously stored in the ISR is automatically transferred to the SCR.
2. The SCR controls the switch logic, producing the switch configuration of the terminals A1 through A4 and B1 through B4.

The switch configuration is valid 1 ms after the device power supply reaches 4.5V or greater.

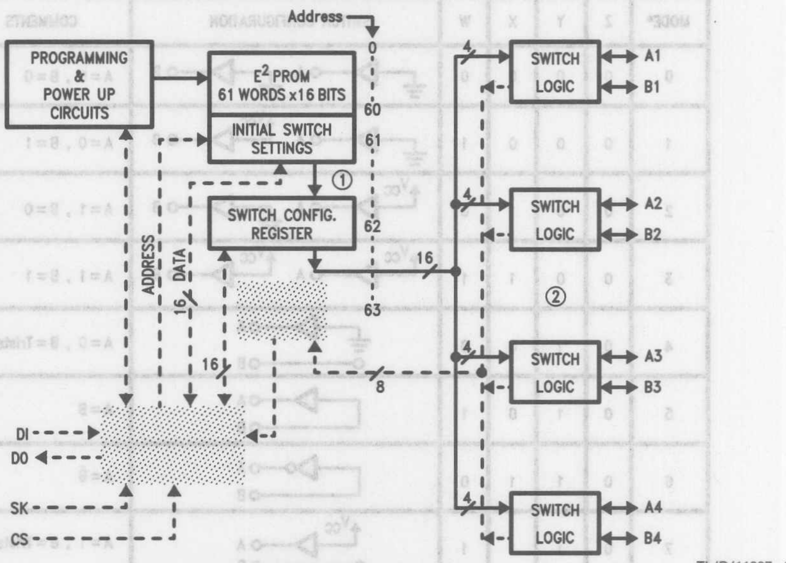

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FIGURE 3. Power-Up Mode

UPDATE MODE

To update the information that is contained in the SCR and therefore on the output terminals:

1. The SCR is updated via the serial bus by writing to address 62.
2. The switch logic updates the outputs by selecting the 1 of 14 modes detailed in Table I. The configuration change becomes effective at the terminals after a brief propagation delay (t_{SWPD}), referenced to the falling edge of CS.

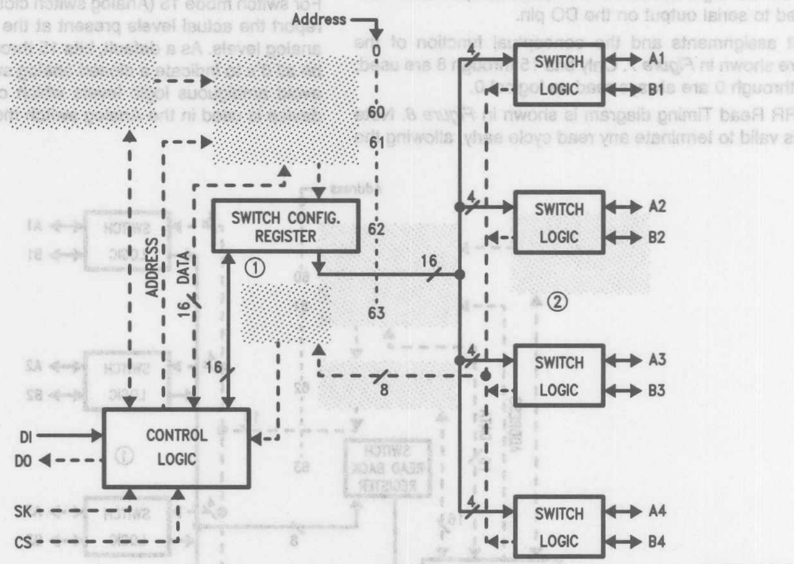

FIGURE 4. Update Mode

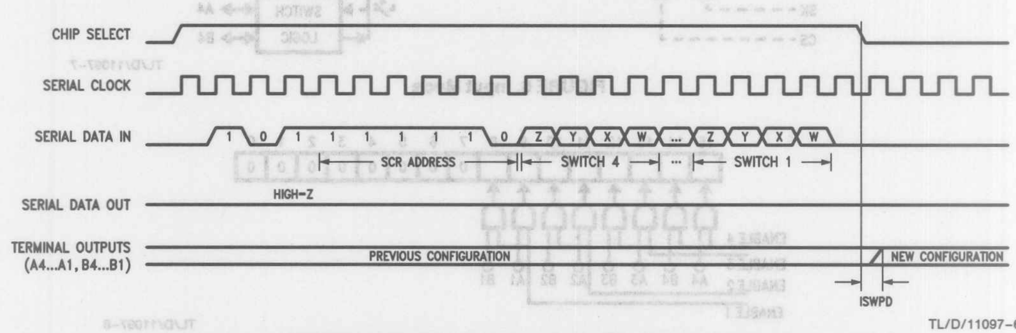

FIGURE 5. SCR Write (Update Mode) Timing Diagram

2. The control logic allows the 8-bit parallel input to be converted to serial output on the DO pin.

The bit assignments and the conceptual function of the SRR are shown in *Figure 7*. Only bits 15 through 8 are used; Bits 7 through 0 are always read as logical 0.

The SRR Read Timing diagram is shown in *Figure 8*. Note that it is valid to terminate any read cycle early, allowing the

Mode 12, Analog switch open, is valid for SRR input mode. For switch mode 13 (Analog switch closed), the SRR will not report the actual levels present at the terminals due to the analog levels. As a default, bits 15 through 8 of the SRR will be all 0's to indicate a closed analog switch. This is done to avoid ambiguous logic levels which could exist when the device is used in the Analog switch mode.

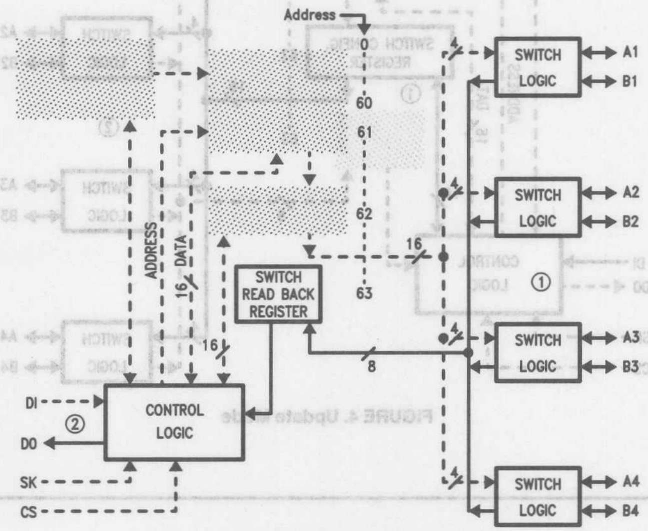

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FIGURE 6. Input Mode

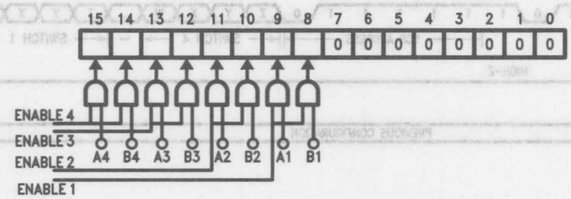

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FIGURE 7. Bit Assignments and Conceptual Function of the Switch Readback Register

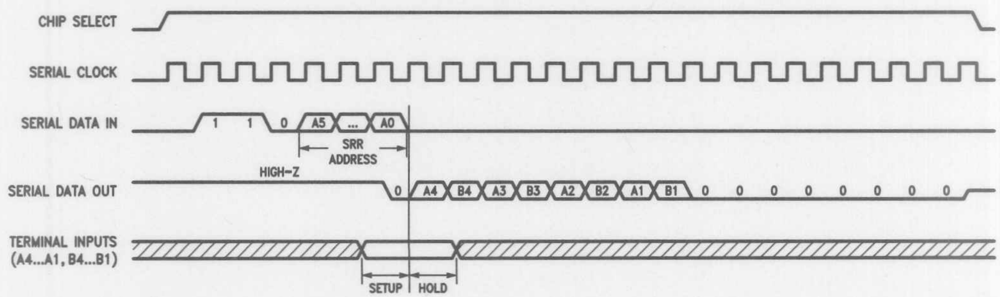

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FIGURE 8. SRR Read (Input Mode) Timing Diagram

location will be delivered on the DO pin. This sequential read can continue indefinitely whereby the address is automatically incremented after delivering 16 bits of data. In this mode the address count will continue through the ISR, SCR and SRR and then wrap around to Address 0.

During a sequential register read there will be a dummy bit preceding the first word read, after which, the bit stream will be continuous without any dummy bit separating the data words.

WRITE CYCLE CONSIDERATIONS

After loading the WRITE instruction and the 16-bit data, the chip enters into a self-timed programming cycle when CS is forced LOW before the next rising edge of the SK clock (refer to *Figure 9*). The timer status is available on the DO pin if the CS input is forced HIGH within 1 ms of starting the programming cycle. LOW on the DO pin indicates that programming is still in progress (BUSY), while HIGH indicates that the device is READY for the next instruction.

National's NM95C12 offers users the standard functionality of a 1024-bit EEPROM and includes 8 programmable terminals that can be used to implement both logic and Analog switch functions simultaneously. These switches can be used, for example, to replace mechanical DIP and SPST switches, as well as allow interrupt polling via the serial bus. When the device is powered-up, the switch configuration is automatically transferred to the output terminals. The terminals can be updated easily by executing a write cycle. In the input mode, the current logic level at the output terminals is read into the device and output onto the serial bus.

The NM95C12 combines unique and useable features with the simplicity of standard EEPROM functionality.

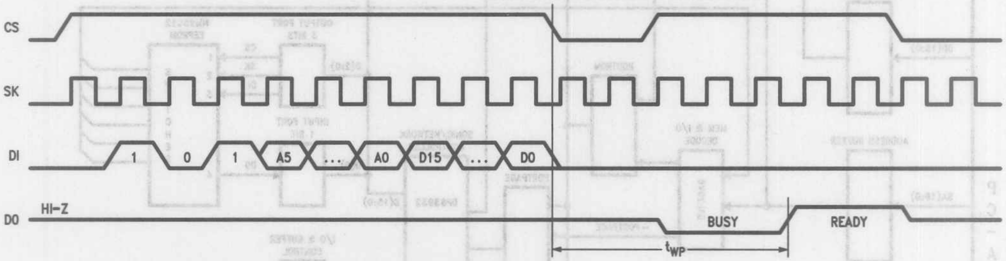

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FIGURE 9. WRITE Timing Diagram

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NM95C12 Applications in a PC-AT® Ethernet® Adapter

National Semiconductor
Application Note 792
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INTRODUCTION

This application describes a typical Ethernet adapter card designed to be plugged into a PC-AT expansion slot. The board is designed around the National Semiconductor DP83932 SONIC™ Network Controller device. This application note will detail the system design and focus on the functions performed by the NM95C12 EEPROM.

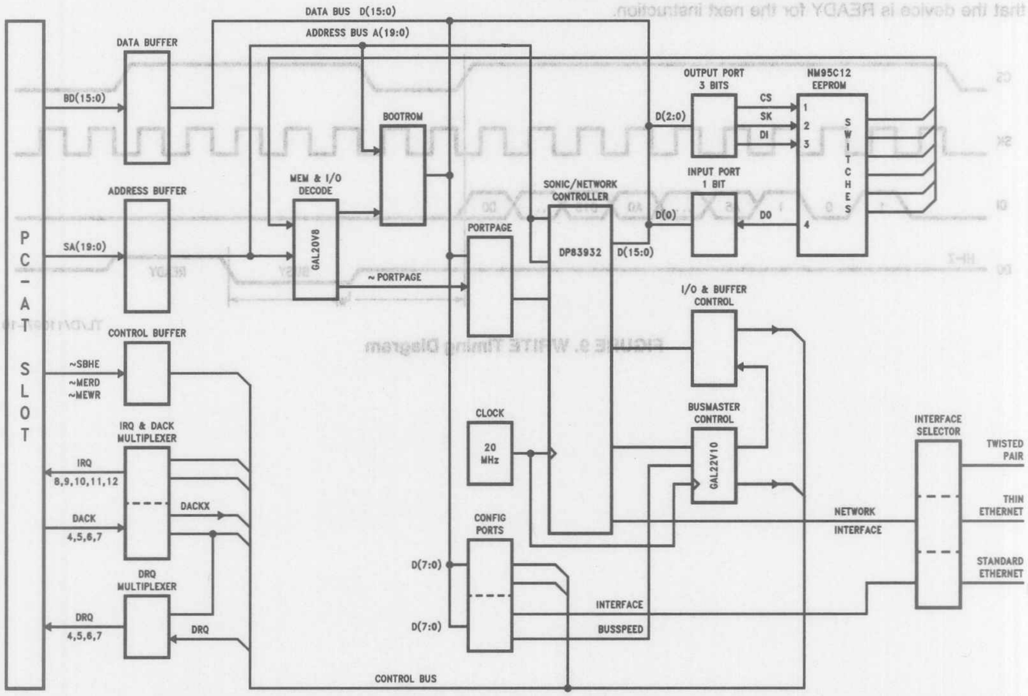
This application note assumes that the reader is familiar with the PC-AT architecture, the DP83932 device, the NM95C12 EEPROM and designing with GAL® Programmable Logic Devices (PLDs).

SYSTEM DESCRIPTION

The network controller card has been designed to meet the following specifications:

- Designed around high performance 32-bit DP83932 Ethernet Controller
- 16-Bit bus master operation to give higher performance
- Fully software configurable (no jumpers or mechanical DIP switches)
- Extensive test and configuration capabilities
- Supports different media interfaces
- Bootrom option

The system block diagram is shown in *Figure 1.*



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*Denotes an active low signal.

FIGURE 1. System Block Diagram

FUNCTIONAL DESCRIPTION OF THE BOARD

The system contains the following logical functions:

1. Network controller (DP83932)
2. Cable interfaces
3. Busmaster interface logic, including data and address buffers
4. EPROM option for remote boot loader

This system uses both the EEPROM locations and the switch logic terminals of the NM95C12 to perform various functions within the system as detailed below.

FUNCTIONAL DESCRIPTION OF NM95C12 EEPROM

Use of the Switches:

The switch terminals of the NM95C12 EEPROM are used as part of the memory map address decoding and the I/O map decoding circuitry, feeding as inputs to a GAL20V8 which performs the address decoding logic from the system address inputs.

The NM95C12 switches control:

1. The base I/O address of the network controller board.
2. The base memory address of the bootrom EPROM option on the board.

ADDRESS DECODING

The address decoding is controlled by a GAL20V8 PLD (refer to the 1990 National Semiconductor PLD Databook and Design Guide for further information) as shown in *Figure 2*.

The inputs to the GAL20V8 are the system address lines, the memory and I/O control signals, and the switch terminals from the NM95C12. The outputs from the GAL20V8 are the various chip select signals for the memory and I/O ports. The system address bus transmits the current address value and the M/~IO signal determines if a memory or I/O cycle is in progress.

Address lines A0–A19 allow up to 1 Meg (0–FFFFF) of memory to be addressed, while address lines A0–A15 allow up to 64K (0-FFFF) of I/O ports to be addressed. If the control signal M/~IO is logical "1" (high) then the processor is performing a memory cycle and if the M/~IO signal is logical "0" then an I/O cycle is in operation.

For a PC-AT various memory and I/O locations are reserved for standard functions such as system memory and I/O (refer to PC-AT documentation to determine which memory and I/O locations are free for add-in boards).

The switch outputs from the NM95C12 are connected as inputs to the GAL address decode logic and are used to determine the base memory and I/O locations for the add-in card. *Figure 2* shows the typical use of a GAL for address decoding.

The advantage of using a PLD for the address decoding is that it is an easy way to implement different address decode functions by logic equations. The logic equations can be implemented with a standard PLD design compiler such as OPAL™ from National Semiconductor or a third party software package such as ABEL™ from Data I/O. The PLD compiler will take the logic equations and convert them into the GAL fuse map which can be used for programming on a wide range of device programmers. A typical set of logic equations using National Semiconductors OPAL software package is shown in *Figure 3*.

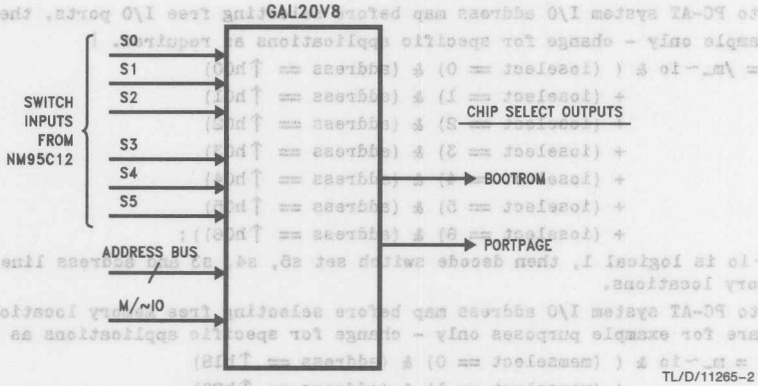


FIGURE 2. Address Decoding

```
BEGIN HEADER
TITLE    Address decoding for PC AT Ethernet adapter card
PATTERN  Addr_Dec
REVISION Rev 0
AUTHOR   Dave Engineer
COMPANY  National Semiconductor
DATE     June 1991
Everything in the header command is copied directly into the JEDEC map as a comment field for
easy documentation
END HEADER

BEGIN DEFINITIONS
device G20V8;                                        { specify the device used }
inputs s0, s1, s2, s3, s4, s5;                       { define the inputs }
inputs m_~io, a0, a1, a2, a3, a4, a5;
outputs(com) bootroom, portpage;                     {define the outputs}
{ OPAL will perform automatic pin assignment }
set ioselect=[s2,s1,s0], memselect=[s5,s4,s3];       { define the switch sets }
set address=[a5,a4,a3,a2,a1,a0];
END DEFINITIONS

BEGIN EQUATIONS
{" / " = logical NOT function (i.e. logical 0)
 " & " = logical AND function
 " + " = logical OR function }
{ if m_~io is logical 0, then decode switch set s2, s1, s0 and address lines for the various
base I/0 locations.
  Refer to PC-AT system I/0 address map before selecting free I/0 ports, the decodes shown are
  for example only - change for specific applications as required. }
bootrom = /m_~io & ( (ioselect == 0) & (address == ↑h00)
                   + (ioselect == 1) & (address == ↑h01)
                   + (ioselect == 2) & (address == ↑h02)
                   + (ioselect == 3) & (address == ↑h03)
                   + (ioselect == 4) & (address == ↑h04)
                   + (ioselect == 5) & (address == ↑h05)
                   + (ioselect == 6) & (address == ↑h06));
{ if m_~io is logical 1, then decode switch set s5, s4, s3 and address line for the various
base memory locations.
  Refer to PC-AT system I/0 address map before selecting free Memory locations, the decodes
  shown are for example purposes only - change for specific applications as required. }
portpage = m_~io & ( (memselect == 0) & (address == ↑h18)
                   + (memselect == 1) & (address == ↑h20)
                   + (memselect == 2) & (address == ↑h28)
                   + (memselect == 3) & (address == ↑h30)
                   + (memselect == 4) & (address == ↑h38);
END EQUATIONS
```

FIGURE 3. GAL® Logic Equations

USE OF THE NM95C12 EEPROM LOCATIONS

1. Three locations are used to store the ethernet address of the card.
2. One location is used to store the interrupt number and the DMA channel of the board.
3. One location is used to store the busmaster speed setting of the card.
4. Two locations are used to store information about the production flow of the board e.g.; the version number of the out-going inspection, and serialization program which stores a unique ethernet address in the EEPROM.
5. There are also some EEPROM locations used to enable some special features in the network driver such as protocol, DMA priority, etc.

Figure 4 below shows the memory usage of the NM95C12.

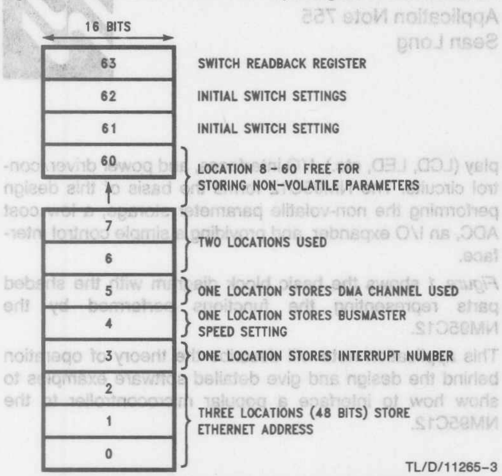


FIGURE 4. Memory Locations Used in NM95C12

FUNCTIONAL DESCRIPTION OF THE SOFTWARE

The driver for the card can be supplied in two ways:

1. As a driver which is loaded from the disk.
2. As a bootrom which is located at the card.

The driver determines the base I/O address of the card. This is done by scanning the possible I/O map where the card can be located (seven possible locations) and testing if the NM95C12 EEPROM can be found.

The EEPROM is found if, after an address is shifted in the EEPROM, the DO output from the NM95C12 has become logical "zero". Then the CS pin will be disabled and there will be a check if the DO output pin will become high (this pin is pulled up with a 47K resistor).

When the software finds the base address of the card, it reads the locations which contain the DMA and IRQ number to use and programs these values into the corresponding output latches. These latches will enable and/or multiplex the corresponding DMA (DACKx, DRQx) and INT (IRQx) to the busmaster logic and interrupt logic.

The same operation is done for the busmaster speed, one location in the EEPROM determines the active low and high time for busmaster cycles, the output of this latch will go to the busmaster state machine (implemented in a GAL22V10).

The ethernet address will be read by the driver and copied to a private location in the driver data area for use with the network software.

The bootrom can be located at five locations in memory (controlled by the NM95C12 switch logic) and can be disabled if required.

CONCLUSION

This application has shown the many advantages of the NM95C12 EEPROM with DIP Switches. In this example the NM95C12 replaces the functions typically performed by a Bipolar PROM (store ethernet address), mechanical DIP switches/jumpers (select options), and general read/write logic (software testing of the hardware configuration). The use of the switch terminals as part of the address decode logic makes the address decode function more flexible and allows for software control.

The easy interfacing to the NM95C12 (just four pins) and the simple, but powerful instruction set allows the NM95C12 to give the system designer:

- Greater flexibility
- Fully software controllable and testable
- Greater reliability (no mechanical switches or jumpers)
- Reduced component count
- Lower component cost

Applications

INTRODUCTION

This application note describes a general purpose industrial controller and details how a NM95C12 can be used to integrate a number of different functions typically found in such a design.

General purpose application examples of the use of the NM95C12 are presented rather than a specific design. Each design idea and software can be incorporated into the designer's required application.

The basic building blocks of an industrial controller (for example, heating, process control, etc.) are a microcontroller, an Analogue to Digital Converter (ADC), an EEPROM, a display (LCD, LED, etc.), I/O interfaces, and power driver/control circuits. The NM95C12 forms the basis of this design performing the non-volatile parameter storage, a low cost ADC, an I/O expander, and providing a simple control interface.

Figure 1 shows the basic block diagram with the shaded parts representing the functions performed by the NM95C12.

This application note will describe the theory of operation behind the design and give detailed software examples to show how to interface a popular microcontroller to the NM95C12.

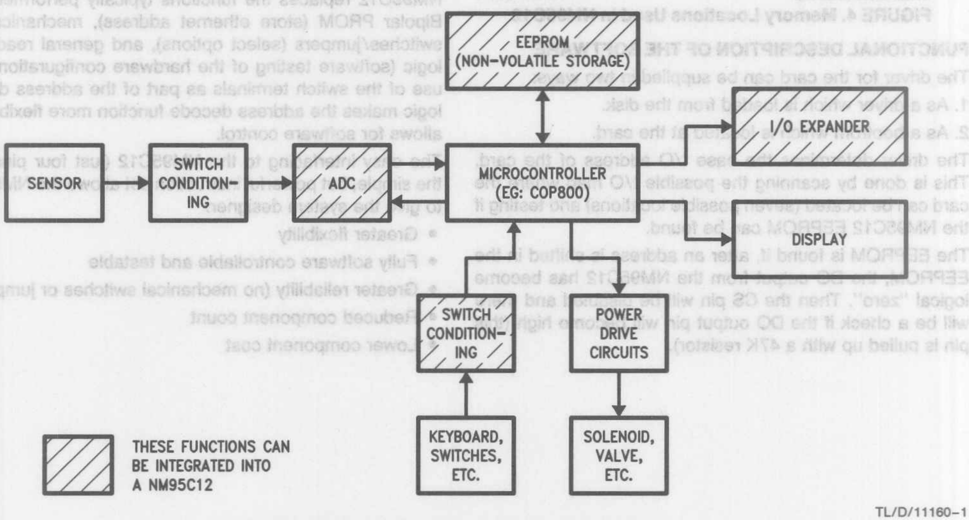
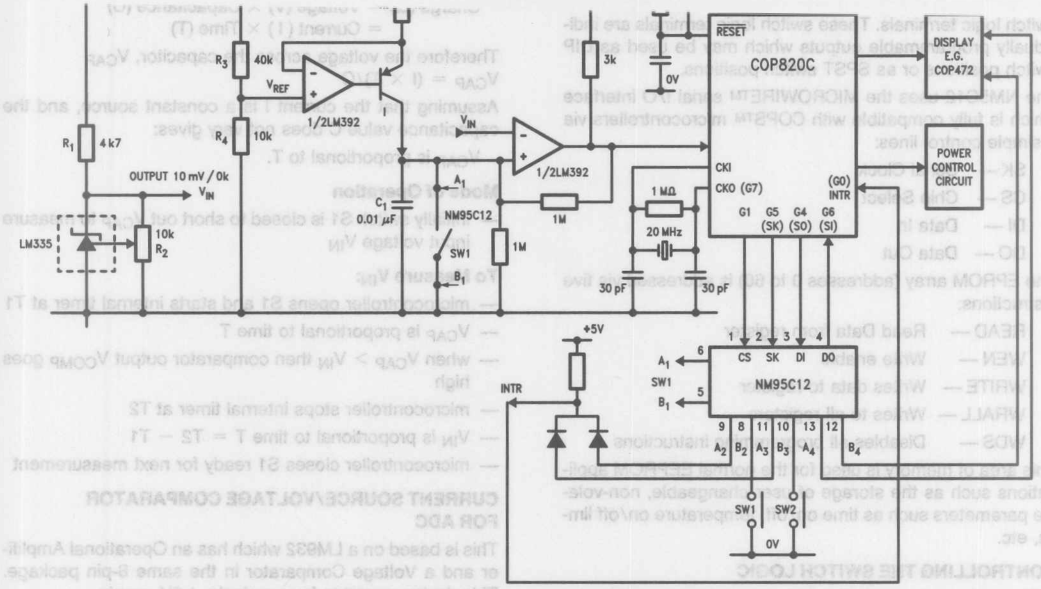


FIGURE 1. Typical Industrial Controller Block Diagram



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COP820/NM95C12 Industrial Controller

THE NM95C12 1024-BIT CMOS EEPROM WITH DIP SWITCHES

The NM95C12 features 1K-bit EEPROM memory with 8 switch logic terminals. These switch logic terminals are individually programmable outputs which may be used as DIP switch positions or as SPST switch positions.

The NM5C12 uses the MICROWIRE™ serial I/O interface which is fully compatible with COPS™ microcontrollers via 4 simple control lines:

SK — Serial Clock
CS — Chip Select
DI — Data In
DO — Data Out

The EPROM array (addresses 0 to 60) is addressed via five instructions:

READ — Read Data from register
WEN — Write enable
WRITE — Writes data to register
WRALL — Writes to all registers
WDS — Disables all programming instructions

This area of memory is used for the normal EEPROM applications such as the storage of user changeable, non-volatile parameters such as time on/off, temperature on/off limits, etc.

CONTROLLING THE SWITCH LOGIC

Address locations 61 to 63 control the switch operation.

Address	Name	Description
61	ISS	Provides the initial switch configuration automatically on power-up. Controlled via a WRITE operation.
62	SCR	The SCR is not an E2 location and hence is volatile. The SCR is loaded automatically from address 61 on power-up. The SCR controls the switch terminals A1–A4 and B1–B4.
63	SRR	The SRR allows the current logic levels of the switch terminals to be read back via the MICROWIRE bus.

THEORY OF OPERATION

The relationship for charge of a capacitor is as follows:

$$\text{Charge (Q)} = \text{Voltage (V)} \times \text{Capacitance (C)} = \text{Current (I)} \times \text{Time (T)}$$

Therefore the voltage across the capacitor, V_{CAP}

$V_{CAP} = (I \times T)/C$

Assuming that the current I is a constant source, and the capacitance value C does not vary gives:

V_{CAP} is proportional to T.

Mode of Operation

— initially switch S1 is closed to short out V_{CAP} to measure input voltage V_{IN}

To Measure V_{IN}:

— microcontroller opens S1 and starts internal timer at T1

— V_{CAP} is proportional to time T

— when $V_{CAP} > V_{IN}$ then comparator output V_{COMP} goes high

— microcontroller stops internal timer at T2

— V_{IN} is proportional to time $T = T2 - T1$

— microcontroller closes S1 ready for next measurement

CURRENT SOURCE/VOLTAGE COMPARATOR FOR ADC

This is based on a LM932 which has an Operational Amplifier and a Voltage Comparator in the same 8-pin package. This device operates from a single +5V supply.

Refer to the National Semiconductor General Purpose Linear Databook for further details of the LM392.

INPUT SENSOR

For this example assume temperature needs to be controlled.

LM335: This is a precision, low-cost, easily calibrated two terminal temperature sensor that behaves like a zener diode with a voltage of +10 mV/degree Kelvin. The initial accuracy is ±1° and can be externally trimmed with a potentiometer connected to the ADJ pin.

Refer to the National Semiconductor Linear Databook 2 for further details of the LM335 Temperature Sensors.

NM95C12 SWITCH LOGIC APPLICATIONS/ CONFIGURATIONS

A_1, B_1—Control the Charge/Discharge of Capacitor for ADC

Switch Configuration:

Analog Switch Open: Mode 12, ZYXW = 110?
(? = don't care)

Analog Switch Closed: Mode 13, ZYXW = 111?

To change the state of the switch terminals A_1, B_1, follow the flowchart in *Figure 3*.

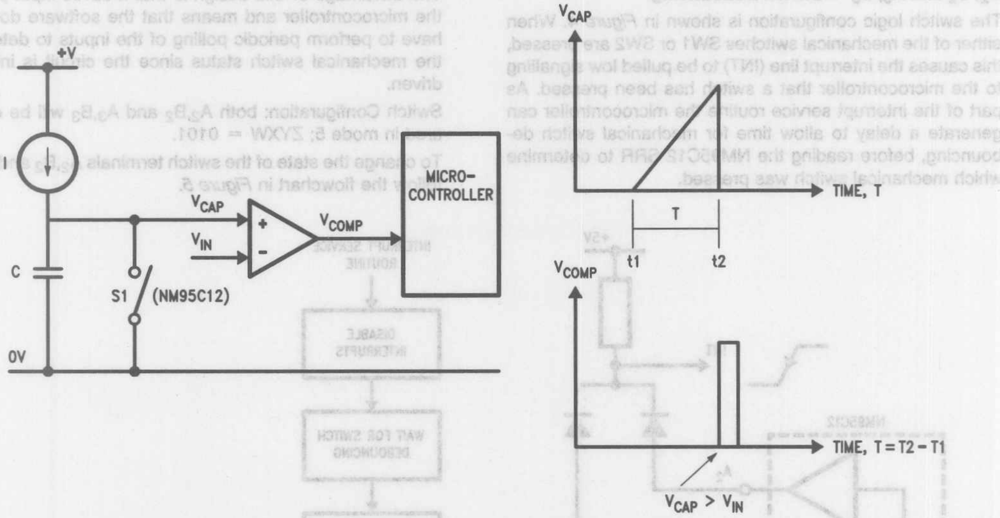

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FIGURE 2. Single Slope Analogue to Digital Converter

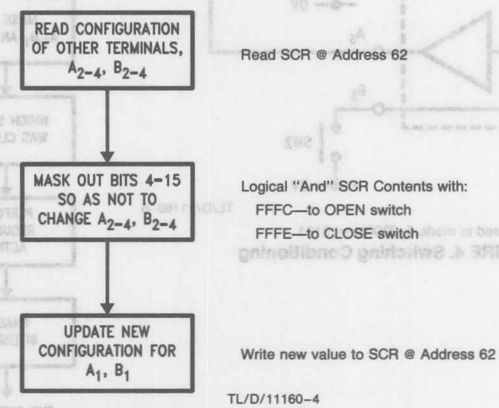

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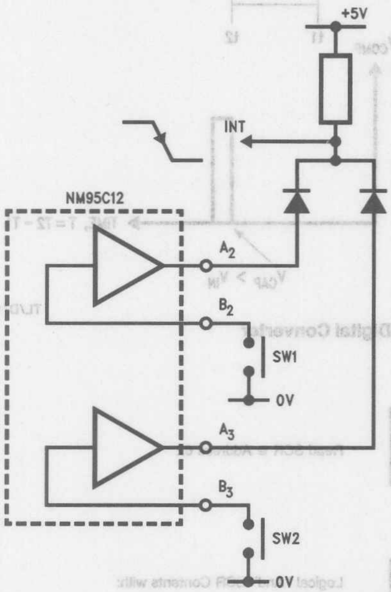
FIGURE 3. Controlling Switch Terminals A1, B1

A_2, B_2 and A_3, B_3 — Switch Debouncing

The switch logic configuration is shown in *Figure 4*. When either of the mechanical switches SW1 or SW2 are pressed, this causes the interrupt line (INT) to be pulled low signalling to the microcontroller that a switch has been pressed. As part of the interrupt service routine the microcontroller can generate a delay to allow time for mechanical switch debouncing, before reading the NM95C12 SRR to determine which mechanical switch was pressed.



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A_2,B_2, A_3,B_3 Configured in mode 5, ZYXW = 0101

FIGURE 4. Switching Conditioning

The advantage of this design is that it saves input pins on the microcontroller and means that the software does not have to perform periodic polling of the inputs to determine the mechanical switch status since the circuit is interrupt driven.

Switch Configuration: both A_2,B_2 and A_3,B_3 will be configured in mode 5; ZYXW = 0101.

To change the state of the switch terminals A_2,B_2 and A_3,B_3 follow the flowchart in *Figure 5*.

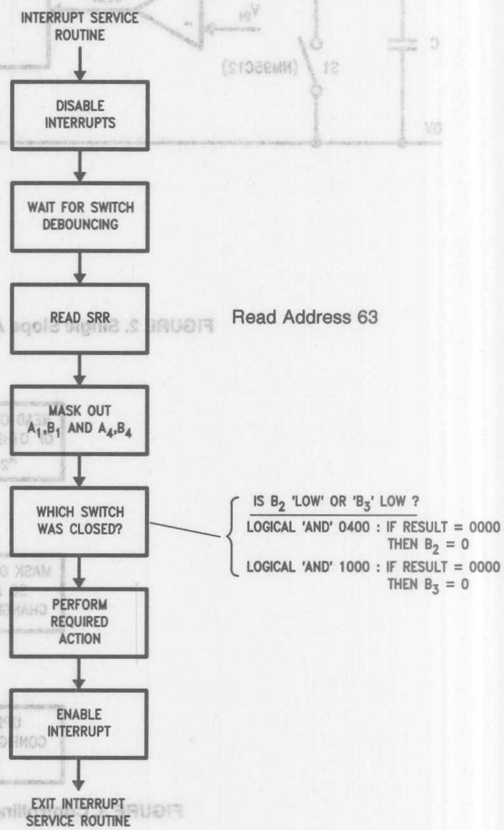

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FIGURE 5. Controlling Switch Terminals A_2,B_2, A_3,B_3

A_4,B_4 Programmable I/O

These two terminals use mode 1 to 4 according to the logic level required on the output. In this example A_4 is used for the Display Chip Select signal and B_4 is used for the Display On/Off control signal.

In order to update and display the contents of the Display then both terminals A_4 and B_4 need to be set to a logic "1" therefore A_4,B_4 are configured in mode 3 with ZYXW = 0011.

To change the state of the switch terminals A_2,B_2 and A_3,B_3 follow the flowchart in *Figure 6*.

SOFTWARE TO INTERFACING THE NM95C12 TO THE COP820 MICROCONTROLLER

This section includes a number of subroutines to interface to a NM95C12 as described in the design example above. There are subroutines to implement each of the basic instructions together with routines for configuring and controlling the switch logic. These subroutines can be used as the basis for a design and be tailored to meet the individual application requirements.

CONCLUSION

The NM95C12 is an extremely versatile and inexpensive device which allows simple interfacing to all popular microcontrollers and microprocessors via a 4-wire serial bus. The complete operation of the NM95C12 can be controlled by a few simple instructions.

The design outlined offers an inexpensive solution for industrial control applications with the key benefits of:

— simple interfacing between microcontroller, EEPROM, "ADC"

— low part count

— fully software controlled and changeable

This has highlighted the flexibility of the NM95C12 and how the switch terminals can be configured for a wide range of applications including: mechanical switch replacement, programmable Address Decoder, programmable I/O expander and a programmable interrupt controller. The NM95C12 offers greater reliability than mechanical switches with the benefits of software control and lower cost.

Plus you still get the 1K-bit EEPROM memory as well!; together with the 8 switch terminals it forms a truly remarkable device.

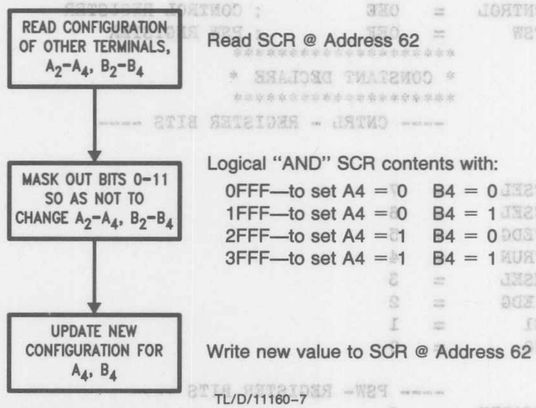


FIGURE 6. Controlling Switch Terminals A_4,B_4

```
; AS IN THE DATA-SHEETS.
;
; ****************************************************
; * PORT~ , CONFIGURATION- AND CONTROL REGISTERS *
; ****************************************************
        PORTLD   =   0D0          ; PORT L DATA
        PORTLC   =   0D1          ; PORT L CONFIGURATION
        PORTLP   =   0D2          ; PORT L PIN
;
        PORTGD   =   0D4          ; PORT G DATA
        PORTGC   =   0D5          ; PORT G CONFIGURATION
        PORTGP   =   0D6          ; PORT G PIN
        PORTD    =   0DC          ; PORT D
        PORTI    =   0D7          ; PORT I
;
        SIOR     =   0E9          ; SID SHIFT REGISTER
        TMRLO    =   0EA          ; TIMER LOW BYTE
        TMRHI    =   0EB          ; TIMER HIGH BYTE
        TAULO    =   0EC          ; TIMER REGISTER LOW BYTE
        TAUHI    =   0ED          ; TIMER REGISTER HIGH BYTE
;
        CNTROL   =   0EE          ; CONTROL REGISTER
        PSW      =   0EF          ; PSW REGISTER
;               ********************
;               * CONSTANT DECLARE *
;               ********************
;                ---- CNTRL - REGISTER BITS ----
;
        TSEL     =   7
        CSEL     =   6
        TEDG     =   5
        TRUN     =   4
        MSEL     =   3
        IEDG     =   2
        S1       =   1
        S0       =   0
;
;                ---- PSW- REGISTER BITS ----
        HCARRY   =   7
        CARRY    =   6
        TPND     =   5
        ENTI     =   4
        IPND     =   3
        BUSY     =   2
        ENI      =   1
        GIE      =   0

;                I/O - SIGNALS ----
;
        TMRINP   =   3
        INTR     =   0
        TIO      =   3
        SO       =   4
        SK       =   5
        SI       =   6
        CKO      =   7
;
        .CHIP    820
        LD       SP,#02F          ; DEFAULT INITIALIZATION OF SP
```

```
;INCLD COP820.INC
;
; This program provides in the form of subroutines, the ability to enable,
; disable, read and write to the NM95C12 EEPROM with DIP switches.
;
;       ************************************************
;       * PROGRAM VARIABLE MEMORY LOCATION DEFINITIONS  *
;       ************************************************
;
SNDBUF  = 0 ;CONTAINS THE COMMAND BYTE TO BE WRITTEN TO NM95C12
RDATL   = 1 ;LOWER BYTE OF THE NM95C12 REGISTER DATA READ
RDATH   = 2 ;UPPER BYTE OF THE NM95C12 REGISTER DATA READ
WDATL   = 3 ;LOWER BYTE OF THE DATA TO BE WRITTEN TO NM95C12 REGISTER
WDATH   = 4 ;UPPER BYTE OF THE DATA TO BE WRITTEN TO NM95C12 REGISTER
ADDRESS = 5 ;THE LOWER 6-BITS OF THIS LOCATION CONTAIN THE ADDRESS
            ;OF THE NM95C12 REGISTER TO BE READ/WRITTEN
FLAGS   = 6 ;USED FOR SETTING UP FLAGS
            ;
            ; FLAG VALUE       ACTION
            ; ----------       ------
            ;    00            WRITE ENABLE,DISABLE,WRITE ALL
            ;    01            READ CONTENTS OF NM95C12 REGISTER
            ;    03            WRITE TO NM95C12 MEMORY REGISTER
            ;    07            WRITE NM95C12 SCR REGISTER
            ;    OTHERS        ILLEGAL COMBINATION
;
; THE INTERFACE BETWEEN THE COP820C/840C AND THE NM95C12 (1024-BIT EEPROM)
; CONSISTS OF FOUR LINES. THE G1 (CHIP SELECT LINE), G4 (SERIAL OUT SO),
; G5 (SERIAL CLOCK SK) AND G6 (SERIAL IN SI).
;
; ANOTHER PINS USED BY THIS DESIGN IS G0 (INTERRUPT INTR)
;
;
;       ******************
;       * INITIALIZATION *
;       ******************
;
;
        LD PORTGC,032      ;Setup G1,G4,G5 as outputs
        LD PORTGD,00       ;Initialize G data reg to zero
        LD CNTROL,08       ;Enable MSEL, select MW rate of 2tc
        LD B,fPSW          ;Load B with address of PSW
        LD X,fSIOR         ;Load X with address of Serial I/O Register
;
;
;
;       ********************
;       * WEN INSTRUCTION  *
;       ********************
;
;
;
; THIS ROUTINE ENABLES PROGRAMMING OF THE NM95C12. PROGRAMMING MUST
; BE PRECEDED ONCE BY A PROGRAMMING ENABLE (WEN).
;
WEN:
        LD  SNDBUF,f030   ; LOAD OP CODE AND 'ADDRESS'
        LD  FLAGS,f0
        JSR INIT
        RET
;
;
;       ********************
;       * WDS INSTRUCTION  *
;       ********************
;
```

4

```
;
; THIS ROUTINE DISABLES PROGRAMMING OF THE NM95C12.
;
WDS:
        LD  SNDBUF,f0        ; LOAD OP CODE AND 'ADDRESS'
        LD  FLAGS,f0
        JSR INIT
        RET
;
;
;
;       ********************
;       * READ INSTRUCTION *
;       ********************
;
;
; THIS ROUTINE READS THE CONTENTS OF THE NM95C12 REGISTER.
; THE NM95C12 ADDRESS IS SPECIFIED IN THE LOWER 6-BITS OF
; LOCATION "ADDRESS". THE UPPER 2-BITS SHOULD BE SET TO ZERO.
; THE 16-BIT CONTENTS OF THE NM95C12 REGISTER ARE STORED IN
; RDATL AND RDATH.
;
READ:   LD  A,ADRESS     ; LOAD ADDRESS A5-A0 INTO ACCUMULATOR
        OR  A,f080       ; SET OP CODE BITS TO '10'
        X   A,SNDBUF     ; TRANSFER COMMAND BYTE TO SERIAL I/O VARIABLE
        LD  FLAGS,f1
        JSR INIT
        RET
;
;
;
;       *********************
;       * WRITE INSTRUCTION *
;       *********************
;
;
; THIS ROUTINE WRITES A 16-BIT VALUE STORED IN WDATL AND WDATH
; TO THE NM95C12 REGISTER WHOSE ADDRESS IS CONTAINED IN THE
; LOWER 6-BITS OF THE LOCATION "ADDRESS". THE UPPER 2-BITS OF
; ADDRESS LOCATION SHOULD BE SET TO ZERO.
;
WRITE:  LD  A,ADRESS      ; LOAD ADDRESS A5-A0 INTO ACCUMULATOR
        OR  A,f040        ; SET OP CODE BITS TO '01'
        X   A,SNDBUF      ; TRANSFER COMMAND BYTE TO SERIAL I/O VARIABLE
        LD  FLAGS,f3
        JSR INIT
        RET
;
;
;
;       *********************
;       * WRALL INSTRUCTION *
;       *********************
;
;
;
; THIS ROUTINE WRITES A 16-BIT VALUE STORED IN WDATL AND WDATH
; TO ALL THE NM95C12 REGISTERS
;
WRALL:  LD  SNDBUF,f040  ; LOAD OP CODE AND ADDRESS'
        LD  FLAGS,f3
        JSR INIT
        RET
;
;
```

```
;
;
; THIS ROUTINE WRITES A 16-BIT VALUE STORED IN WDATL AND WDATH
; TO THE NM95C12 SCR (SWITCH CONTROL REGISTER) WHOSE ADDRESS IS 62 DECIMAL
; WHICH EQUALS f03E HEXADECIMAL. OP CODE = '01'
; A WRITE TO THE SCR DOES NOT REQUIRE A PROGRAMMING CYCLE
;
WRSCR:  LD  SNDBUF,f07E  ; LOAD OP CODE AND ADDRESS
        LD  FLAGS,f7
        JSR INIT
        RET
;
;
;
;       ***********************************
;       * EXECUTE INSTRUCTION SUBROUTINES *
;       ***********************************
;
;
;
; THIS ROUTINE SENDS OUT THE START BIT AND THE COMMAND BYTE.
; IT ALSO DECIPHERS THE CONTENTS OF THE FLAG LOCATION AND TAKES
; A DECISION REGARDING WRITE, WRITE SCR, READ OR RETURN TO THE
; CALLING_ROUTINE.
;
INIT:   SBIT 1,PORTGD    ;SET CHIP SELECT HIGH
        LD SIOR,f001     ;LOAD SIOR WITH START BIT
        SBIT BUSY,[B]    ;SEND OUT THE START BIT
PUNT1:  IFBIT BUSY,[B]
        JP PUNT1
        LD A,SNDBUF
        X  A,[X]         ;LOAD SIOR WITH COMMAND BYTE
        SBIT BUSY,[B]    ;SEND OUT COMMAND BYTE
PUNT2:  IFBIT BUSY,[B]
        JP PUNT2
        IFBIT 0,FLAGS    ;ANY FURTHER PROCESSING?
        JP NOTDON        ;YES
        RBIT 1,PORTGD    ;NO, RESET CS AND RETURN
        RET
;
NOTDON:
        IFBIT 1,FLAGS    ;READ OR WRITE?
        JP WR95C12       ;JUMP TO WRITE ROUTINE
        LD SOIR,f000     ;NO, READ NM95C12
        SBIT BUSY,PSW    ;DUMMY CLOCK TO READ ZERO
        RBIT BUSY,[B]
        SBIT BUSY,[B]
PUNT3:  IFBIT BUSY,[B]
        JP PUNT3
        X  A,[X]
        SBIT BUSY,[B]
        X  A,RDATH
```

4

```
PUNT4:  IFBIT BUSY,[B]
        JP PUNT4
        LD A,[X]
        X  A,RDATL
        RBIT 1,PORTGD
        RET
;
WR95C12:
        LD  A,WDATH
        X   A,[X]
        SBIT BUSY,[B]
PUNT5:  IFBIT BUSY,[B]
        JP  PUNT5
        LD  A,WDATL
        X   A,[X]
        SBIT BUSY,[B]
PUNT6:  IFBIT BUSY,[B]
        JP  PUNT6         ; FINISHED CLOCKING OUT DATA
        RBIT 1,PORTGD     ; RESET CHIP SELECT
        IFBIT 2, FLAGS    ; WRITE/WRALL OR WRSCR?
        RET               ; WRSCR , NO PROGRAMMING TIME SO RETURN
        SBIT 1,PORTGD     ; SET CHIP SELECT TO ALLOW TO POLL DO FOR BUSY/READY
POLL:   IFBIT SI,PORTGP ; IS NM95C12 DO = SI LOW?
        JP ENDTWP         ; DO HAS GONE HIGH, SO END PROGRAMMING CYCLE
        JP POLL           ; DO IS STILL LOW, SO KEEP POLLING
;
ENDTWP;
        BIT 1, FLAGS      ; RESET CHIP SELECT
        RET
;
        .END
```

Using the NM95C12 to Solve Common Manufacturing Problems

National Semiconductor
Application Note 756
Kent Brooten

INTRODUCTION

This application note describes how the NM95C12 E^2P-ROM + Dip Switches is utilized to reduce manufacturing costs and increase reliability.

PROBLEM

The application described herein is a factory programmable power supply. The existing system *(Figure 1)* requires one of three different power supplies, depending on the options installed in the final unit. The design engineer has presented two solutions:

1. Three different assemblies, one for each output configuration, or,
2. One assembly with a dip switch (or jumpers) to select the configuration.

The manufacturing engineer would prefer to have one assembly that would satisfy all three needs. Dip switches are undesirable because they are difficult to flow solder when on the PCB (and later clean the PCB) as well as posing a threat to the final system should an untrained technician choose to change a switch setting (thus altering the output voltage). Jumpers are undesirable since they require hand soldering—an additional step.

The manufacturing engineer would prefer to have one final test program—not three.

THE SOLUTION

The NM95C12 provides the solution. It enables the power supply module to be configured for any of the three output voltages. There only needs to be one assembly. No dip switches or jumpers are used. The Automatic Test Equipment (ATE) used at final test can check all three configurations. The test program can set the final configuration as well as assign a serial number and date of manufacture which is stored in the EEPROM.

THE DESIGN

The power supply is designed using an LM2577 switching regulator ("the Simple Switcher") in the flyback mode *(Figure 2)*. The resistor divider R_1/R_2 set the output voltages V_{OUT1} and V_{OUT2}. All three output voltages can be set by merely selecting which combination of R_1/R_2 is connected to the feedback pin of the switching regulator. When the switches in the NM95C12 are configured for the analog switch mode, they can be used to connect the appropriate switch to the feedback pin of the Simple Switcher™.

The manufacturing group need only produce one assembly which is electronically configured either at final test or during final assembly. An increase in manufacturing efficiency results.

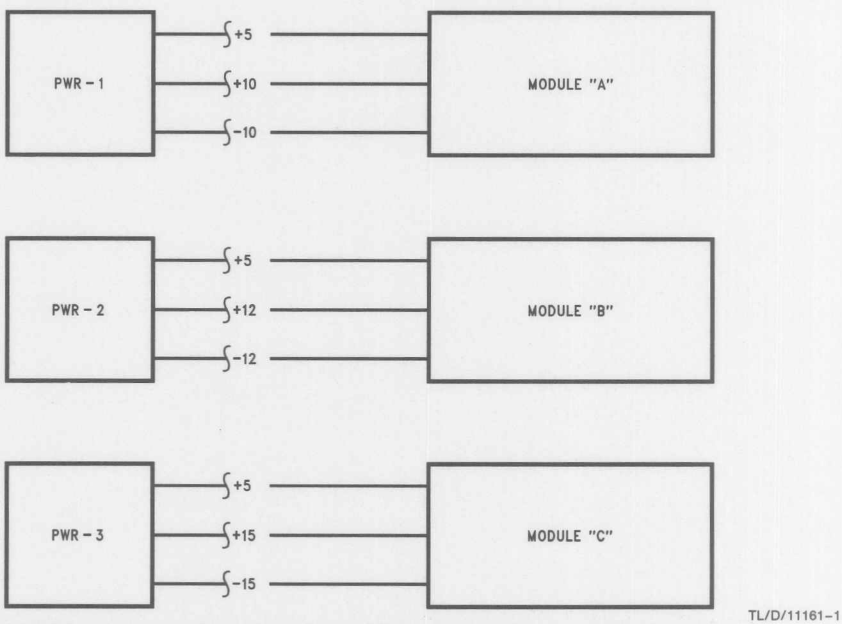


FIGURE 1. Modules A, B, C Each Require Slightly Different Power Supply Modules

During final test, the ATE can check each switch position by sending serial commands via the serial μWIRE interface of the NM95C12. The serial number and date of manufacture can be stored at this time. Output configuration can be selected at final test or the power supply modules can be stored and the output voltage programmed at a later time.

Note that there is no microcontroller necessary in the system. While the NM95C12 is typically utilized in a μController based system, it can also be used in non-μController applications. The ATE provides programming and control of the NM95C12 and connects to pads on the PCB via a bed-of-nails test fixture. Alternatively, the Clock, Data IN, Data OUT and Chip Select lines can be routed to fingers on an edge connector.

PROGRAMMING

The programming example is written in the popular Z80 assembly language. An NSC800 is used for this example. Flow charts are shown for each module.

SUMMARY

The NM95C12 is used in this application to replace a dip switch. The user benefits in many ways:

1. Increased efficiency by manufacturing 1 large lot of sub-assemblies rather than 3 smaller ones,
2. Ease of manufacturing since neither mechanical dip switches have to be treated with extra care nor jumpers specially installed,
3. Only 1 sub-assembly needs to be inventoried, cutting costs,
4. Increased reliability because mechanical devices are not used,
5. Increased efficiency at final test since only 1 test program can check all three configurations,
6. Inventory costs are reduced because 1 assembly will satisfy any of 3 different functions, and
7. A history of the module can be stored in the EEPROM portion of the device including serial number, date of manufacture, date of last repair, etc.

4

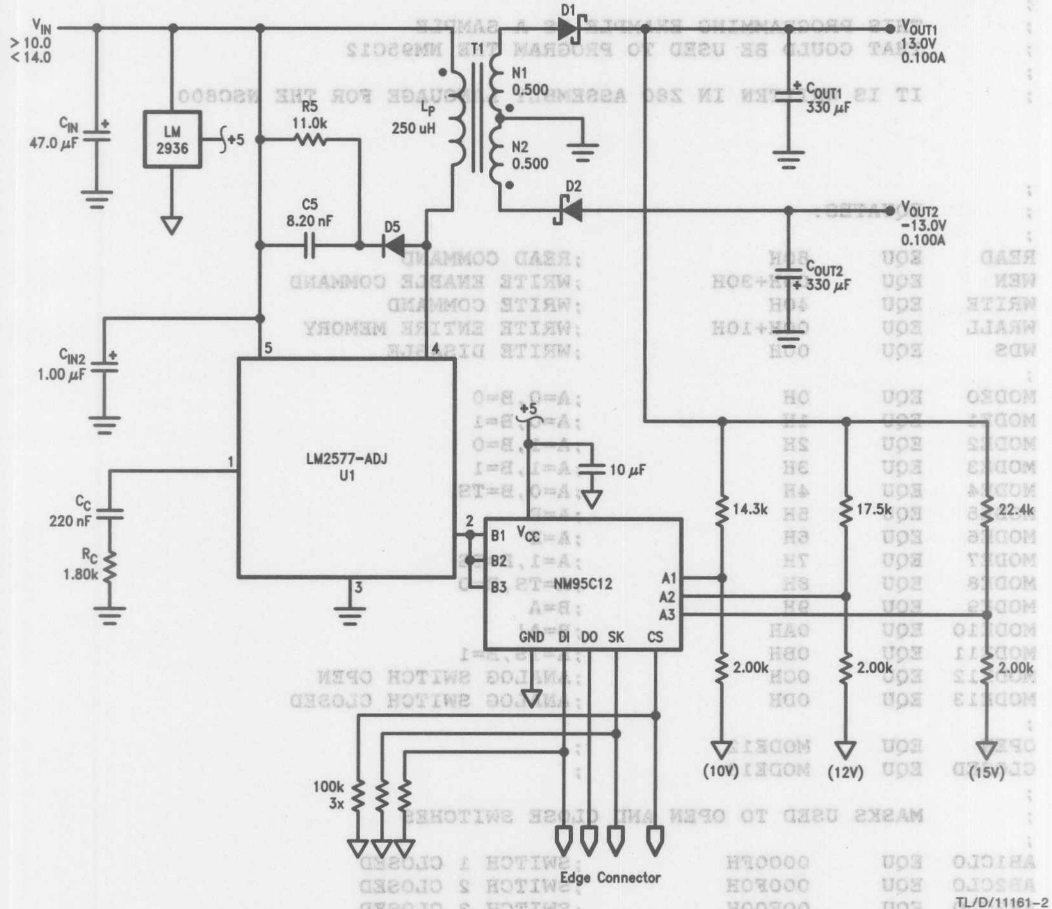

V_IN
> 10.0
< 14.0
C_IN
47.0 µF
LM
2936
+5
R5
11.0k
C5
8.20 nF
D5
T1
L_P
250 uH
N1
0.500
N2
0.500
D1
D2
V_OUT1
13.0V
0.100A
C_OUT1
330 µF
V_OUT2
−13.0V
0.100A
C_OUT2
330 µF
C_IN2
1.00 µF
LM2577-ADJ
U1
C_C
220 nF
R_C
1.80k
+5
10 µF
B1
B2
B3
V_CC
NM95C12
A1
A2
A3
GND
DI
DO
SK
CS
14.3k
17.5k
22.4k
2.00k
2.00k
2.00k
(10V)
(12V)
(15V)
100k
3x
Edge Connector
TL/D/11161-2

FIGURE 2

```
;        IT IS WRITTEN IN Z80 ASSEMBLY LANGUAGE FOR THE NSC800


;
;        EQUATES:
;
READ     EQU      80H                 ;READ COMMAND
WEN      EQU      00H+30H             ;WRITE ENABLE COMMAND
WRITE    EQU      40H                 ;WRITE COMMAND
WRALL    EQU      00H+10H             ;WRITE ENTIRE MEMORY
WDS      EQU      00H                 ;WRITE DISABLE
;
MODE0    EQU      0H                  ;A=0,B=0
MODE1    EQU      1H                  ;A=0,B=1
MODE2    EQU      2H                  ;A=1,B=0
MODE3    EQU      3H                  ;A=1,B=1
MODE4    EQU      4H                  ;A=0,B=TS
MODE5    EQU      5H                  ;A=B
MODE6    EQU      6H                  ;A=B'
MODE7    EQU      7H                  ;A=1,B=TS
MODE8    EQU      8H                  ;A=TS,B=0
MODE9    EQU      9H                  ;B=A
MODE10   EQU      0AH                 ;B=A'
MODE11   EQU      0BH                 ;A=TS,B=1
MODE12   EQU      0CH                 ;ANALOG SWITCH OPEN
MODE13   EQU      0DH                 ;ANALOG SWITCH CLOSED
;
OPEN     EQU      MODE12              ;
CLOSED   EQU      MODE13              ;
;
;        MASKS USED TO OPEN AND CLOSE SWITCHES
;
AB1CLO   EQU      0000FH              ;SWITCH 1 CLOSED
AB2CLO   EQU      000F0H              ;SWITCH 2 CLOSED
AB3CLO   EQU      00F00H              ;SWITCH 3 CLOSED
AB4CLO   EQU      0F000H              ;SWITCH 4 CLOSED
AB1OPN   EQU      0000CH              ;SWITCH 1 OPEN
AB2OPN   EQU      000C0H              ;SWITCH 2 OPEN
AB3OPN   EQU      00C00H              ;SWITCH 3 OPEN
AB4OPN   EQU      0C000H              ;SWITCH 4 OPEN
AB1MSK   EQU      0FFF0H              ;MASK
AB2MSK   EQU      0FF0FH              ;
AB3MSK   EQU      0F0FFH              ;
AB4MSK   EQU      00FFFH              ;
;
;        EEPROM MEMORY LOCATIONS
;
ENABLE   EQU      0                   ;LOC 0,BIT 0=1 IF WR ENABLE
;                                     ;           =0 IF WR DISABLED
SN       EQU      1                   ;SERIAL NUMBER STORAGE
DATE     EQU      32                  ;DATE STORED (DP8570 FORMAT)
PUSCR    EQU      61                  ;SCR LOADED FROM HERE ON POWER UP
SCR      EQU      62                  ;SWITCH CONFIGURATION REGISTER
SRR      EQU      63                  ;SWITCH READ BACK REGISTER (READ ONLY)
```

TL/D/11161–3

```
EEPORT: EQU     00H             ;I/O ADDRESS OF PARALLEL PORT
EE:     EQU     EEPORT          ;SHORTHAND

;       THE PARALLEL PORT IS CONFIGURED AS:
;
;               BIT 0 = DATA OUT      OUTPUT
;               BIT 1 = CLOCK         OUTPUT
;               BIT 2 = CHIP SELECT   OUTPUT
;               BIT 3 = N/U
;               BIT 4 = N/U
;               BIT 5 = N/U
;               BIT 6 = N/U
;               BIT 7 = DATA IN       INPUT
;
;       FOR THIS PROGRAMMING EXAMPLE:
;
;               H  = EEPROM OPCODE
;               L  = EEPROM ADDRESS
;               DE = 16 BIT DATA
;               B  = SHIFT COUNTER
;               C  = PORT DATA STORAGE
;               A  =

        ORG     1000H
;
;
;       MAIN PROGRAM
;
;       THIS SAMPLE PROGRAM SETS SWITCH 1 CLOSED, ALL OTHERS OPEN
;
MAIN:
        LD      H,WEN           ;ENABLE CODE FOR NM95C12
        CALL    WRCMD           ;SEND COMMAND
        LD      DE,AB1CLO+AB2OPN+AB3OPN+AB4OPN
                                ;SWITCH 1 CLOSED
                                ;SWITCH 2 OPEN
                                ;SWITCH 3 OPEN
                                ;SWITCH 4 OPEN
        LD      H,WRITE         ;EEPROM OPCODE
        LD      L,SCR           ;ADDRESS TO WRITE TO
        CALL    WRDATA          ;WR TO SWITCH CONFIGURATION REGISTER
        LD      H,WRITE         ;OPCODE
        LD       L,PUSCR             ;ADDRESS
        CALL    WRDATA          ;WR TO POWER UP SCR
        LD      H,WDS           ;WRITE DISABLE
        CALL    WRCMD           ;DISABLE FURTHER WRITING
        HALT                    ;END OF THIS EXAMPLE
```

TL/D/11161-4

```
;
;       WRITE COMMAND SUBROUTINE
;
;       USE FOR "WEN" AND "WDS" COMMANDS
;
;       WRITES COMMAND TO EEPROM
;       EXPECTS COMMAND TO BE IN H REG
;       EXPECTS ADDRESS TO BE IN L REG
;
WRCMD:
        CALL    PRECK               ;SET CS, CHECK FOR BUSY
        CALL    SHIFT8              ;SEND COMMAND
        CALL    CSLOW               ;SET CS INACTIVE
        RET                         ;DONE
;
;       WRITE DATA SUBROUTINE
;
;       USE FOR "WRITE" AND "WRALL" COMMANDS
;
;       WRITES COMMAND AND DATA TO EEPROM
;       EXPECTS COMMAND TO BE IN H REG
;       EXPECTS ADDRESS TO BE IN L REG
;       EXPECTS DATA    TO BE IN D&E REG
;       ASSUMES EEPROM IS WRITE ENABLED
;
WRDATA:
        CALL    PRECK               ;PRELIMINARY CKS
        CALL    SHIFT8              ;SEND COMMAND
        CALL    SHIFT16             ;SEND DATA
        CALL    CSLOW               ;SET CS INACTIVE
        RET
;
;       THIS ROUTINE DOES A PRECHECK OF THE EEPROM STATUS
;
;       IT SETS CS ACTIVE
;       WAITS AT LEAST 500 NS
;       LOOPS TILL NOT BUSY
;       LEAVES CS ACTIVE, DATA OUT LOW
;       IT EXPECTS PORT DATA IN C REG
;
PRECK:
        PUSH    AF                  ;SAVE
        LD      A,C                 ;GET PORT DATA
        AND     OFDH                ;MASK CLK & DATA LOW
        OR      4                   ;SET CS ACTIVE
        LD      C,A                 ;SAVE
        OUT     (EE),A              ;WRITE TO PORT
PRECK1:
        IN      A,(EE)              ;READ PORT
        AND     80H                 ;ACC = 0 IF BUSY
        JP      Z,PRECK1            ;LOOP UNTILL NOT BUSY
        POP     AF                  ;RESTORE
        RET                         ;ELSE DONE
```

TL/D/11161–5

```
;       IT WRITES TO A PARALLEL PORT WHOSE OUTPUTS ARE CONFIGURED AS:
;
;       BIT 0 = DATA
;       BIT 1 = CLOCK
;       BIT 2 = CHIP SELECT (ACTIVE HI)
;
;       IT ASSUMES CS IS ACTIVE
;       IT SENDS A START BIT (LOW TO HI TRANSITION)
;       THEN IT SENDS DATA MSB FIRST
;       IT EXPECTS PORT DATA IN C REG
;       IT DESTROYS H,L,B
;
SHIFT8:
        PUSH    AF              ;SAVE
        CALL    STRTBT          ;SEND START BIT
        LD      B,7             ;LOOP COUNTER
        LD      A,L             ;ADDRESS
        OR      H               ;COMBINE WITH OPCODE
        LD      L,A             ;SAVE IN L
SNDBIT:
        LD      A,C             ;GET PORT CONTENTS
        AND     OFDH            ;MASK CLK AND DATA LOW
        LD      C,A             ;SAVE
        RLC     L               ;CK MSB OF DATA
        JP      NC,SH8LP        ;IF 0, DO NOTHING
        OR      1               ;ELSE SET DATA BIT HI
SH8LP:
        OUT     (EE),A          ;SEND DATA WITH CLK=0
        OR      2               ;CLK=1
        OUT     (EE),A          ;SEND IT
        AND     OFDH            ;CLK=0
        OUT     (EE),A          ;SEND IT
        DEC     B               ;LOOP ONE FEWER TIMES
        JP      NZ,SNDBIT       ;LOOP UNTILL DONE
;
;       ELSE, WE HAVE SENT 8 BITS
;
        POP     AF              ;RESTORE
        RET                     ;
```

TL/D/11161–6

4

```
;
;       BIT 0 = DATA
;       BIT 1 = CLOCK
;       BIT 2 = CHIP SELECT (ACTIVE HI)
;
;       IT ASSUMES CS IS ACTIVE
;       <DE> HOLDS DATA TO BE SENT (MSB FIRST)
;
SHIFT16:
        PUSH     AF
        PUSH     DE                ;
        LD       B,7               ;LOOP COUNTER
SNDBT:
        LD       A,C               ;GET PORT CONTENTS
        AND      OFDH              ;MASK CLK AND DATA LOW
        LD       C,A               ;SAVE
        RLC      D                 ;CK MSB OF FIRST BYTE OF DATA
        JP       NC,SH16LP         ;IF 0, DO NOTHING
        OR       1                 ;ELSE SET DATA BIT HI
SH16LP:
        OUT      (EE),A            ;SEND DATA WITH CLK=0
        OR       2                 ;CLK=1
        OUT      (EE),A            ;SEND IT
        AND      OFDH              ;CLK=0
        OUT      (EE),A            ;SEND IT
        DEC      B                 ;LOOP ONE FEWER TIMES
        JP       NZ,SNDBT          ;LOOP UNTILL DONE
;
;       ELSE, WE HAVE SENT FIRST 8 BITS
;
        LD       B,7               ;LOOP COUNTER
SNDBT1:
        LD       A,C               ;GET PORT CONTENTS
        AND      OFDH              ;MASK CLK AND DATA LOW
        LD       C,A               ;SAVE
        RLC      E                 ;CK MSB OF SECOND BYTE OF DATA
        JP       NC,SH16LP1        ;IF 0, DO NOTHING
        OR       1                 ;ELSE SET DATA BIT HI
SH16LP1:
        OUT      (EE),A            ;SEND DATA WITH CLK=0
        OR       2                 ;CLK=1
        OUT      (EE),A            ;SEND IT
        AND      OFDH              ;CLK=0
        OUT      (EE),A            ;SEND IT
        DEC      B                 ;LOOP ONE FEWER TIMES
        JP       NZ,SNDBT1         ;LOOP UNTILL DONE
;
;       ELSE, WE HAVE SENT ALL 16 BITS
;
        POP      DE                ;
        POP      AF                ;RESTORE
        RET                        ;
```

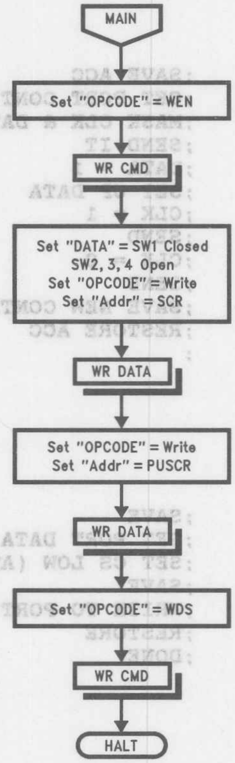
TL/D/11161-7

```
;
;       SEND A START BIT
;
STRTBT:
        PUSH    AF              ;SAVE ACC
        LD      A,C             ;GET PORT CONTENTS
        AND     0FCH            ;MASK CLK & DATA LOW
        OUT     (EE),A          ;SEND IT
        OR      1               ;DATA = 1
        OUT     (EE),A          ;SET UP DATA
        OR      2               ;CLK = 1
        OUT     (EE),A          ;SEND
        AND     0FDH            ;CLK = 0
        OUT     (EE),A          ;SEND
        LD      C,A             ;SAVE NEW CONTENTS IN C
        POP     AF              ;RESTORE ACC
        RET                     ;
;
;       SET CS LOW (INACTIVE)
;
;       ALTERS C REG
;
CSLOW:
        PUSH    AF              ;SAVE
        LD      A,C             ;GET PORT DATA
        AND     0F8H            ;SET CS LOW (AND DATA AND CLK)
        LD      C,A             ;SAVE
        OUT     (EE),A          ;WRITE TO PORT
        POP     AF              ;RESTORE
        RET                     ;DONE

        END
```

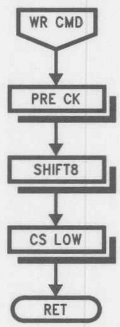
TL/D/11161-8

Main Loop

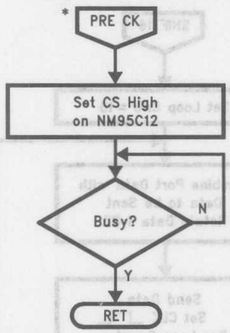


TL/D/11161–9

Write Command to NM95C12

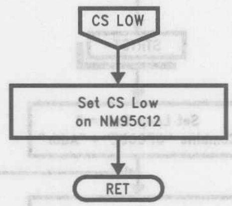


TL/D/11161–10



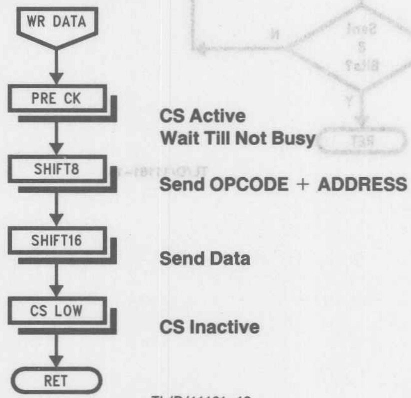
TL/D/11161-11

*Pre-check of NM95C12 sets CS active. Returns when NM95C12 not busy.



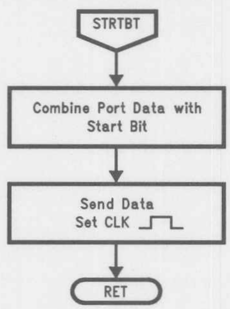
TL/D/11161-12

Write Data (16 Bits) to NM95C12

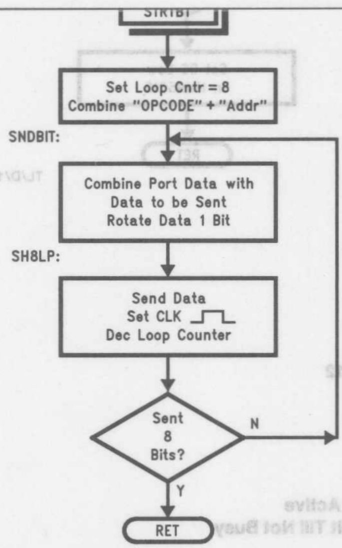


TL/D/11161-13

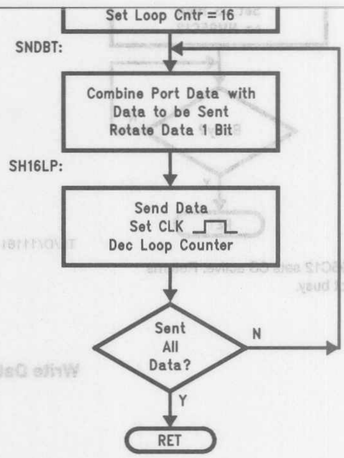
Send Start Bit to NM95C12



TL/D/11161-14



TL/D/11161-15



TL/D/11161-16

Programmable Switches for Analog Applications

INTRODUCTION

National's NM95C12 EEPROM programmable switch occupies a unique niche in the switch marketplace. Consisting of a 1024-bit serial input EEPROM with 8 programmable switches, the output can provide either an analog switch or TTL compatible logic functions.

The combination of switch performance and the flexibility offered in the ability to software reconfigure the switching function makes the NM95C12 an excellent device for analog systems requiring switching or multiplexing. Often calibration sequences or multiplexing functions have either required using several IC's or manually shorting and opening printed circuit board connections, until the availability of the NM95C12.

However, the limited analog range of the NM95C12 makes it difficult to use for general analog functions. In order to capitalize on the full capabilities of programmable switches, it is important to understand the appropriate design techniques in level shifting, increasing the output drive capability, and increasing the output signal range. The focus of this application note is to summarize general circuits that perform this function, and thereafter provide a practical transducer measurement system example. The discussion will be solely devoted to extending the use of the NM95C12's switches function, and not on the actual software programming or operation of the IC.

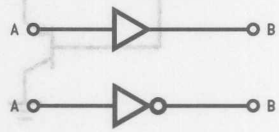
GENERAL DESCRIPTION

A detailed description of the overall operation of the NM95C12 can be found in AN-735, "Understanding National's NM95C12 EEPROM with Programmable Switches", or the NM95C12 data sheet. However, for the sake of completeness, the NM95C12 consists of a 61-word x 16-bit EEPROM array, a 16-bit Initial Switch Register, a 16-bit Switch Configuration Register, a 16-bit Switch Readback Register, four identical blocks of switch logic, programming and power-up circuits and control logic. Essentially, the NM95C12 programmable switch can be easily configured, and reconfigured, for applications including both analog and digital switching functions. 60 internal addresses are available to reconfigure the switch settings on the fly. Upon power-up the Initial Switch Register, address 61, provides a defined set-up state. This operational feature is extremely valuable since it provides an established initial condition for the system.

SWITCH DETAILS

Each switch pair can be configured for either logic functions, or as an analog switch. Functional block details relating control of the switches to the input control logic can be found in Table I of the NM95C12 data sheet. Basically, the logic switch configurations are at standard TTL levels. Also, the analog switch configurations can be looked at as standard MUX switches. Since this note specifically focuses on extending the operating voltage range of the analog switches, the emphasis will be on the analog switches. *Figure 1* summarizes the salient operating features of the switch pairs.

Logic Function

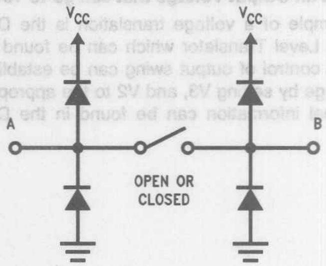


TL/D/11188–1

Input Leakage $\pm 2.5\ \mu A$ max

TTL Level Input/Output

Switch Functions



TL/D/11188–2

R_{ON} 200Ω max

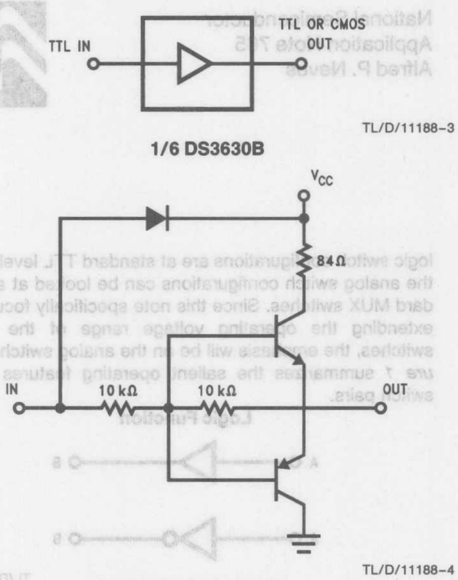
R_{OFF} 10 MΩ min

$(+0.7) \geq V_{OUT} \geq (V_{CC} - 0.7V)$

FIGURE 1. The NM95C12 can be Programmed to Configure either Logic Function or an Analog Switch

LEVEL SHIFTING AND EXTENDING THE SWITCHES RANGE

In considering level switching and enhancement of the voltage range for the NM95C12, it is logical to examine some simple level translations that can be solved with commercially available IC's. Examples of simple translation circuits includes the DS1630B Hex CMOS Compatible Buffer shown in *Figure 2*. Where simple translation of TTL output signals to higher levels of output voltage is required (such as CMOS compatible signals), used at the output of logic configured NM95C12 switch, the DS1630B represents a simple solution.



Equivalent Circuit

FIGURE 2. The DS1630B/DS3630B is a Hex CMOS Buffer Amplifier. It Features Low Power Consumption, and an Output Voltage that can go to 16V (V_{CC}).

An example of a voltage translation is the DS8800 Dual Voltage Level Translator which can be found in *Figure 3*. Custom control of output swing can be established over a 31V range by setting V3, and V2 to the appropriate values. Additional information can be found in the DS8800 data sheet.

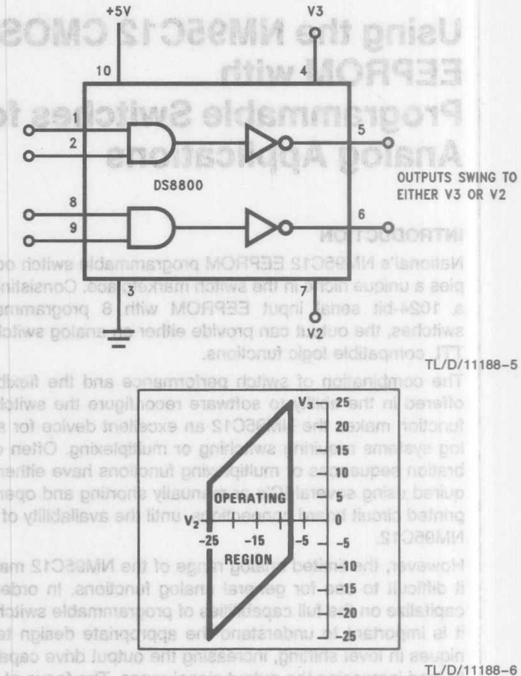


FIGURE 3. The DS8800 is a Dual Voltage Translator that is useful for Programming MOS Type Memory, Establishing Bias Voltages, and Driving Transducers. Output Swing is Limited to 31V.

Figures 4 through *10* illustrate some useful translation circuits that use discrete components to achieve higher output drive than typical monolithic IC's. The circuit in *Figure 4* is similar in functionality to the DS8800. However, wider output swings (limited to BVCeo of the output transistor), and larger sink/source current ability is achieved.

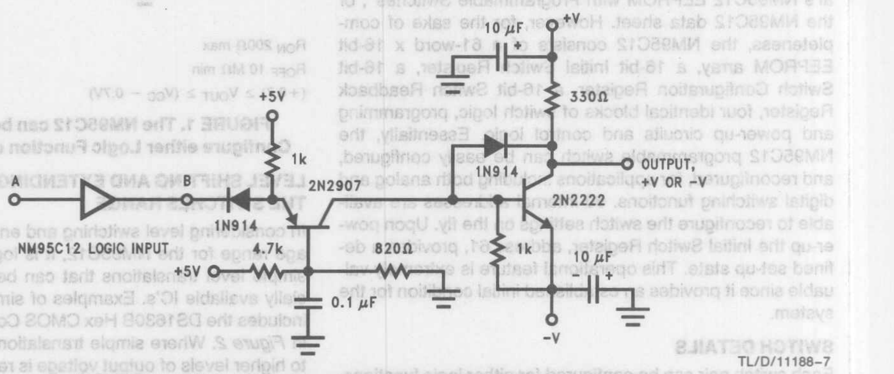
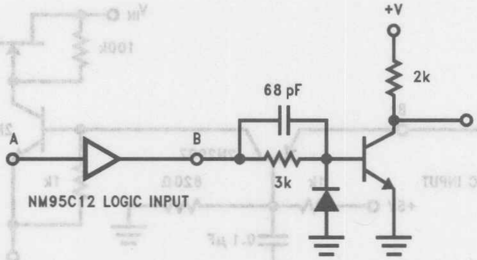
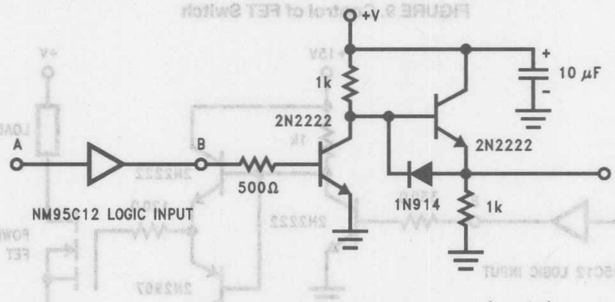


FIGURE 4. −V to +V Voltage Translation, from TTL Input Signal



TL/D/11188-8

FIGURE 5. A Simple 0 → +V (+V Typically is 3V → +18V) Level Translation Stage. $I_{SOURCE} > I_{SINK}$



$I_{SINK} > I_{SOURCE}$

TL/D/11188-9

FIGURE 6. High Output Current Sink Level Translation Stage—Excellent for Transducer Bridge Drive

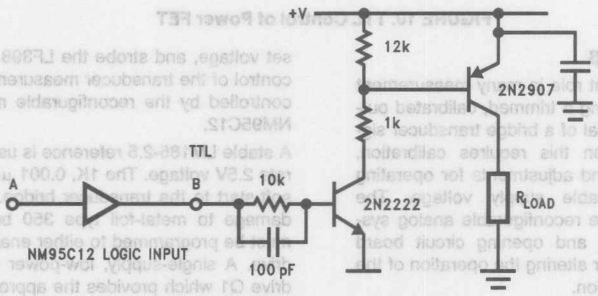


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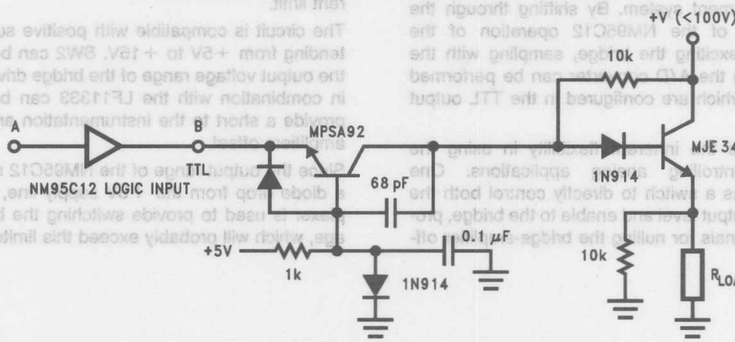
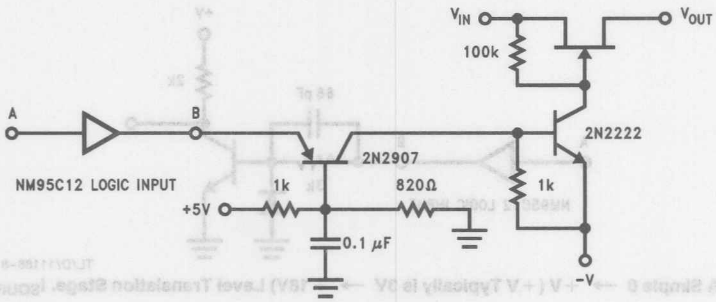
FIGURE 7. A Simple 0V → +V Switch, from TTL Input



TL/D/11188-11

FIGURE 8. 0V to High Voltage Translation Circuit, from TTL Input



TL/D/11188-12

FIGURE 9. Control of FET Switch

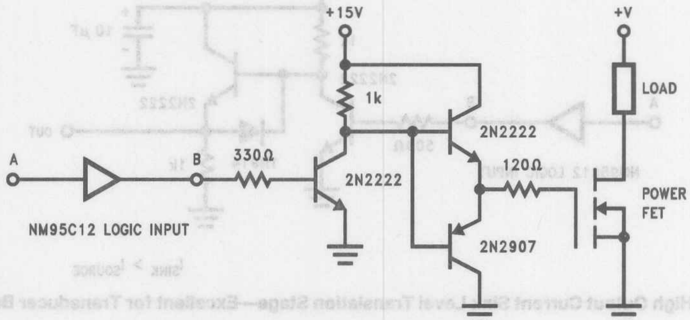


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FIGURE 10. TTL Control of Power FET

TWO PRACTICAL EXAMPLES

Bridge circuits play a dominant role in many measurement applications. Typically, providing a trimmed, calibrated output response is usually the goal of a bridge transducer signal processing system. Often this requires calibration, switching for it's operation, and adjustments for operating conditions related to available supply voltage. The NM95C12 provides a software reconfigurable analog system, where manual shorting and opening circuit board traces is not required for either altering the operation of the system, or performing calibration.

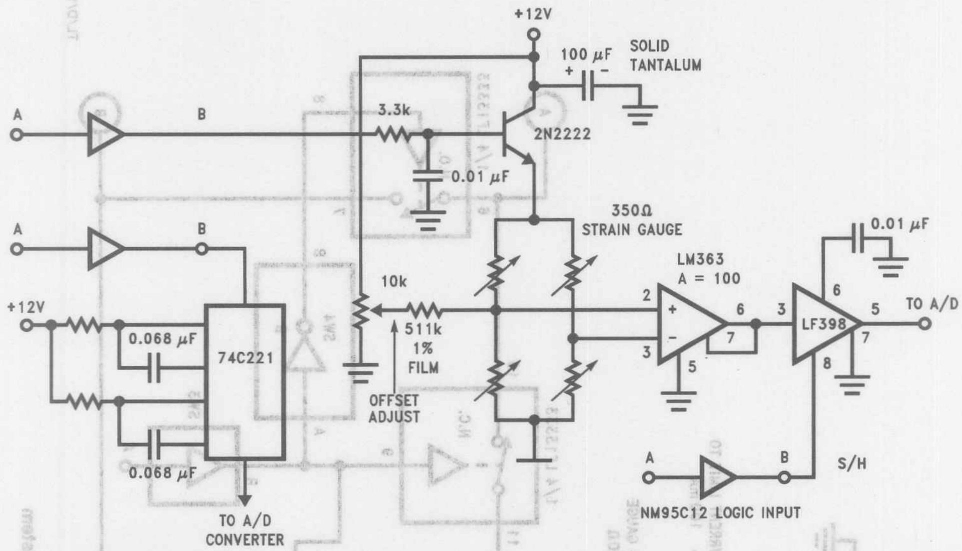
Figure 9 shows how the NM95C12 can be used to control a transducer measurement system. By shifting through the 61-word sequence of the NM95C12 operation of the bridge—pulsing or exciting the bridge, sampling with the LF398, and strobing the A/D converter can be performed with the switches, which are configured in the TTL output mode.

Figure 10 illustrates the inherent flexibility in using the NM95C12 for controlling analog applications. One NM95C12 is used as a switch to directly control both the excitation voltage output level and enable to the bridge, provide TTL control signals for nulling the bridge-amplifier offset voltage, and strobe the LF398 sample/hold. Complete control of the transducer measurement system can now be controlled by the reconfigurable memory contents of the NM95C12.

A stable LM185-2.5 reference is used to generate an accurate 2.5V voltage. The 1K, 0.001 μF, 20K circuit provides a soft-start to the transducer bridge. This prevents potential damage to metal-foil type 350 bridge transducers. SW1 must be programmed to either enable or disable the bridge drive. A single-supply, low-power dual op-amp is used to drive Q1 which provides the appropriate bridge drive. Reliability is enhanced by including a 100 mA short circuit current limit.

The circuit is compatible with positive supply voltages extending from +5V to +15V. SW2 can be enabled to alter the output voltage range of the bridge drive. SW3 and SW4, in combination with the LF11333 can be programmed to provide a short to the instrumentation amplifier to null the amplifiers offset.

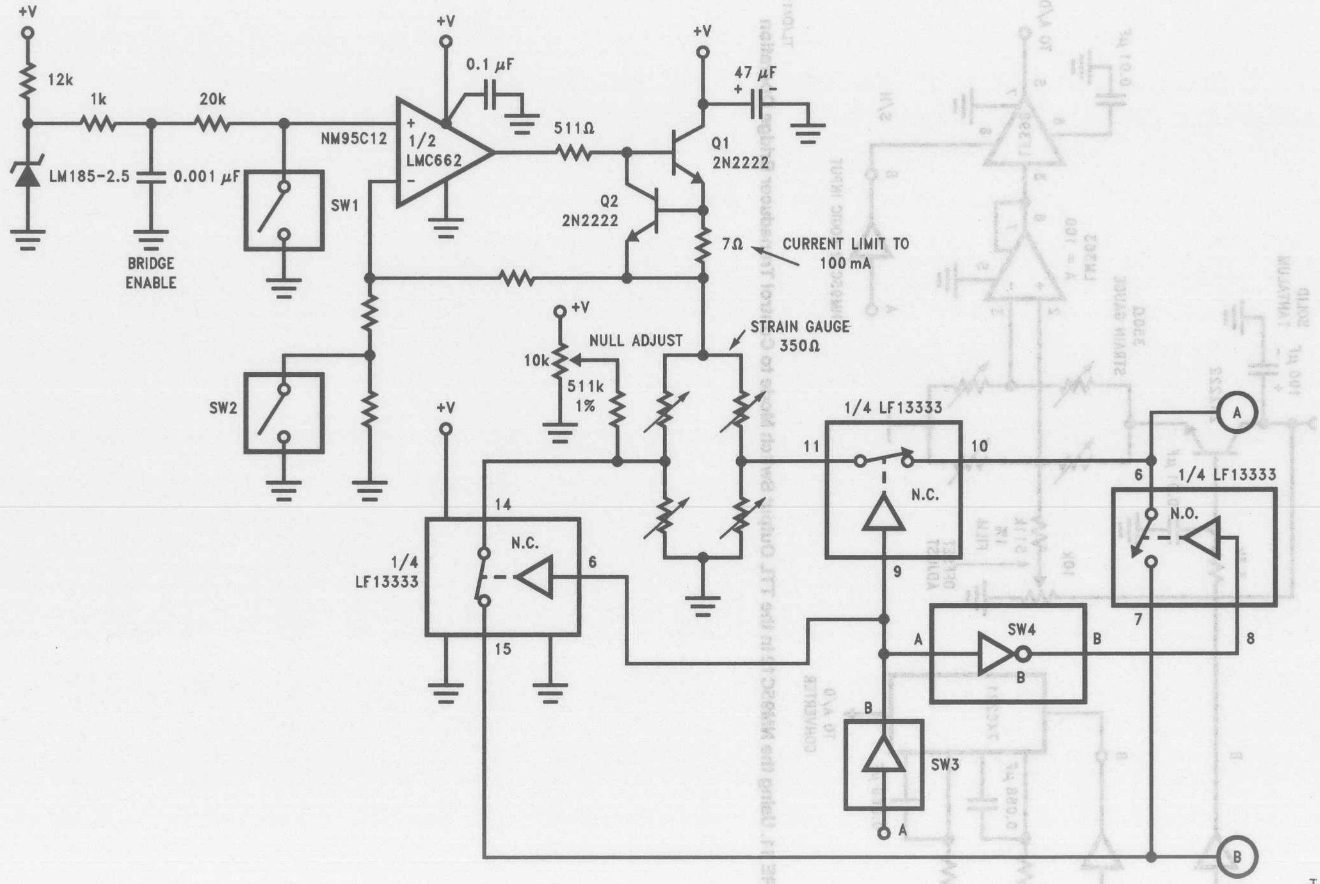
Since the output range of the NM95C12 switch is limited to a diode drop from the +5V supply line, a LF13333 multiplexer is used to provide switching the bridge output voltage, which will probably exceed this limited voltage range.



TL/D/11188–14

FIGURE 11. Using the NM95C12 in the TTL Output Switch Mode to Control Transducer Bridge Operation

4



SWX are Internal Switches to the NM95C12

FIGURE 12. Transducer Measurement System

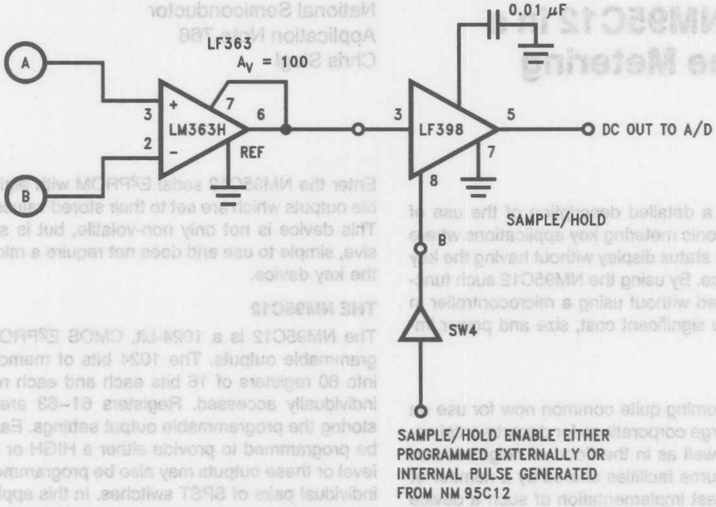


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FIGURE 12. Transducer Measurement System (Continued)

Using the NM95C12 in a Stand Alone Metering Device

National Semiconductor
Application Note 766
Chris Siegl

ABSTRACT

This application gives a detailed description of the use of the NM95C12 in electronic metering key applications where it is desirable to have a status display without having the key connected to any device. By using the NM95C12 such functionality can be obtained without using a microcontroller in the key. This can have significant cost, size and power impact.

INTRODUCTION

Metering keys are becoming quite common now for use on copying machines in large corporations for departmental accounting purposes as well as in the flood of neighborhood copy centers and resource facilities shared by a number of businesses. The simplest implementation of such a device is a simple mechanical counter with an advance solenoid—as each copy is made a pulse advances the counter. This approach suffers a number of drawbacks including low reliability, easy to tamper with, bulky and unable to itemize between different uses or equipment. These types of devices are no longer just used for copying machines—fax machine usage, word processor usage, plotters, and laser printers are now becoming part of the shared resources of a corporation or among a number of businesses as well as such services being incorporated into the neighborhood copy center. While the mechanical counter could still be used in such applications where the device under use could increment the counter at different rates depending on the type of usage, a different counter could be used for each service; generating an itemized receipt for the user becomes very cumbersome.

By using a non-volatile memory in the key device an itemized list can be kept of the services used. The value of the services used could also be tracked and the key terminated when a certain limit is reached. The key device could function like a debit card where the user gets a certain amount of credit stored in his card—when it is all used up he must go back for more at which point a cash register or other device with a printer and a receptacle for the key device would print an itemized list of usage and optionally erase the memory and store a new credit amount. The disadvantage of this approach when compared to the mechanical counter is the lack of an indication of the remaining credit or usage to the user. One way to solve this problem is to include a display on the device being used to display the current credit information. This has the disadvantage that the user must have the key device plugged into a service device to find his credit status. Another approach is to include a microcontroller in the key device along with a display, a battery and a switch to activate the display. If the battery fails, information in the key is lost. By using serial E^{2}PROM memory devices such as the NM9306, NM93Cxx or NM93CSxx families solves the information retention problem when the battery fails, but we still need the microcontroller if the key device is to have an active display without connection to another device.

Enter the NM95C12 serial E^{2}PROM with eight programmable outputs which are set to their stored values on power up. This device is not only non-volatile, but is small, inexpensive, simple to use and does not require a microcontroller in the key device.

THE NM95C12

The NM95C12 is a 1024-bit, CMOS E^{2}PROM with 8 programmable outputs. The 1024 bits of memory are divided into 60 registers of 16 bits each and each register can be individually accessed. Registers 61–63 are dedicated to storing the programmable output settings. Each output may be programmed to provide either a HIGH or a LOW output level or these outputs may also be programmed to form four individual pairs of SPST switches. In this application we will only be programming these pins as HIGH or LOW outputs but there are many other applications where a SPST switch or switches would be useful.

Other features of the NM95C12 include a very low operating current (less than 4 mA), software write protection, self timed write cycle (erase cycles not necessary) with an endurance of over 40,000 writes per register and at least 10 year data retention.

Interfacing to the NM95C12 is done through the on-board MICROWIRE™ port; this port consists of four signal lines: a serial clock (SK), serial data input (SI), serial data output (SO), and chip select (CS). MICROWIRE is supported in hardware in the COP400, COP800 and HPC™ microcontroller families. MICROWIRE can also be easily implemented on most microncontrollers and microprocessors in software. The TP3064 and TP3065 implement a MICROWIRE hardware interface to various standard microprocessors.

DISPLAY INTERFACE

The NM95C12 has 8 programmable outputs. The switch configuration register (SCR) controls these outputs in pairs, four bits per pair. Table I shows the different switch configurations possible for each pair. In this application we are only interested in modes 0, 1, 2 and 3. Because the NM95C12 has a much greater current sinking capability than sourcing we will configure our LED displays with their cathodes to the output port. A LOW output results in a lit LED. *Figure 1* shows a bar graph display being driven by the NM95C12. A single resistor SIP can be used to limit the current to the LEDs. The configuration register looks like *Figure 2* with a, b, c . . . h representing the LED segments. To light a particular segment the appropriate bit in the SCR register must be set to 0. This register is set to the contents of the word stored in the E^{2}PROM's location 61 at power-up. The SCR register itself is located at address 62 and can be written to directly without affecting the E^{2}PROM location 61 and the new contents of the SCR register will be lost on power-down. At the next power-up the contents of location 61 will again be stored in the SCR.

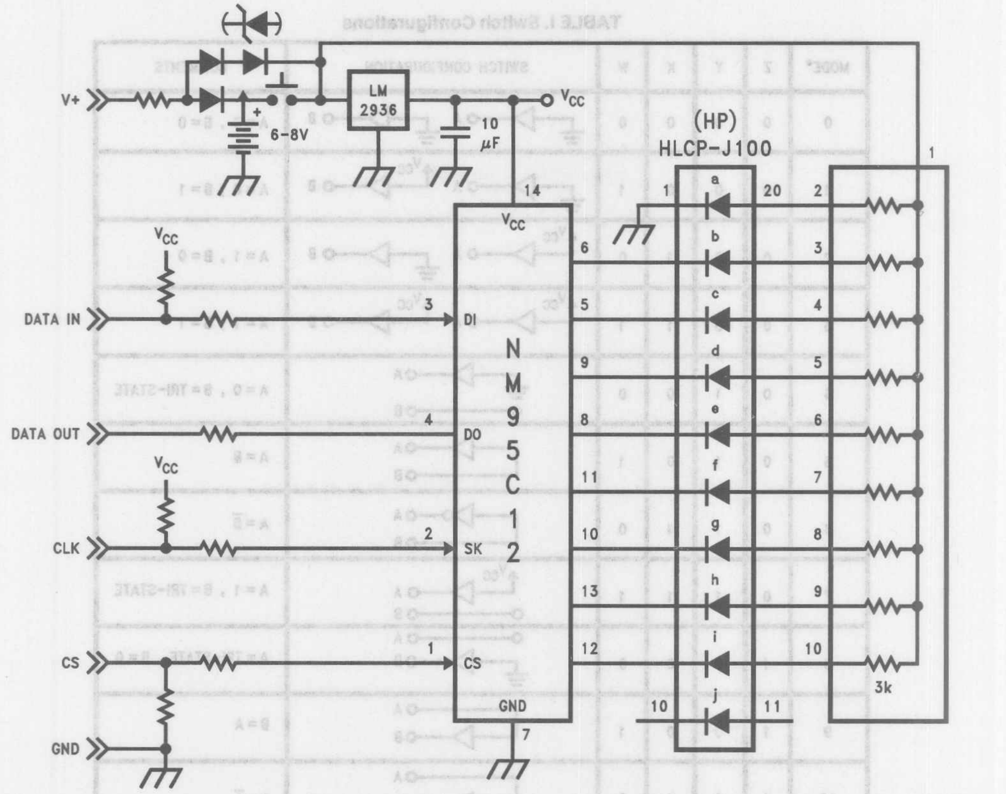

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FIGURE 1

Switch Configuration Register (SCR)

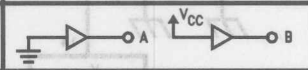
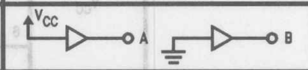
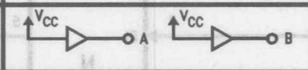
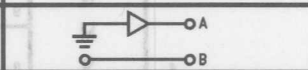
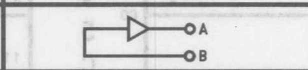
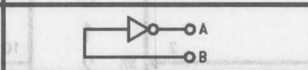
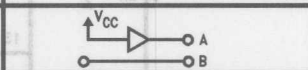
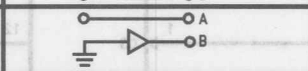
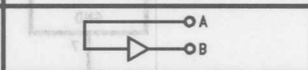
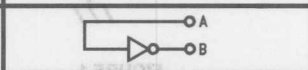
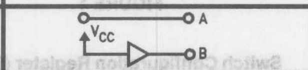
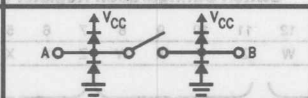
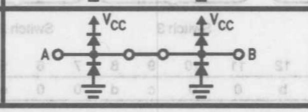
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Z	Y	X	W	Z	Y	X	W	Z	Y	X	W	Z	Y	X	W
Switch 4				Switch 3				Switch 2				Switch 1			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	a	b	0	0	c	d	0	0	e	f	0	0	g	h

FIGURE 2. SCR Configured to Drive Bar Graph
(a 0 in a, b . . . h turns on appropriate segment)

The circuit in *Figure 1* uses some tricks to maximize the battery life. The LM2936 (low dropout; ultra-low quiescent current 5V regulator) was used to regulate the battery voltage down to 5V for the NM95C12. By bypassing the regulator for the +V connection to the resistor SIP the current through the regulator only feeds the NM95C12 which in its quiescent state (with all inputs at CMOS logic levels) is <50 μA the dropout voltage of the LM2936 is <0.1V. To have the LEDs operate correctly it is important to keep the battery voltage under 8V to 9V otherwise the LEDs which should be off will get turned on through the protection diodes (see modes 12 and 13 of Table I) not to mention the increase in current discharging the battery. Another approach would be to power the LEDs from the regulated +5V. Now the thing to watch out for is the current limit of the LM2936; exceeding 65 mA could force the regulator to go into current limit.

TABLE I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = TRI-STATE
5	0	1	0	1		A = B
6	0	1	1	0		$A = \overline{B}$
7	0	1	1	1		A = 1 , B = TRI-STATE
8	1	0	0	0		A = TRI-STATE , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		$B = \overline{A}$
11	1	0	1	1		A = TRI-STATE , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

All the circuits in this application note use very low current Hewlett Packard displays (they are specified for operation at 1 mA per segment) to maximize battery life. Other displays at higher currents can be used but care must be exercised not to exceed the current capabilities of the LM2936 as well as the power dissipation capabilities of the NM95C12 especially if the surface mount package is used at higher temperatures. Another side effect of higher currents in the LEDs is the V_{OL} specification is 0.4V at an I_{OL} of 2.1 mA but will rise with higher I_{OL}s (typically stays well under 1V at 10 mA).

Instead of using a bar graph individual LEDs could be used in much the same manner. The length of bar graph lit or number of LEDs lit would show the amount of credit remaining. Another approach would be to use a 7 segment display. *Figure 3* shows such a circuit. The button is pressed when the user wishes to see the display. There is a diode bypass of the push button switch so the display is active while the key is plugged into the device under use. The user can monitor his remaining credit while operating the device. The battery is being charged whenever the key is plugged into a device. If the battery should ever go too low to operate, the user just plugs the key into a device for a while to recharge—the contents of the E^2PROM are not lost. The rechargeable battery could be replaced with a 9V transistor battery (typical voltage on these is 7V to 8V) which will give operating life of multiple months if checked only intermittently. No data would be lost during battery changes. *Figure 3* shows how the key would be configured using the transistor battery. Table II shows the bit combinations for the SCR register to generate the digits 0 to 9. Notice with the 7 segment display we no longer can use a resistor SIP because segment LEDs are all tied to a common cathode. Resistors in this configuration are available in DIPs as well as SOIC.

Applications desiring two digits (credit can now be displayed as percent remaining) can be implemented with two MM74HC4511 display decoder/drivers as shown in *Figure 4*. The MM74HC4511s have a quiescent current of $<80\ \mu A$ maximizing battery life and are available both in DIP as well as SOIC packages. The MM74HC4511 has a maximum supply voltage of 6V so it should be operated from +5V regulated supply as shown in *Figure 5*. Table III shows how the BCD (binary coded decimal) data is configured in the SCR register to display the two digits.

TABLE II

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	a	b	0	0	c	d	0	0	e	f	0	0	g	dp	
0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0
0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	1	0	0	1	0	0	0	1	0	2
0	0	1	1	0	0	1	1	0	0	0	0	0	0	1	0	3
0	0	0	1	0	0	1	0	0	0	0	1	0	0	1	0	4
0	0	1	0	0	0	1	1	0	0	0	1	0	0	1	0	5
0	0	1	0	0	0	1	1	0	0	1	1	0	0	1	0	6
0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	7
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	0	8
0	0	1	1	0	0	1	0	0	0	0	1	0	0	1	0	9

TL/D/11189–3

4

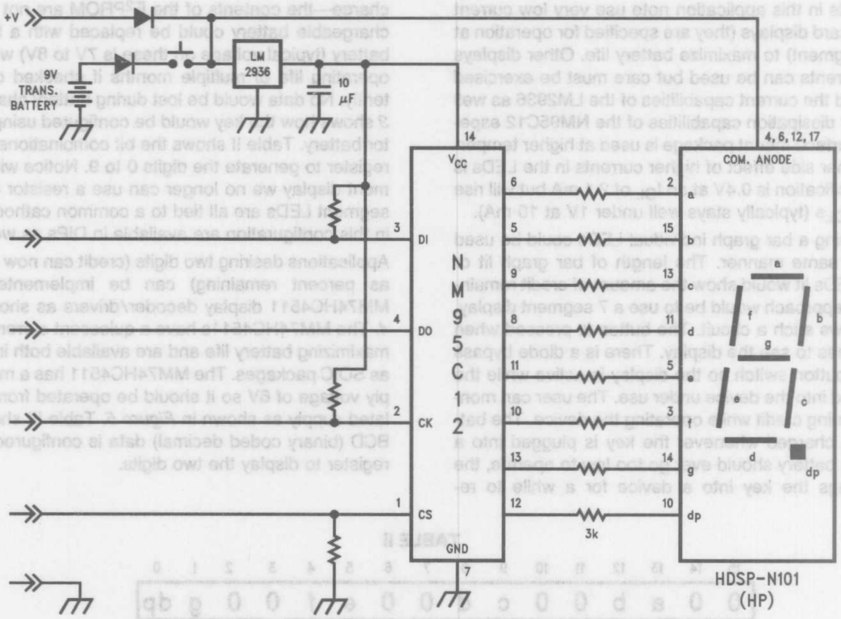

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FIGURE 3

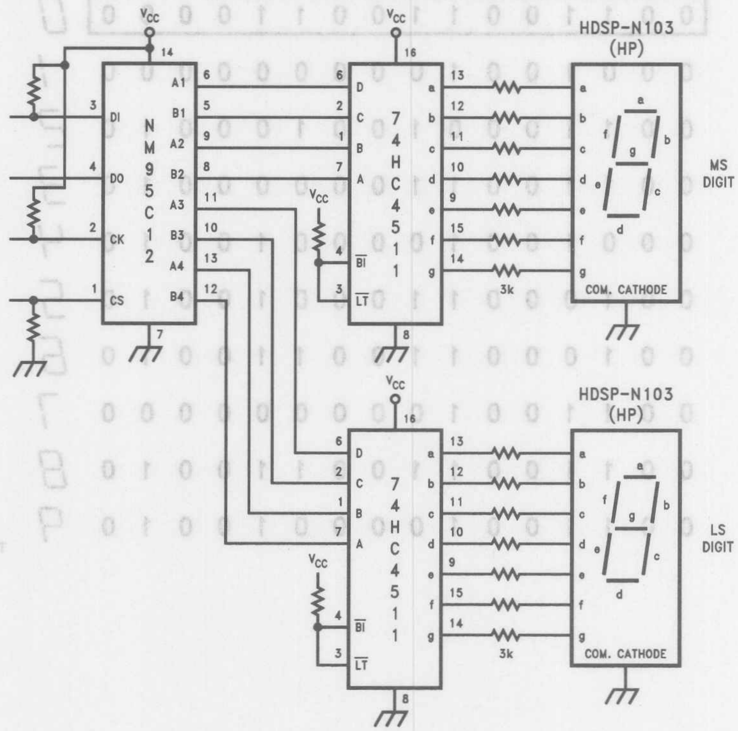

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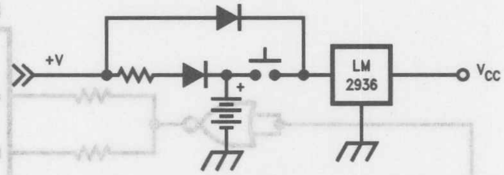
FIGURE 4



TL/D/11189–5

FIGURE 5

TABLE III

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	D	C	0	0	B	A	0	0	D	C	0	0	B	A
MS DIGIT								LS DIGIT							

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	01
0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	43
0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	1	95

TL/D/11189–6

If there is a need to display the number 100 as well, this can be accomplished with the addition of just one quad NOR gate as shown in *Figure 6*. Here we get a little tricky. By adding some gating to the two most significant bits of the most significant digit a coding can be worked out that gives a zero code to the most significant digit driver at the same time as driving through another gate the hundreds digit. *Figure 7* shows the logic along with a table of the states. If the 2 most significant bits of the most significant digit are inverted before going to the SCR register the right numbers will be displayed. To display 100 the SRC is loaded with all zeros. Table IV shows some example numbers.

MODULE INTERFACE

The metering device or key must connect to the service device through some type of connector. The simplest approach is to bring out the MICROWIRE port through a connector to a processor or microcontroller in the service device. The MICROWIRE port consists of four signal lines; a serial clock (SK), serial data input (SI), serial data output (SO), and the chip select (CS). When CS is LOW the chip is powered down into standby mode (outputs A1 through A4 and outputs B1 through B4 are still driven even while in standby) and accesses on the MICROWIRE port are disabled. So while the metering device is unplugged from the service device we want this signal low, therefor this signal has a pull down resistor. To begin an access to the NM95C12 the CS is first set high by the service device then a high start bit is on DI and clocked into the NM95C12 by a low to high transition on SK (see *Figure 8*) the start bit is then followed by opcode and address (see Table V) with SK low to high transitions for each bit. In the case of a read instruction, subsequent toggling of the SK line causes the addressed data to be shifted out on DO. Data should not be sampled on DO on the low to high transition of SK as this is when the bit is shifted out. On write operations they must be preceded by the write enable instruction (WEN). In the write instruction (WRITE) the data follows right after the address. (see *Figure 9*).

The MICROWIRE interface is supported in hardware on the COP400, COP800 and HPC microcontroller families. MICROWIRE can also be easily implemented on most microcontrollers and processors in software. Application Note AN-507 "Using the NMC93CSxx family" covers the details of how to communicate with these types of serial memory devices from various microcontrollers. The TP3464 and TP3465 implement a MICROWIRE hardware interface to various standard microprocessors.

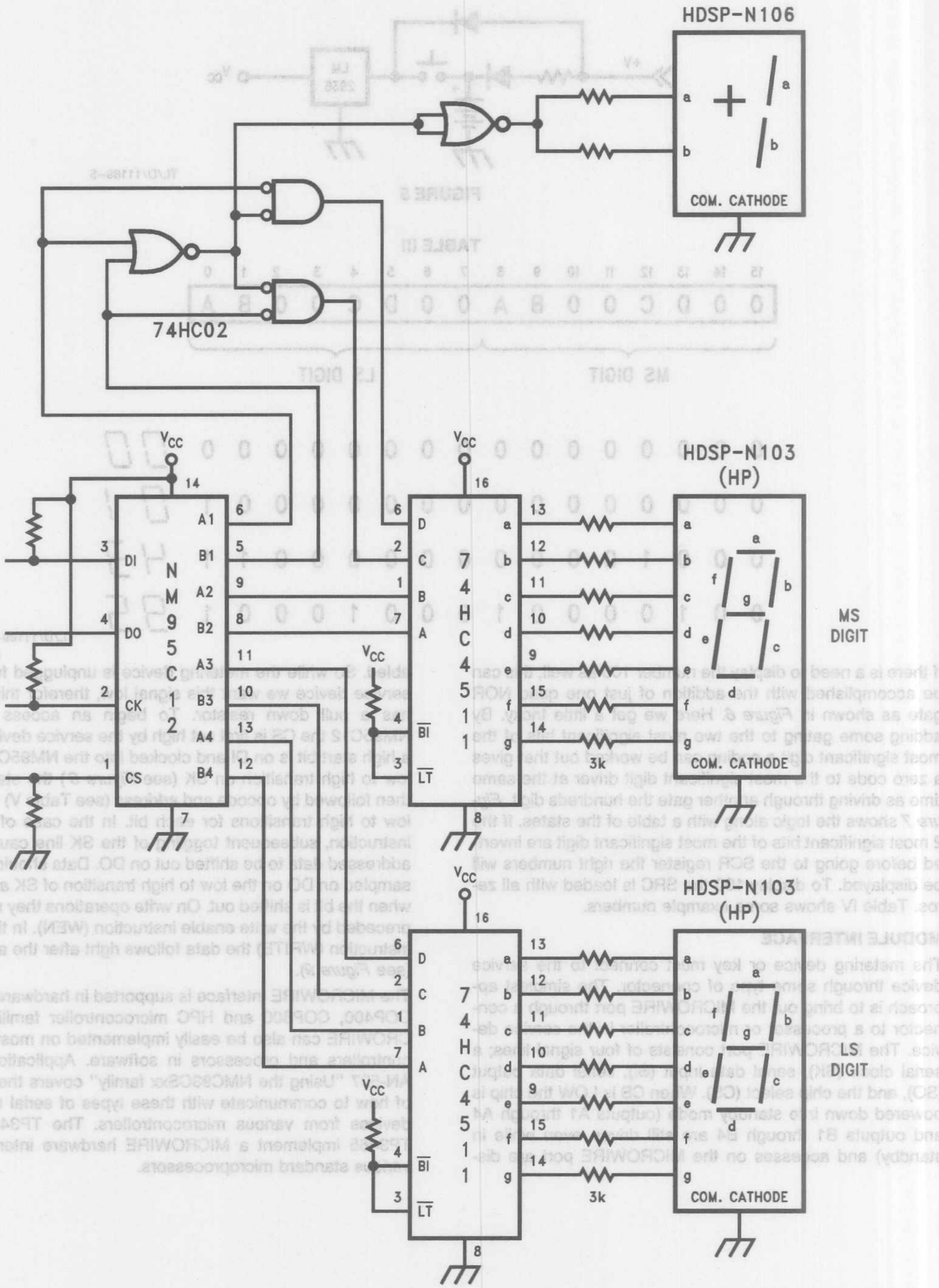
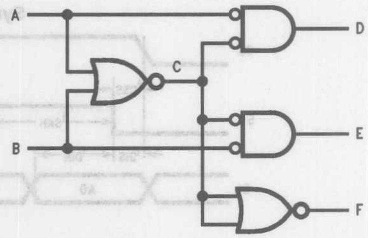

HDSP-N106
a
b
COM. CATHODE
74HC02
V_{CC}
14
3
DI
4
DO
2
CK
1
CS
N M 9 5 C 1 2
A1
B1
A2
B2
A3
B3
A4
B4
7
6
5
9
8
11
10
13
12
16
D
C
B
A
$\overline{BI}$
$\overline{LT}$
7 4 H C 4 5 1 1
13
12
11
10
9
15
14
8
3k
HDSP-N103
(HP)
MS
DIGIT
LS
DIGIT
TL/D/11189-7

FIGURE 6

If there is a need to minimize the number of contacts in the connector from the metering device to the service device, Application Note AN-423 "The NMC9346—An Amazing Device" gives the details to implementing power and MICROWIRE signals over just two connections.

CONCLUSION

This application note describes a number of approaches to metering devices from the very simple to the complex. If more E²PROM is required it is available in the NM93Cxx family in 8-pin DIPs and SOIC in various sizes. With the features of very low power, small size, and low cost as well as the simplicity of interface to most processors and controllers already part of the panel interface of most server devices, the implementation of this type of product is very easy.



TL/D/11189-8

A	B	C	D	E	F
0	0	1	0	0	0
1	0	0	0	1	1
0	1	0	1	0	1
1	1	0	0	0	1

FIGURE 7

TABLE IV

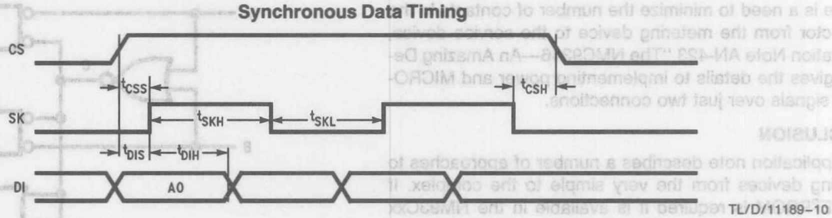
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	$\overline{D}$	$\overline{C}$	0	0	B	A	0	0	D	C	0	0	B	A	
MS DIGIT								LS DIGIT								
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	00
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	01
							•									
							•									
							•									
0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	89
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	100

TL/D/11189-13

TABLE V. NMC95C12 Instructions

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Reads data stored in memory, starting at specified address
WEN	1	00	11XXXX		Write enable must precede all programming modes
WRITE	1	01	A5–A0	D15–D0	Writes register
WRALL	1	00	01XXXX	D15–D0	Writes all registers
WDS	1	00	00XXXX		Disables all programming instructions

Synchronous Data Timing



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Instruction Sequence

READ:

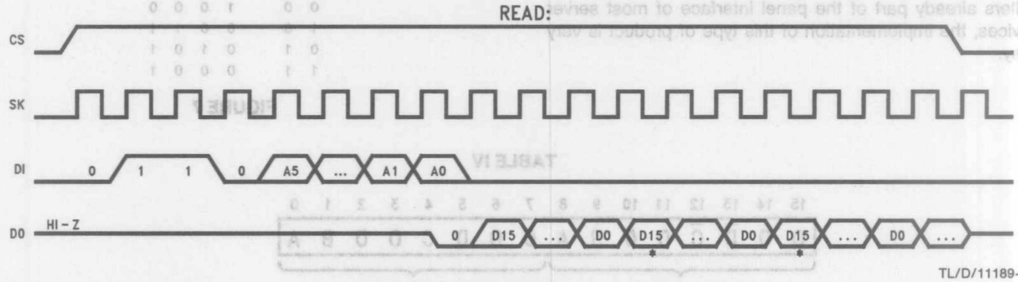

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FIGURE 8

WRITE:

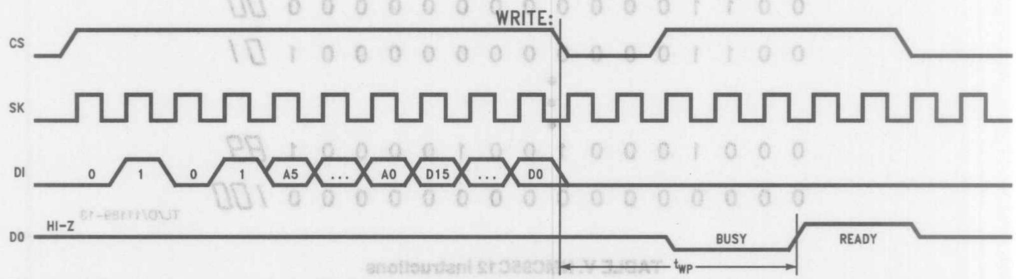

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FIGURE 9

INTRODUCTION

The design of an adapter card for a PC requires some knowledge of the different mechanisms used by the PC to access or exchange data with the adapter card.

The complexity of the mechanism used depends upon the level of functionality one wishes to implement on his design. At the low-end, the PC will access the adapter card as a simple I/O location, where for the more sophisticated cards, a BIOS will be incorporated onto the adapter card which may also use memory, I/O, interrupts and DMA channels from the PC.

This note discusses how to use the NM95C12 as a low cost solution for the implementation of high-end features on a general purpose adapter card for a PC.

1.0 OVERVIEW OF THE PC AND THE ADAPTER CARDS

In order to fully understand the possibilities offered by using an NM95C12 at the interface level between the PC and its adapter card, let's review the characteristics of that interface.

1.1 The PC has a certain amount of memory available for adapter cards. Both the location and space occupied by this memory vary depending on the type of PC (XT, AT). The XT reserves memory locations for 8-bit data transfers onto the adapter cards. The AT reserves the same locations for 8-bit data transfers but also reserves additional space for 16-bit data transfers.

1.2 The same mechanism applies to the I/O locations on the PC that are reserved for accesses onto an adapter card. A certain amount of I/O addresses will allow the PC to perform 8-bit data transfers with the adapter card on an XT system and some more locations will additionally be made available for 16-bit data transfers with the adapter card on an AT system.

1.3 Any adapter card you install into a PC is allowed to request interrupt service from the main PC card. An XT system offers the adapter card 6 interrupt lines where an AT system offers an additional 5 lines. (Not all of these lines are directly available for the adapter cards since some of them will be used by other cards on the PC.)

1.4 Finally, some DMA channels on the PC main board can be used by the adapter card through proper handling of DMA REQUEST and DMA ACKNOWLEDGE lines available on the PC connector. As for the other mechanisms, 8-bit DMA data transfers are allowed on an XT system where both 8- and 16-bit DMA data transfers are allowed on an AT-based system.

2.0 POSITIONING THE ADAPTER CARD

Any designer which intends to use one or more of the data transfer paths described above is aware that his card will have to carry the ability to be mapped into the available areas on the system, since other cards already installed into the PC probably make use of a part of the space reserved for the adapter cards.

2.1 If the adapter card contains memory accessible from the PC main board, up to two different levels of mapping may take place depending on the size of the memory. For a small memory size (let's say 8K or less), the entire area will be linearly accessible from the PC but its location will have to be mappable at different places into the range reserved for the adapter cards, thus ensuring that it will not interfere with any other cards using parts of this range. For larger memory, a second level of mapping is required, partitioning the memory into software selectable windows of 2K, 4K, 8K, etc. which location will still be mappable into available areas as described above (see *Figure 1*).

2.2 The same procedure applies to I/O locations on the adapter card. Any peripheral address has to have the possibility to be accessed at different selectable locations into the I/O address range reserved for adapter cards, thus ensuring that there won't be any address conflict with peripherals from other cards already installed into the system.

2.3 If the adapter card has the ability to request interrupt service from the PC main board, it also has to have the possibility to select the interrupt line it will use among those not being used by other adapter cards.

2.4 Finally, as for the interrupt lines, an adapter card using DMA channels must be able to select channels not used by other adapter cards.

3.0 TWO ISSUES: POSITIONING AND INITIALIZING

The most widely used way of implementing all of the above options is to install jumpers on the adapter card which setting will allow the end user to position its card into the available areas (see *Figure 2*). Even though this method has some disadvantages, like the fact that the user has to open the PC and remove the adapter card each time he has to modify the setting and the fact that a description of the settings allowed has to be carried along with the adapter card, it remains one of the cheaper and most easy to implement methods of positioning an adapter card into a PC.

Let's now consider some other interesting features that could be implemented on an adapter card. Once the application software is loaded from a diskette usually provided with the card, it may be possible to initialize and then to configure the card. For example, if the card is a data communication product, its on-board peripherals first have to be properly initialized and then the overall configuration of the link has to be defined (the parity and stop bits, the baud rate and such parameters as flow control, echoing, DCE or DTE arrangement, split clocking, etc. for either asynchronous or synchronous data transmission). Once all these parameters have been defined, the card should be operational as long as the power feeds the system.

An interesting step further in functionality would then be the implementation of some non-volatile data storage area on board into which the actual initialization and configuration of the adapter would be stored and referred to at any subsequent call of the application software following a power-up.

4

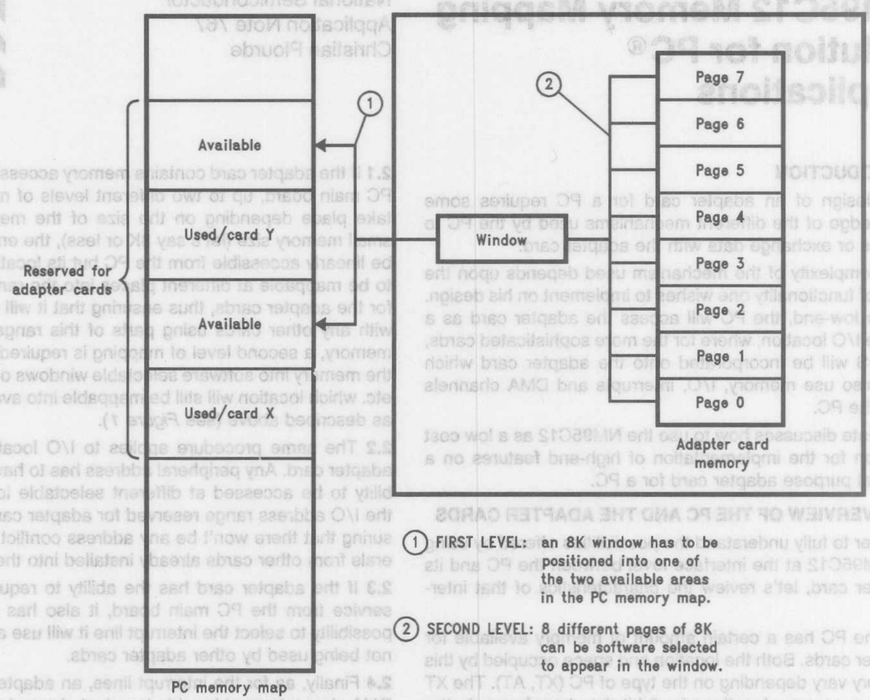

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FIGURE 1. Partitioning of 64K of Memory through an 8k Window Positioned into One of Two Available Areas in the PC Memory Map

If a BIOS is installed on the adapter card, the user could even be prompted to verify and modify (if required) the configuration of the card right away at power-up, since the BIOS signatures are scanned and given control after the usual diagnostics executions, graphic card, floppy and hard-disk recognition.

4.0 USE OF AN NM95C12 ADDS POWERFUL FEATURES TO YOUR ADAPTER CARD

The proposed application is to provide the PC with the possibility to access an NM95C12 located on the adapter card. The BIOS on the adapter card would instruct the PC to verify the status of a configuration flag stored in the NM95C12. If the status indicates that the card hasn't been initialized and configured yet, the user will be requested to accomplish these tasks prior to any further operation of the adapter card. Once the initialization has been properly loaded and saved, the BIOS, at any subsequent power-up, will simply instruct the user of the current configuration and ask if any modification is required.

The initialization portion of the card would make use of both the non-volatile memory and the dip switch's replacement features on the NM95C12. The positioning of the memory, the selection of the I/O addresses range and the interrupt lines or DMA channels (if required) would be set using the dip switch's replacement according to the user selection at first initialization. The other bytes or words used to initialize the peripherals on the adapter card would be stored in the NM95C12. All the configuration parameters related to the software operation of the card would also be saved into the NM95C12.

It is understood that such a solution does not eliminate all the jumpers or dip switches' on the adapter card. The location of the BIOS implemented on the card and the I/O address used to access the NM95C12 both have to be determined and set prior to the installation of the card into the PC. There is no easy way, if any, to work around such restrictions.

The circuit on *Figure 3* shows a simple way to implement an interface to the PC that will allow the user to position an 8K window of memory into one of eight possible locations in the adapter card's reserved area. He will have the possibility to select one of eight possible ranges of addresses for the I/O address of the peripherals on board and he will also be able to select one of four interrupt lines available on the PC connector. The memory on the adapter card consists of 32K of RAM divided into four pages of 8K. The selection of the page is performed through a write operation of 2 bits in a register whose I/O location has been determined by the setting of the NM95C12.

At power-up, before the system has been initialized, the PC must have the possibility to access at least the BIOS on the adapter card (ROM BIOS on *Figure 3*). LK1 on *Figure 3* allows eight different locations for that BIOS in the PC memory range reserved for that purpose. Since that BIOS will verify the configuration byte or word into the NM95C12, the I/O addresses of the circuit that accesses the NM95C12 also have to be selected prior to the installation of the adapter card into the PC. This is done via LK2 on *Figure 3*.

The circuit that allows the accesses to the NMC9512 is very simple. A sequence of writes to a latch (ltch A on *Figure 3*)

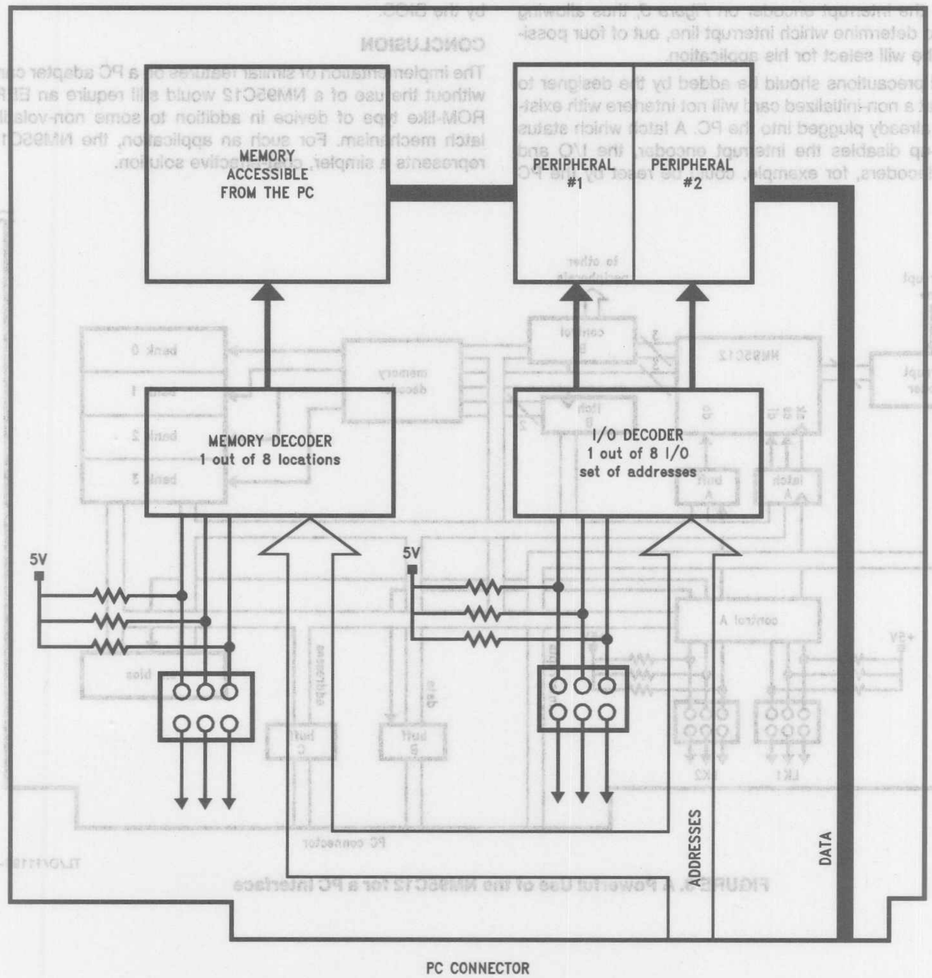

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FIGURE 2. Using Jumpers (or Dip Switches) to Position Both Memory and I/O Addresses on an Adapter Card

enables CS on the NM95C12, presents the data to be written to pin DI and latches this data into the NM95C12 by toggling the pin SK. The same principle applies to the read operation except that the bit output at pin DO of the NM95C12 is sent to the PC via a buffer (buff A on *Figure 3*).

The clock of latch A, the enable of buff A and the select and output enable of the ROM BIOS are all controlled by control A on *Figure 3* which may be a GAL.

The user is then allowed to position and configure its card. On the example of *Figure 3*, three lines of the NM95C12 are connected to the memory decoder. The status of these lines will position a window of 8K of RAM into one of eight possible locations in the PC memory area reserved for adapter cards. Three other lines of the NM95C12, connected to control B on *Figure 3*, will allow the same possibility for the I/O address of the peripherals on the adapter card. One of these peripherals is latch B into which the PC is now allowed to write two bits whose value will select one of the four pages of RAM to appear on the 8K window positioned by the first three lines of the NM95C12.

Finally, the two remaining lines of the NM95C12 are connected to the interrupt encoder on *Figure 3*, thus allowing the user to determine which interrupt line, out of four possible lines, he will select for his application.

Additional precautions should be added by the designer to ensure that a non-initialized card will not interfere with existing cards already plugged into the PC. A latch which status at power-up disables the interrupt encoder, the I/O and memory decoders, for example, could be reset by the PC once the proper configuration has been loaded or confirmed by the BIOS.

CONCLUSION

The implementation of similar features on a PC adapter card without the use of a NM95C12 would still require an EEPROM-like type of device in addition to some non-volatile latch mechanism. For such an application, the NM95C12 represents a simpler, cost-effective solution.

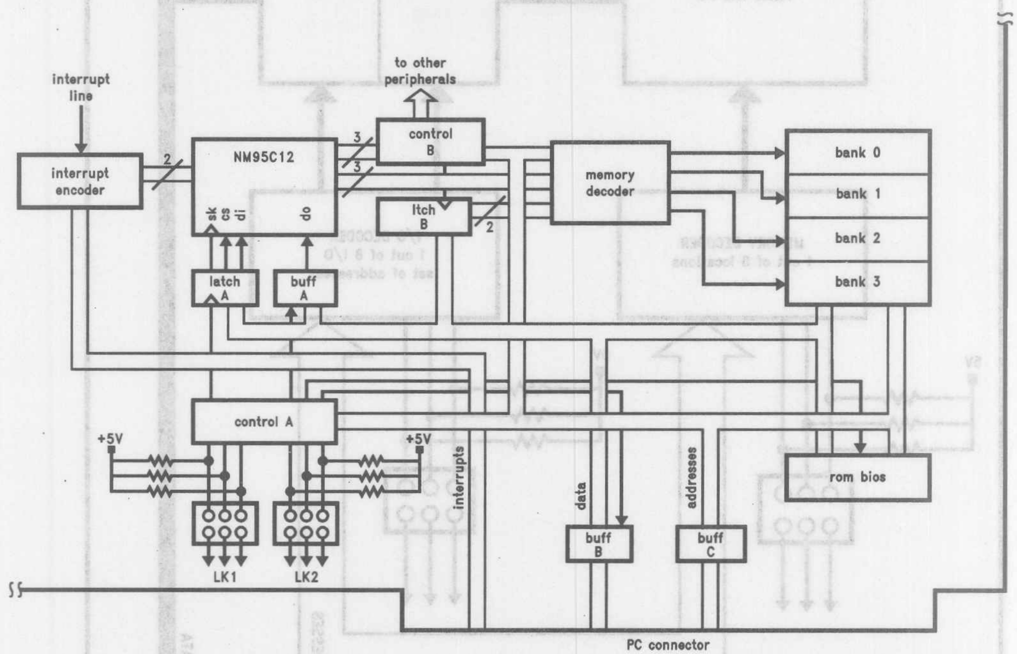

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FIGURE 3. A Powerful Use of the NM95C12 for a PC Interface

Integrated Manufacturing Control Using the Data Quad Switch EEPROM—NM95C12

National Semiconductor
Application Note 789
Jan Ladiges

INTRODUCTION

Manufacturing methods and testing techniques have become increasingly automated over the past few years. Of current interest are techniques which allow automated access to manufacturing information which, in turn, is used to tailor test and set up for individual manufactured assemblies. This note explores the application of the latest generation of memory devices to manufacturing control situations and integrating access schemes for test, in system programming and manufacturing control.

WHAT INFORMATION?

The first question raised in manufacturing control applications is what information needs to be accessable. In most cases information like serial number, date of manufacture, and revision number need to be written once during initial manufacture. Ideally, this information should be secure (i.e., read only). As a product passes through test additional data may be recorded such as calibration constants or configuration data. If an assembly should fail, the type of failure and number of recurrences may be recorded at the repair depot to determine, for example, if this assembly should be scrapped.

All of this data does not require a large memory device. National Semiconductor's family of serial access E²PROMs are ideal candidates because of low cost, small footprint and ease of access.

SECURITY

The issue of data security is addressed by the 93CSXX family of devices. In these units a portion (or all) of the memory area may be set up to appear as ROM (once desired data has been loaded into the device). The amount of ROM vs PROM is determined by a value in the protection register which delimits the portion of the device that is write protected. For details refer to AN-507 — Using the 93CSXX MICROWIRE™ family.

Some of the synchronous bus devices (24CXX I²C family) have write protection of the upper half of the memory space by bringing a control line (WP) high.

ACCESS

In the most basic form of automated manufacturing control, an E²PROM is simply added to a circuit assembly as an isolated block. There may be no electrical connection between the memory and any portion of the circuit assembly. A means of accessing the pins of the memory device must be considered. This may involve adding extra contacts to a card edge, creating a separate pin-type connector area or simply providing BON (Bed Of Nails) access. The latter may prove impractical with the increased use of surface mount.

A more promising and efficient use of board resource can be realized if the memory device shares I/O pins and power supply with the host assembly. The number of access points required for varying applications schemes ranges from 2 (for synchbus with no security) to 5 (for microwire with full security).

To take maximum advantage of the E²PROM it is often desirable to allow access both externally (like the isolated case) and internally by the system resident on the circuit assembly.

An example of shared functionality is given in *Figure 1* which allows the resident system to flag a fault condition. The unique feature of this is the fault flag will be valid even if system power is cycled on and off or the board removed from the system. The visible flag (an LED) allows a technician to quickly identify a problem board. Additional information (i.e., a fault code) can be written into the E²PROM as well. The module, when returned for repair, contains all the traditional manufacturing information as well as the fault code.

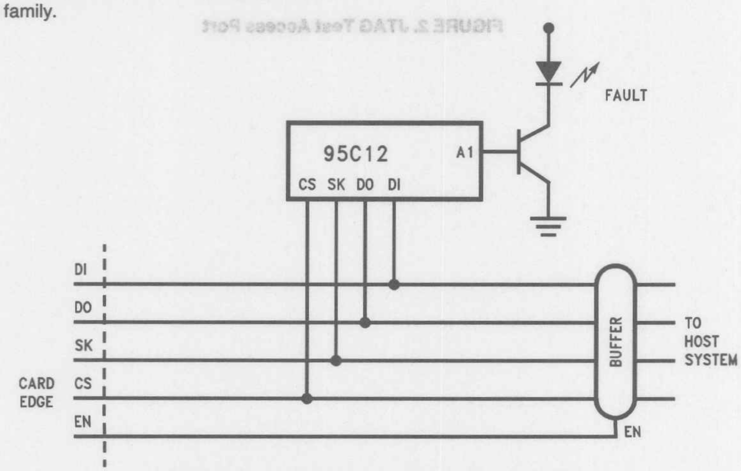

FIGURE 1. Shared Access with Non-Volatile Fault Flag

tical at present density levels and virtually impossible when SMD's are mounted on both sides of the board.

To facilitate surface mount board testing, electronic rather than mechanical techniques have evolved. The solution often consists of boundary scan and some form of built in self test (BIST).

JTAG (Joint Test Action Group), sponsored by the IEEE P1149-1 Working Group, has defined a boundary scan standard which has become widely endorsed. This JTAG standard specifies that each conforming IC have a Test Access Port (TAP) which allows devices to be connected in series and minimizes interconnect overhead *(Figure 2)*. The boundary scan register (double buffered) gives access to

Surveying current programmable logic trends, GAL type devices are extremely popular to replace small blocks of random logic. One disadvantage is that traditionally each different "pattern" would have to be programmed, tested and identified prior to being installed on the assembly. With SMT versions of these devices, handling alone poses a significant inconvenience.

The concept of programming devices after they have been installed (ISP — In System Programming) is beginning to attract interest.

What do these test and ISP techniques have in common with manufacturing control? — serial board access.

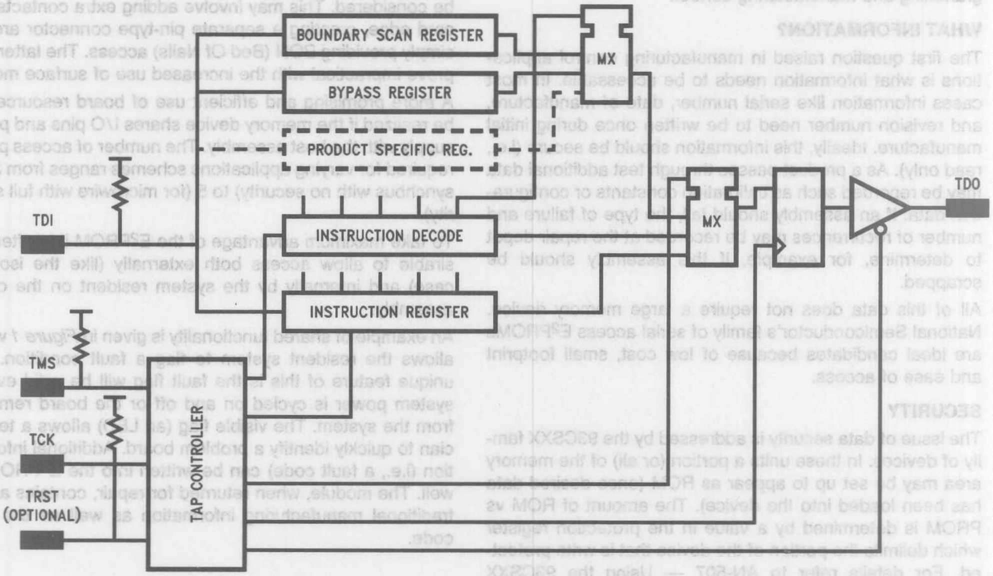

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FIGURE 2. JTAG Test Access Port

GALs and implements a serial E²PROM for manufacturing control data.

All 3 functions require a serial access scheme. If each is considered independently, a considerable number of pins would have to be dedicated to these functions (at least 12 connection points). One common bus and a common protocol to access management information, provide test access, and perform incircuit PLD programming would be ideal.

AN EXAMPLE COMMON ACCESS SYSTEM

The circuit of *Figure 3* uses a COP 822 microcontroller to create a JTAG to MICROWIRE converter with added support for E²PROM and PLD programming requires only 5 access pins.

Because JTAG test access often requires high speed, this system has been broken down as two JTAG loops (hence two TMS pins), one high speed dedicted to the test loop and a slower speed loop dedicated to E²PROM and PLD access through the COP 822. The speed of this JTAG loop is limited by COP processing speed in translation to MICROWIRE.

This approach represents a solution for common access using devices available today. As standards take hold (like JTAG) then non-volatile memories and ISP PLD's may appear supporting a **standard** serial protocol and further reducing the overheads in a common access scheme.

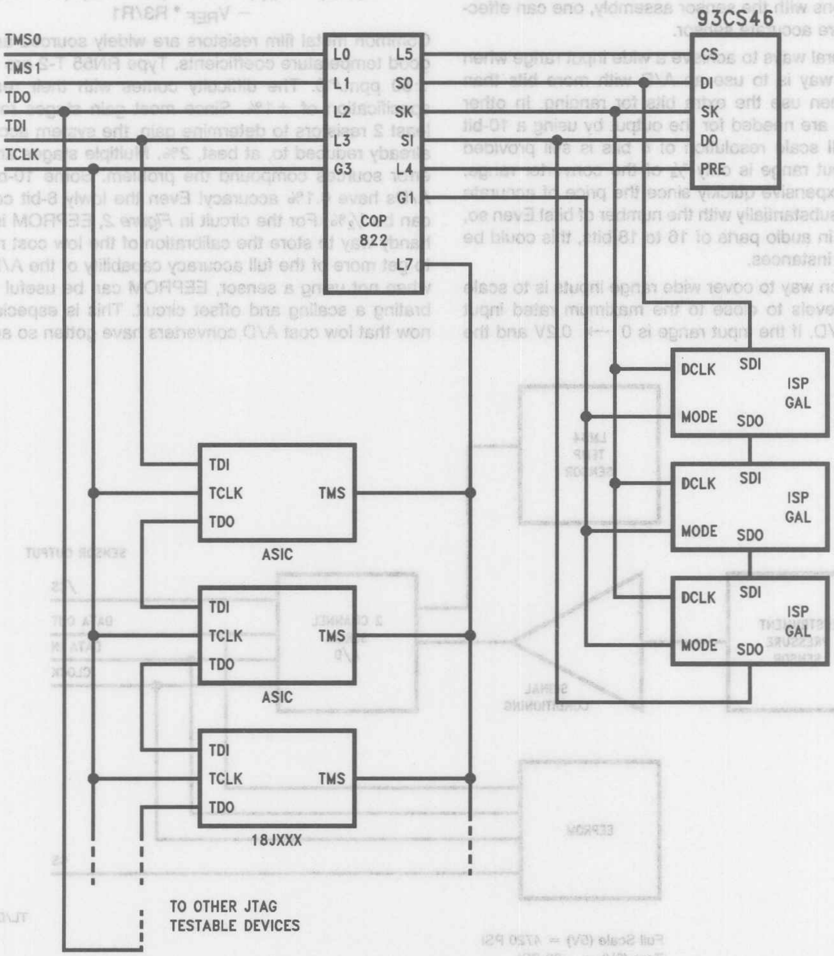

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FIGURE 3. Common JTAG Access for Test, ISP, and Manufacturing Control

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NM95C12 EEPROM Controls Amplifier Gain

National Semiconductor
Application Note 790
Harry W. Lewis

BACKGROUND

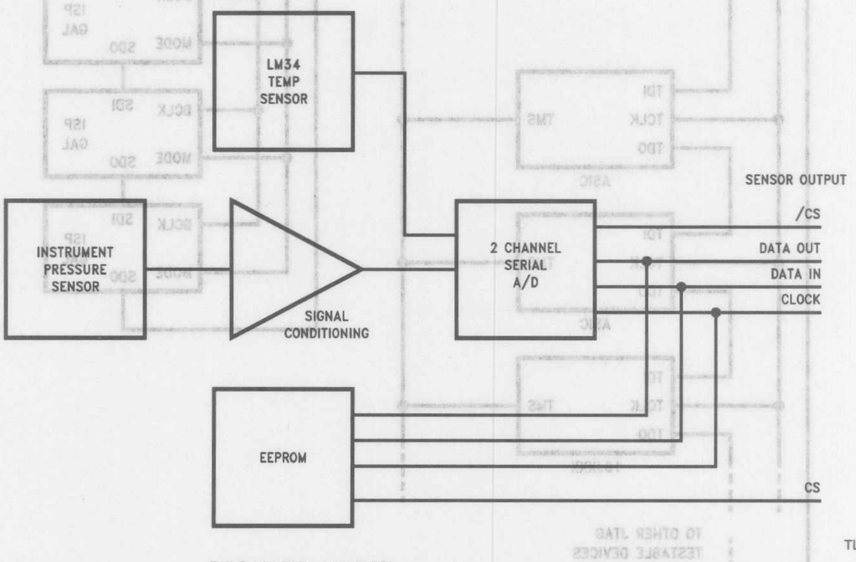
Electrically Erasable PROM or EEPROM finds wide application in analog data acquisition. When using sensors, some possibilities include storing calibration constants (gain, nonlinearities, temperature effects and offset), the engineering units of measurements, and even keeping serial numbers. In *Figure 1* for example, after an A/D converter converts the analog sensor output, the processor can use correction factors from the EEPROM to get a final value. By keeping these corrections with the sensor assembly, one can effectively get a more accurate sensor.

There are several ways to achieve a wide input range when required. One way is to use an A/D with more bits than needed and then use the extra bits for ranging. In other words, if 8 bits are needed for the output by using a 10-bit converter a full scale resolution of 8 bits is still provided even if the input range is only ¼ of the converter range. This can get expensive quickly since the price of accurate A/Ds goes up substantially with the number of bits! Even so, with advances in audio parts of 16 to 18 bits, this could be viable in some instances.

A more common way to cover wide range inputs is to scale the incoming levels to close to the maximum rated input range of the A/D. If the input range is 0 → 0.2V and the converter is rated 0 → 5V, a gain of 25 in front of the A/D will give the full resolution over the reduced range. Additionally, the input range can be offset from zero. While many A/Ds have range and offset options, there are limits if the accuracy is to be kept. A circuit to use both scaling and offset is *Figure 2*. The gain and offset are mostly determined by the reference and the resistor ratios.

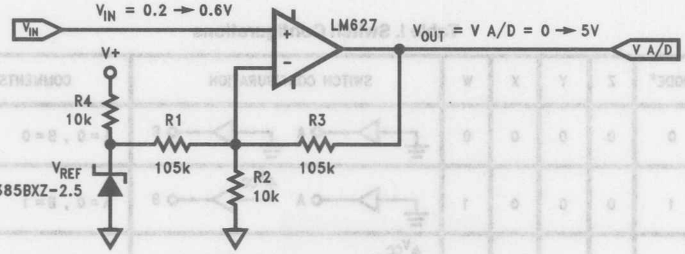
$$V(A/D) = V_{IN}\,(1 + R3 * (R1 + R2)/(R1 * R2)) - V_{REF} * R3/R1$$

Common metal film resistors are widely sourced and have good temperature coefficients. Type RN55 T-2 are rated at ±50 ppm/°C. The difficulty comes with their resistance specification of ±1%. Since most gain stages require at least 2 resistors to determine gain, the system accuracy is already reduced to, at best, 2%. Multiple stages and other error sources compound the problem. Some 10-bit serial A/Ds have 0.1% accuracy! Even the lowly 8-bit converter can be ½%. For the circuit in *Figure 2*, EEPROM is a very handy way to store the calibration of the low cost resistors to get more of the full accuracy capability of the A/D. Even when not using a sensor, EEPROM can be useful for calibrating a scaling and offset circuit. This is especially true now that low cost A/D converters have gotten so accurate.



Full Scale (5V) = 4720 PSI
Zero (0V) = −83 PSI
Temp Coefficient = +0.2 PSI/°F
Serial # = 184625
Last Rev = F

FIGURE 1. Sensor with Digital Output and Correction Factors



$$V_{OUT} = V\,A/D = V_{IN}\left(1 + \frac{R3\,(R1 + R2)}{(R1 * R2)}\right) - \frac{R3}{R1}V_{REF}$$

$$= 12.5 * V_{IN} - 2.5V$$

FIGURE 2. Scaling and Offset Circuit

DON'T BE A DIP

For storing data, EEPROM can generally beat DIP switches. However, there were some other things that DIP switches could do better. One case was having external access to logic levels without needing an additional port chip. Another area was switching analog voltages. To replace an analog DIP switch, a designer often had to add an output port and a separate CMOS or other switch to do the actual switching. The NMC95C12 1024-bit CMOS EEPROM with DIP switches attacks both these areas. When first glancing at the data sheet, the title "EEPROM with DIP switches" can conjure up visions of the data being stored in 1024 tiny levers on top of the package! Of course that is not the case, see *Figure 3* for the real block diagram. Actually the part has 61 words of 16 bits of EEPROM for general use. That totals 976 bits. The DIP switches referenced in the title are 8 pins with switch logic to allow several different modes of operation as controlled by the switch configuration register. There is a nonvolatile Initial Switch Setting Register of 16 bits. And, finally, a Switch Readback Register allows the pins to be used as a digital input port. Processor interface is by a serial MICROWIRE™ port.

THE BIG SWITCH

Switches are the main difference between the NM95C12 and other EEPROMs. They can be thought of as four independent switches each having two pins, A and B. Each switch has four control bits labeled W, X, Y and Z to set it to one of its 14 modes. Table I shows all the modes. The Switch Configuration Register (SCR *Figure 4*) is 16 bits long to hold all four bits of each of the four switches. It is not made from EEPROM cells so it can be written faster and there is no wearout mechanism. Being volatile, the SCR is reloaded at each powerup from the EEPROM Initial Switch Setting Register.

WHERE DID THE PARALLEL PORT COME FROM?

Switch modes 0–3 allow the 2 pins to be digital outputs. When bits Y and Z are set to 0, A = X and B = W. Other modes allow A and/or B to be TRI-STATE® for use as digital inputs or I/O. *Figure 5* shows the switches being used for general input and output, to set gain controls, and to drive analog multiplexers. In *Figure 5*, the port of U4 selects the input channel of the A/D via the multiplexer U3. Input channel 7 has a selectable gain preamplifier (U1) whose gain is controlled by U2 selecting the proper feedback tap. The resistor values for R1, R2, R3 and R4 are standard 1% values. Ideally the values would be 48K, 12K, 3K and 1K. Although they are not quite correct for the gains desired, calibration values stored in the EEPROM can correct for this while fixing the other errors. One thing to keep in mind when selecting the standard values, make sure the A/D stays in its active range during the whole range of expected signal input. If the A/D needed to exceed the maximum count, the error generated is not correctable. This implies making the gains on the low side.

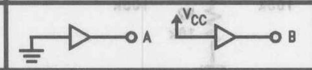
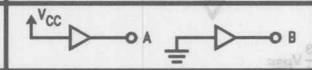
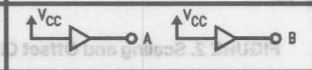
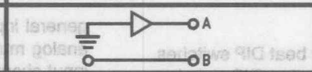
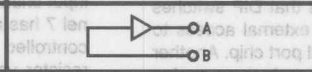
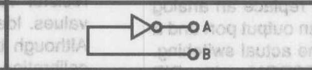
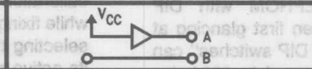
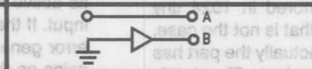
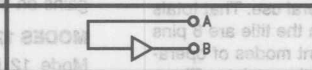
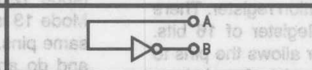
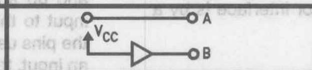
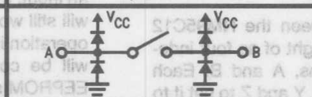
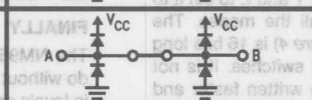
MODES 12 AND 13?

Mode 12 is an open (10+ MΩ) between pins A and B. Mode 13 is an ANALOG short (200Ω or less) between the same pins. In *Figure 6*, analog switches give variable gains and do analog multiplexing. Switches 1 and 2 select the input to the A/D. Switches 3 and 4 control gain. Although the pins used for a closed analog switch can not be read as an input, the input function of the Switch Readback Register will still work for the other pins, so mixed analog and digital operation is possible. Of course, errors in the amplifier gains will be corrected by storing calibration constants in the EEPROM section of the part.

FINALLY!

The NM95C12 can accomplish what a DIP switch used to do without the extra parts. You have external access to logic levels and you can even switch analog voltages. All without needing additional port or multiplexer chips.

Table I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = TRI-STATE
5	0	1	0	1		A = B
6	0	1	1	0		A = $\overline{B}$
7	0	1	1	1		A = 1 , B = TRI-STATE
8	1	0	0	0		A = TRI-STATE , B = 0
9	1	0	0	1		B = A
10	1	1	1	0		B = $\overline{A}$
11	1	0	1	1		A = TRI-STATE , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

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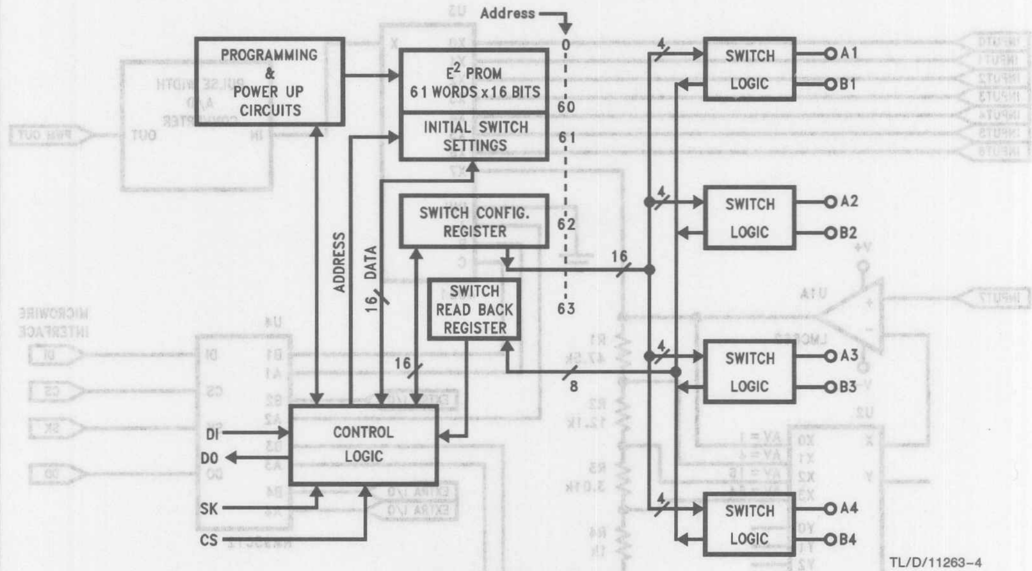
*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.



TL/D/11263-4

FIGURE 3. Block Diagram

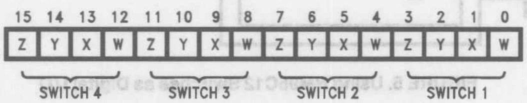


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FIGURE 4. Switch Configuration Register (SCR)

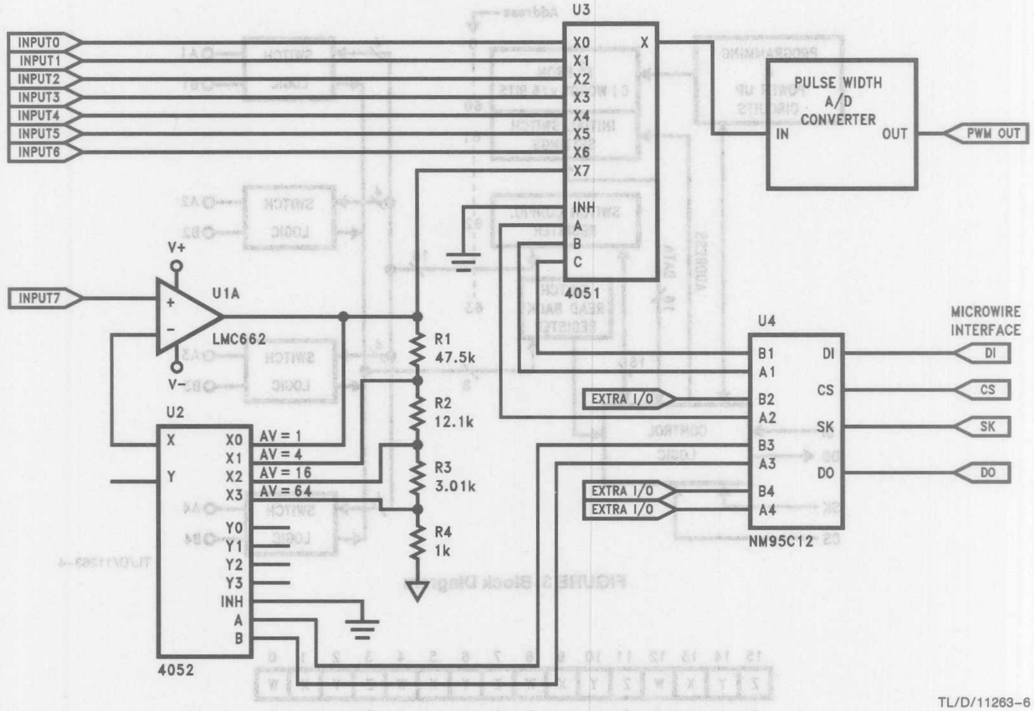
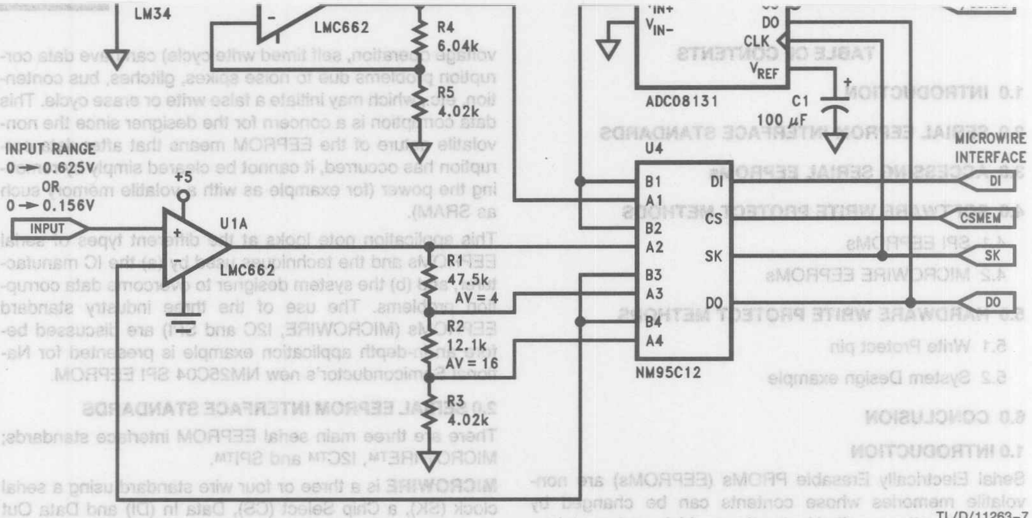


FIGURE 5. Using NM95C12 Switches as Digital I/O



TL/D/11263–7

FIGURE 6. Using NM95C12 Switches as Analog Switches

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TABLE OF CONTENTS

1.0 INTRODUCTION

Serial Electrically Erasable PROMs (EEPROMs) are non-volatile memories whose contents can be changed by unique bit patterns called instructions, which are input to the memory array using serial data and clock pins. Serial EEPROMs operate from a single V_{CC} voltage supply (typically 2.0V–5.5V); an on-board charge pump provides the higher voltages required during the programming operation. These features offer the designer an easy to use and very flexible device. The ability to have a non-volatile memory whose contents can be changed "in-system" gives design engineers much greater flexibility. Serial EEPROMs provide a highly reliable and cost effective solution for a wide range of applications which need to store information such as calibration data, setting levels, and other user programmable data.

However, one factor a system designer needs to be aware of is the possibility of data corruption caused by "erroneous" or "false" data writes. Full featured EEPROMs (single voltage operation, self timed write cycle) can have data corruption problems due to noise spikes, glitches, bus contention, etc., which may initiate a false write or erase cycle. This data corruption is a concern for the designer since the non-volatile nature of the EEPROM means that after data corruption has occurred, it cannot be cleared simply by removing the power (for example as with a volatile memory such as SRAM).

This application note looks at the different types of serial EEPROMs and the techniques used by (a) the IC manufacturer, and (b) the system designer to overcome data corruption problems. The use of the three industry standard EEPROMs (MICROWIRE, I2C and SPI) are discussed before an in-depth application example is presented for National Semiconductor's new NM25C04 SPI EEPROM.

2.0 SERIAL EEPROM INTERFACE STANDARDS

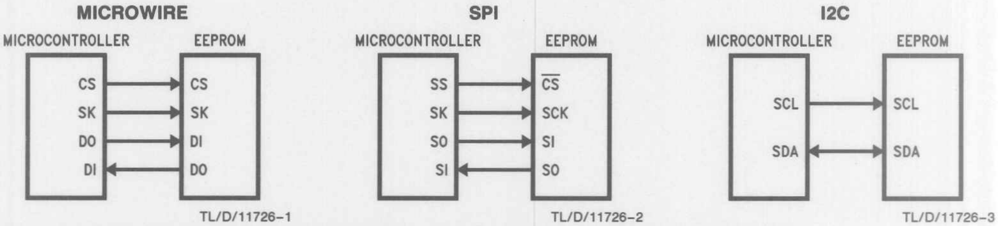
There are three main serial EEPROM interface standards; MICROWIRE™, I2C™ and SPI™.

MICROWIRE is a three or four wire standard using a serial clock (SK), a Chip Select (CS), Data In (DI) and Data Out (DO) lines. These devices are available in either standard form (NM93C06/46/56/66) or a security form (NM93CS06/46/56/66).

I2C (Inter-Integrated Circuit) is a two wire synchronous bus which uses SCL (clock) and SDA (data) to clock data between a master (for example a microcontroller) and a slave (the EEPROM). These devices are available in either standard form (NM24C02/04/08/16) or write protected form (NM24C03/05/09/17).

SPI (Serial Peripheral Interface) is a three or four wire synchronous bus which uses a chip select (CS), a serial clock (SCK), Data In (SI) and Data Out (SO) lines.

The three standardized serial interfaces are shown in *Figure 1.* The key specifications of these three interfaces are compared in *Figure 2.*



Note: If a standardized bus is not available, general purpose I/O port lines can be used to communicate with a serial device.

FIGURE 1. Serial EEPROM Interfaces

National Semiconductor has serial EEPROMs for all 3 standards

	MICROWIRE NM93Cxx	SPI NM25Cxx	I2C NM24Cxx
Max Bus Speed	1 MHz	2.1 MHz	100 KHz
No Active Pins	3 or 4	3 or 4	2
Max Memory Size	N/A	N/A	16 kbit
Largest Device	4 kbit ⟵ 16 kbit	4 kbit	16 kbit
Acknowledge	NO	NO	YES
Data Size	8 bits or 16 bits	8 bits	8
Block Write	NO	YES	YES
Sequential Read	YES (CS version)	YES	YES
No Device on Bus	Limited by Port Pins	Limited by Port Pins	Up to 16 kbits
Security Feature	YES (CS version)	YES	YES (03/05/09/17)

FIGURE 2. Serial EEPROM Bus Comparison

Serial EEPROM devices are available from National Semiconductor in all three industry standards, in a variety of sizes as shown in *Figure 3*.

	MICROWIRE			I^{2}C		SPI
	Standard	Security	Special Feature	Standard	Write Protected	
256-bit	NM93C06	NM93CS06				
1 kbit	NM93C46	NM93CS46	NM93C46A NM59C11 NM95C12			
2 kbit	NM93C56	NM93CS56		NM24C02	NM24C08	
4 kbit	NM93C66	NM93CS66		NM24C04	NM24C05	NM25C04
8 kbit				NM24C08	NM24C09	
16 kbit	NM93C86A			NM24C16	NM24C17	

*Note: Contact Customer Support Center at (800) 272-9959 for latest details of availability.

FIGURE 3. Serial EEPROM Availability

3.0 ACCESSING SERIAL EEPROMs

No matter which type of serial interface standard used by an EEPROM, they all have two basic instructions: READ and WRITE data.

READ: This is a non-destructive instruction which reads data from the memory array.

WRITE: This is a destructive instruction. The data in the memory array is either erased or over written by the new data.

A typical set of EEPROM instructions, using the NM25C04 SPI EEPROM as an example is shown in *Figure 4*.

Instruction Name	Operation
WREN	Set Write Enable Latch
WRDI	Reset Write Enable Latch
RDSR	Read Status Register
WRSR	Write Status Register
READ	Read Data from Memory Array
WRITE	Write Data to Memory Array

Note: EEPROM powers-up in Write Disable Mode

Note: Must execute WREN before a Write instruction

Note: Status Register is used to:
- Poll READY/BUSY
- Set zone write protection ranges
- Indicate Write enable status

FIGURE 4. NM25C04 SPI EEPROM Instructions

In order to ensure data integrity, the system designer needs to understand the possible causes of inadvertent data writes which may cause data corruption, and the ways of overcoming this problem.

4.0 SOFTWARE WRITE PROTECT METHODS

All National Semiconductor EEPROMs incorporate common features to protect against inadvertent data writing to offer high reliability operation. A program disable mode is included which will ensure that devices power-up in the "Write Disable mode". This means that unless the "Write Enable" instruction is executed, the EEPROM will abort any requested write or erase cycles. This is especially useful for protecting against data corruption during power transitions.

4.1 SPI EEPROMs (NM25C04)

National Semiconductor's SPI EEPROMs such as the 4 kbit NM25C04 includes the following design features to guard against inadvertent data writes:

— Write Protect ($\overline{WP}$) pin to disable memory writes

— Write Disable Instructions

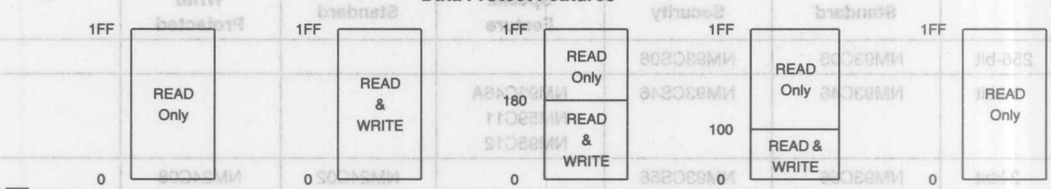
— Software write protection: the user can define a portion of the memory to be READ Only.

The various write protection configurations are shown in *Figure 5*.

4.2 MICROWIRE EEPROMs

All NM93CSxx devices have the security feature which allows the user to define a portion of the memory to be write protected, either permanently or temporarily. This is useful for storing secure information in a system, such as calibration data. To control the secure memory involves a combination of setting a hardware pin and various software instructions as shown in *Figure 6*.

Data Protect Features



$\overline{WP}$ Pin	0	1	1	1	1
BP1	X	0	0	1	1
BP0	X	0	1	0	1

#1. Software Write Enable/Disable
  — Powers-up in write disable state
  — Must execute WREN before a write Instruction

#2. Zone Write protect
  — Controlled by BP1 and BP0 in WRSR (WRite Status Register)

#3. Write Protect Pin ($\overline{WP}$)
  — Hardware method of preventing erroneous write cycles
  — $\overline{WP}$ must be high to allow writes to EEPROM or the status register

FIGURE 5. NM25C04 Write Protect Features

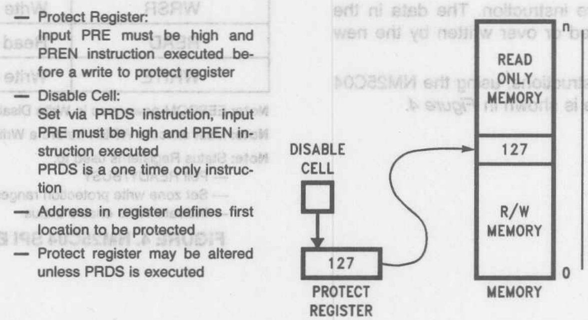


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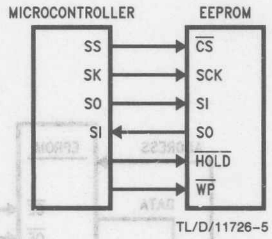
FIGURE 6. NM93CSxx Memory Protect Register

The Write Protect pin ($\overline{WP}$) allows the system designer to include a hardware method for protecting against false data writes. The basic principle is the same for each family of serial EEPROMs; for this example the NM25C04 SPI device is considered.

This interface can be modified by the addition of some external logic to give software control for the $\overline{WP}$ pin to give increased immunity from data corruption. The basic principle is shown in *Figure 8.*

NM25C04 SPI EEPROM



Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input

FIGURE 7. NM25C04 EEPROM Interface to Microcontroller

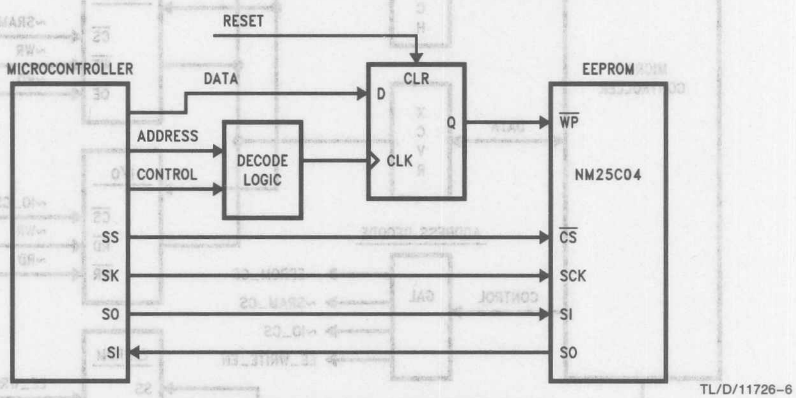


FIGURE 8. Hardware Controlled Write Protect

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The theory of operation is as follows:

System RESET signal clears latch output Q, setting $\overline{WP}$ at logic low level making EEPROM READ only,

For a WRITE instruction to the EEPROM, the microcontroller must first write a logic "1" to the latch to enable the $\overline{WP}$ pin before executing the normal EEPROM WRITE instruction,

After the WRITE instruction the microcontroller writes a logic "0" to the latch to disable further EEPROM WRITEs.

5.2 System Design Example

This method can be implemented in a practical way, as shown in the design in *Figure 9*.

The common system block diagram built around an 8- or 16-bit microcontroller will have EPROM, SRAM, Various I/O Ports and a serial EEPROM. The address decode and control logic implementation typically uses a programmable logic device such as a GAL®. The flexibility and user programmability of the GAL allows a designer to integrate the write protect logic for the serial EEPROM in a reliable and cost effective manner.

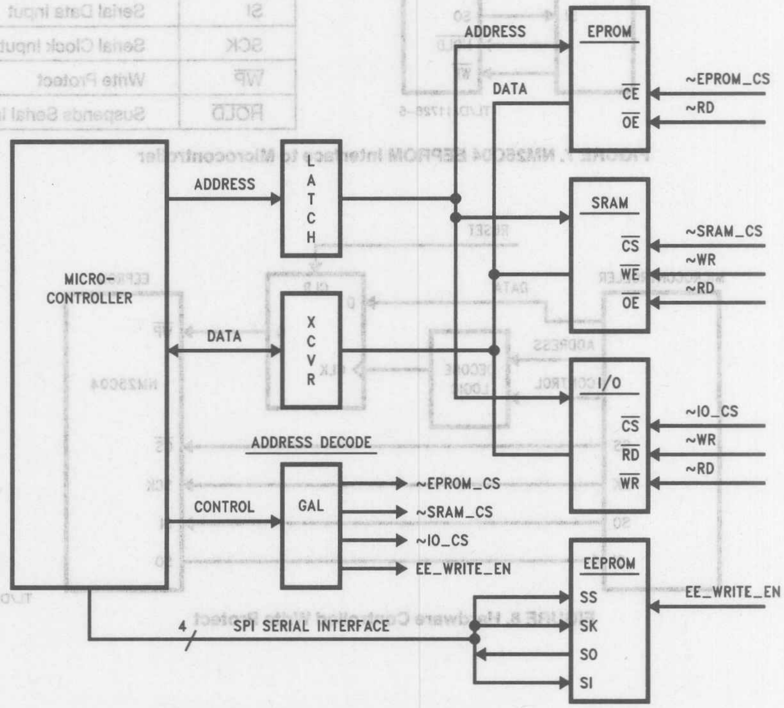

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FIGURE 9. Integrated Address Decode/Write Protect Logic

The system memory map is shown in *Figure 10.*

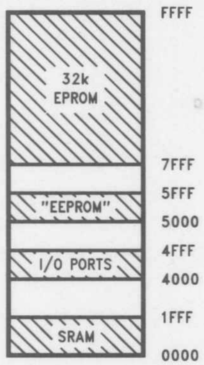

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FIGURE 10. System Memory Map

The EEPROM typically connects directly to the microcontroller, either via a standard serial interface (e.g., SPI port for Motorola 68HC05/11 micro's, MICROWIRE port for National Semiconductor COPS™/HPC™ micro's) or to parallel port pins which can be toggled by software as required. For the purpose of the write protect logic the EEPROM is "mapped" to address space. Note in this example fully exhaustive address decoding was not used.

The logic equations for the GAL can be created using a wide range of PLD design software tools; this example uses National Semiconductor's OPAL™ design software and is shown in the appendix at the end of this application note.

A typical EEPROM WRITE operation would follow the following routine:

Write a "1" to address 5000H (sets $\overline{\text{WP}}$ high)

Perform EEPROM WRITE cycle

Write a "0" to address 5000H (sets $\overline{\text{WP}}$ low)

By having to explicitly follow this set of operations, it protects the serial EEPROM from inadvertent data writes.

6.0 CONCLUSION

Serial EEPROMs are becoming a standard component in virtually every system; they offer the system designer an easy to use, very flexible solution for a wide range of non-volatile parameter storage applications. The addition of an EEPROM allows for increased system functionality and flexibility providing a superior solution to battery back-up RAM. Serial EEPROMs are highly reliable, offering endurances of 1 million data changes, and data retention of greater than 40 years. The combinations of good IC design practice and system design techniques help solve the issue of data corruption giving high integrity non-volatile memory solutions.

REFERENCES

National Semiconductor Memory Databook

National Semiconductor PLD Databook and Design Guide

National Semiconductor Microcontroller Databook

APPENDIX

EEAPPS.OPL

```
Begin Header

GAL Design for Address Decode Logic & EEPROM Write Protect Logic
National Semiconductor, 1992

End Header

Begin Definition

DEVICE GAL22V10;

INPUTS

SYS_CLK = 1,
          A15 = 2, A14 = 3, A13 = 4, A12 = 5,
          A11 = 6, A10 = 7, A9 = 8, A8 = 9,
          RD = 10, WR = 11, D0 = 13,
          RESET = 14;                          (RESET active high)

OUTPUTS (COM)

          !~EPROM_CS = 20, !~SHAM_CS = 19, !~IO_CS = 18; (active low outputs)

OUTPUT (REG)

EE_WRITE_EN = 17;

SET       ADDRESS = [A15,A14,A13,A12,A11,A10,A9,A8];

End Definition

Begin Equations

~EPROM_CS =      !RESET & !RD & WR & ( (ADDRESS >= ^h7F) & (ADDRESS <= ^hFF) );

~SRAM_CS =       !RESET & ( !RD + !WR)
                 & ( (ADDRESS >= ^h00) & (ADDRESS <= ^h1F) );

~IO_CS =         !RESET & ( !RD + !WR)
                 & ( (ADDRESS >= ^h40) & (ADDRESS <= ^h4F) );

EE_WRITE_EN := !RESET & (RD & !WR)
                & D0 & ( (ADDRESS >= ^h50) & (ADDRESS <= ^h5F) );

End Equations
```

EEAPPS.EQN

```
GAL Design for Address Decode Logic & EEPROM Write Protect Logic
National Semiconductor, 1992

;Translated from NSC formatted PLA file.

CHIP EEAPPS GAL22V10
  SYS_CLK=1 A15=2 A14=3 A13=4 A12=5 A11=6
  A10=7 A9=8 A8=9 RD=10 WR=11 D0=13 RESET=14
  EE_WRITE_EN=17 /~IO_CS=18 /~SRAM_CS=19 /~EPROM_CS=20

EQUATIONS

~EPROM_CS = A14 * A13 * A12 * A11 * A10 * A9 * A8 * /RD * WR
          * /RESET
       + A15 * /RD * WR * /RESET

~SRAM_CS = /A15 * /A14 * /A13 * /WR * /RESET
       + /A15 * /A14 * /A13 * /RD * /RESET
~IO_CS = /A15 * A14 * /A13 * /A12 * /WR * /RESET
       + /A15 * A14 * /A13 * /A12 * /RD * /RESET

EE_WRITE_EN := /A15 * A14 * /A13 * A12 * RD * /WR * D0 * /RSET
```


4

INTRODUCTION

National Semiconductor's NM24C EEPROMs are designed to interface with Inter-Integrated Circuit (I^2C) buses and hardware. NSC's electrically erasable programmable read only memories (EEPROMs) offer valuable security features (write protection), two write modes, three read modes and a wide variety of memory sizes. Applications for the I^2C bus and NM24C memories are included in SANs (small-area networks), stereos, televisions, automobiles and other scaled-down systems that don't require tremendous speeds but instead cost efficiency and design simplicity.

I^2C BACKGROUND

The I^2C bus configuration is an amalgam of microcontrollers and peripheral controllers. By definition: a device that transmits signals onto the I^2C bus is the "transmitter" and a device that receives signals is the "receiver"; a device that controls signal transfers on the line in addition to controlling the clock frequency is the "master" and a device that is controlled by the master is the "slave". The master can transmit or receive signals to or from a slave, respectively, or control signal transfers between two slaves, where one is the transmitter and the other is the receiver. It is possible to combine several masters, in addition to several slaves, onto an I^2C bus to form a multimaster system. If more than one master simultaneously tries to control the line, an arbitration procedure decides which master gets priority. The maximum number of devices connected to the bus is dictated by the maximum allowable capacitance on the lines, 400 pF, and the protocol's addressing limit of 16k; typical device capacitance is 10 pF. Up to eight E^2PROMs can be connected to an I^2C bus, depending on the size of the memory device implemented.

Simplicity of the I^2C system is primarily due to the bidirectional 2-wire design, a serial data line (SDA) and serial clock line (SKL), and to the protocol format. Because of the efficient 2-wire configuration used by the I^2C interface compared to that of the MICROWIRE™ and SPI interface, reduced board space and pin count allows the designer to have more creative flexibility while reducing interconnecting cost.

OPERATING NATIONAL SEMICONDUCTOR'S NM24Cs

The NM24C E^2PROMs require only six simple operating codes for transmitting or receiving bits of information over the 2-wire I^2C bus. These fields are explained in greater detail below and briefly described hereafter: a start bit, a 7-bit slave address, a read/write bit which defines whether the slave is a transmitter or receiver, an acknowledge bit, message bits divided into 8-bit segments and a stop bit.

For efficient and faster serial communication between devices, the NM24C Family features page write and sequential read.

The NM24C03/C05/C09/C16/C17 Family offers a security feature in addition to standard features found in the NM24C02/C04/C08/C16 Family. The security feature is beneficial in that it allows Read Only Memory (ROM) to be implemented in the upper half of the memory to prevent any future programming in that particular chip section; the remaining memory that has not been write protected can still be programmed. The security feature in the NM24C03/C05/C09/C17 Family does not require immediate implementation when the device is interfaced to the I^2C bus, which gives the designer the option to choose this feature at a later date. Table I displays the following parameters: memory content, write protect and the maximum number of individual I^2C E^2PROMs allowed on an I^2C bus at one time if the total line capacitance is kept below 400 pF.

Code used to interface the NM24Cs with National Semiconductor's COP8 Microcontroller Family is listed in a latter section of this application note for further information to the reader.

TABLE I

Part No.	Number of 256x8 Page Blocks	Write Protect Feature	Max. Parts
NM24C02	1	No	8
NM24C03	1	Yes	8
NM24C04	2	No	4
NM24C05	2	Yes	4
NM24C08	4	No	2
NM24C09	4	Yes	2
NM24C16	8	No	1
NM24C17	8	Yes	1

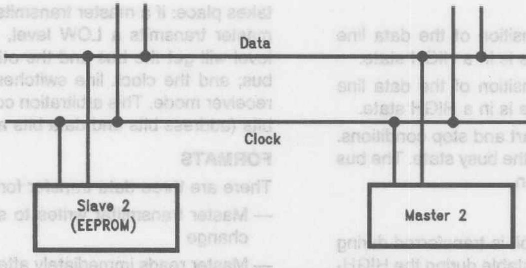

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FIGURE 1. I²C-Bus Configurations

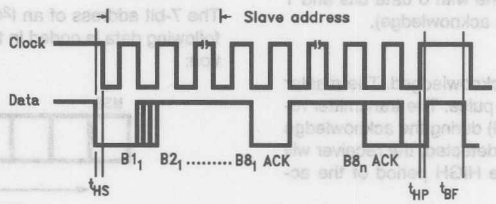

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FIGURE 2. I²C Bus Timing

Start Condition

— Clock and Data line high (Bus free)

— Change Data line from high to low

— After $t_{HS(Min)}$ = 4 μs the master supplies the clock

Acknowledge

— Transmitting device releases the Data line

— The receiving device pulls the Data line low during the ACK-clock if there is no error

— If there is no ACK, the master will generate a Stop Condition to abort the transfer

Stop Condition

— Clock line goes high

— After $t_{HP(Min)}$ = 4.7 μs the Data lines go high

— The master maintains the Data and Clock line high

— Next Start Condition after $t_{FB(Min)}$ = 4.7 μs is possible

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START/STOP CONDITIONS

If both the data and clock lines are HIGH, the bus is not busy. To attain control of the bus, a start condition is needed from a master; and to release the lines, a stop condition is required.

Start Condition: HIGH-to-LOW transition of the data line while the clock line is in a HIGH state.

Stop Condition: LOW-to-HIGH transition of the data line while the clock line is in a HIGH state.

The master always generates the start and stop conditions. After the start condition the bus is in the busy state. The bus becomes free after the stop condition.

DATA BIT TRANSFER

After a start condition "S" one databit is transferred during each clock pulse. The data must be stable during the HIGH-period of the clock. The data line can only change when the clock line is at a LOW level.

Normally each data transfer is done with 8 data bits and 1 acknowledge bit (byte format with acknowledge).

ACKNOWLEDGE

Each data transfer needs to be acknowledged. The master generates the acknowledge clock pulse. The transmitter releases the data line (SDA = HIGH) during the acknowledge clock pulse. If there was no error detected, the receiver will pull down the SDA-line during the HIGH period of the acknowledge clock pulse.

If a slave receiver is not able to acknowledge, the slave will keep the SDA line HIGH and the master can then generate a STOP condition to abort the transfer.

If a master receiver keeps the SDA line HIGH, during the acknowledge clock pulse the master signals the end of data transmission and the slave transmitter release the data line to allow the master to generate a STOP-condition.

ARBITRATION

Only in multimaster systems.

If more than one device are potential masters and more than one desires access to the bus, an arbitration procedure takes place: if a master transmits a HIGH level and another master transmits a LOW level, the master with the LOW level will get the bus and the other master will release the bus; and the clock line switches immediately to the slave receiver mode. This arbitration could carry on through many bits (address bits and data bits are used for arbitration).

FORMATS

There are three data transfer formats supported:

— Master transmitter writes to slave receiver; no direction change

— Master reads immediately after sending the address byte

— Combined format with multiple read or write tranfers.

ADDRESSING

The 7-bit address of an I^{2}C device and the direction of the following data is coded in the first byte after the start condition:

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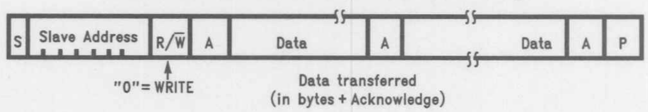
A "0" on the least significant bit indicates that the master will write information to the selected Slave address device; a "1" indicates that the master will read data from the slave. Some slave addresses are reserved for future use. These are all addresses with the bit combinations 1111XXX and 0000XXX. The address 00000000 is used for a general call address, for example, to initialize all I^{2}C devices (refer to I^{2}C bus specification for detailed information).

Master Transmits to Slave, No Directon Change



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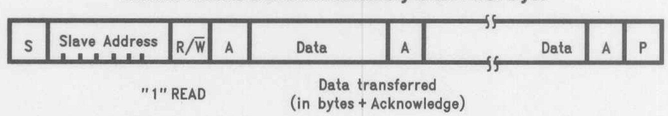
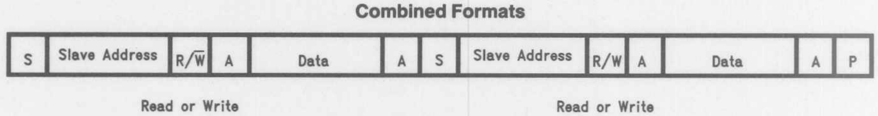
Master Reads Slave Immediately after First Byte



TL/D/11268–5

The master becomes a master receiver after first ACK

Combined Formats



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n bytes Data + ACK   n bytes Data + ACK

S = Start Condition   A = Acknowledge   P = Stop Condition

FIGURE 3. I^{2}C-Bus Transfer Formats

TIMING

The master can generate a maximum clock frequency of 100 KHz. The minimum LOW period is defined as 4.7 μs; the minimum HIGH period width is 4 μs; the maximum rise time on SDA and SCL is 1 μs; and the maximum fall time on SDA and SCL is 300 ns.

Figure 4 shows the detailed timing requirements.

Symbol	Parameter	Min	Max	Units
t_{SCL}	SCL Clock Frequency	0	100	kHz
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μs
t_{HD}; STA	Hold Time Start Condition. After this Period the First Clock Pulse is Generated	4.0		μs
t_{LOW}	The LOW Period of the Clock	4.7		μs
t_{SU}; STA	Setup Time for Start Condition (Only Relevant for a Repeated Start Condition)	4.7		μs
t_{HD}; DAT	Data in Hold Time	5 0*		μs μs
t_{SU}; DAT	Setup Time Data	250		ns
t_r	Rise Time of Both SDA and SCL Lines		1	μs
t_f	Fall time of Both SDA and SCL Lines		300	ns
t_{SU}; STO	Setup Time for Stop Condition	4.7		μs

*Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

FIGURE 4. I²C-Bus Timing Requirements

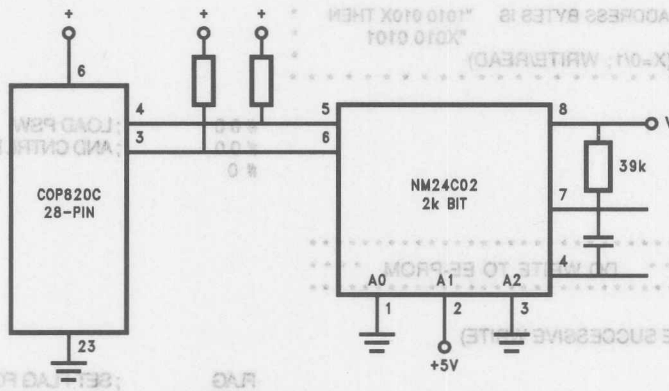

FIGURE 5. I²C Bus EEPROM/μController Configuration Used for Sample Code

SOFTWARE TASKS

I. Write fixed values to E2PROM cells

II. Read values back from E2PROM and save in RAM locations from COP

Note: I²C Bus Modes Used:

Master Transmitter $\xrightarrow{SDA}$ $\xrightarrow{SCL}$ Slave Receiver

Master Receiver $\xleftarrow{SDA}$ $\xrightarrow{SCL}$ Slave Receiver

REMARKS

— The I²C bus, 2-wire serial interface generally requires a pull-up resistor on the SDA line and the SCL line, depending on whether TTL or CMOS hardware interfacing exists.

— I²C bus compatible μC's or peripherals have OPEN DRAIN outputs at SDA and SCL.

— COP800 does not have OPEN DRAIN outputs, but the "bus requirements" can be met by switching SDA and SCL connections into TRI-STATE® for the following cases:

The bus is not accessed

A slave has to send an acknowledge bit.

— MICROWIRE can not be used for I²C bus operations.

— Current sink capability on SDA and SCL must be 3 mA to maintain "Low Level" (an I²C bus spec.).

```
.TITLE IIC - EEPROM   ROUTINES'
.INCLD COP800.INC
.CHIP 840
.LIST X '21

          * * *TASK RELATED RAM - DECLARE* * *

EEADR                              = 002     ; ADDRESS OF EEPROM
EEWRD                              = 003     ; WORD ADDRESS EEPR.
EEDAT1                             = 004     ; DATA TO EECELL
EEDAT2                             = 005     ; SECOND BYTE
FLAG                               = 010     ; FLAG–WORD
EEREAD                             = 012     ; READ–DATA FROM EE
                                   = 013     ; SECOND BYTE
                                   = 014     ; THIRD BYTE
                                   = 015     ; FOURTH BYTE
BITCO                              = 0F0     ; COUNTER FOR BITSHFT

INIT:
    LD SP,                         #06F
    LD B,                          PORTLD    ; INIT LS, L3 FOR EE-
    LD  [B+],                      #00C      ; OPERATIONS
    LD  [B],                       #00C
    LD B,                          #EEDAT2   ; INIT RAMS
    LD  [B-],                      #034      ; FIXEED VALUES FOR
    LD  [B-],                      #012      ; EEWRITE (2 BYTES)
    LD  [B-],                      #0A0      ; MIRROR OF #05
    LD  [B]                        #025      ; MIRROR OF "A5"

        ;* * * * * * * * * * * * * * * * * * * * * * * * * *
        ; EXAMPLE: IF ADDRESS BYTES IS    "1010 010X THEN   *
        ; STORE:                          "X010 0101        *
        ; INTO RAM (X=0/1; WRITE/READ)                      *
        ;* * * * * * * * * * * * * * * * * * * * * * * * * *

    LD PSW,                        #00       ; LOAD PSW
    LD CNTRL,                      #00       ; AND CNTRL REG.
    LD FLAG,                       #0
    .FORM

            ; * * * * * * * * * * * * * * * * * * * * * * *
            ; * * * *   DO WRITE TO EE-PROM   * * * *
            ; * * * * * * * * * * * * * * * * * * * * * * *
            ;

            ; (2 BYTE SUCCESSIVE WRITE)

    SBIT 0,                        FLAG      ; SET FLAG FOR WRITE
    LD B,                          PORTLD    ; POINT LPORT DAT REG.
                                             ; TO MODIFY "SDA, SCL"
    RBIT 2 [B],                              ; PREPARE FOR START
    JSR STACON                               ; CONDITION.
    JSR WAIT                                 ; AFTER WRITE TO EE.
                                             ; WAIT FOR > THAT 40
```

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```
                ; ******************************
                ; ** DO THE START CONDITION  **
                ; ** AND SHIFT OUT ADRESS -  **
                ; ** BYTE AND WORD–ADRESS    **
                ; ******************************
STACON:
    RBIT 3,                       PORTLD    ; FINISH START COND.
    LD B,                         #EEADR    ; PREPARE TO CLOCK
                                            ; OUT ADDRESS.
LOPA:
    LD BITCO,                     #008      ; DO SETS OF 8 BITS

LOPA 1:
    IFBIT 0, [B]                            ; SWITCH SDA BEFORE
    JP ONE,                                 ; SCL
    RBIT 2,                       PORTLD    ; SET BIT LEVLE "0"
    JP CLK

ONE:
    SBIT 2,                       PORTLD    ; SET BIT LEVEL "1"
    JP CLK                                  ; ENSURE SAME BIT
                                            ; LENGTH

CLK:
    SBIT 3,                       PORTLD    ; DO CLOCK PULSE
    NOP
    NOP
    RBIT 3,                       PORTLD    ; ENSURE> 4USEC
    RBIT 2,                       PORTLD    ; SWITCH ALSO SDA LOW
    .FORM

    LD A, [B]                               ; ROTATE BYTE ONE
    RRC A,                                  ; BIT POS. RIGHT
    X A, [B]                                ; AND SAVE
    DRSZ BITCO                              ; CHECK IF 8 BITS
    JP LOPA1,                               ; SHIFTED
    LD A, [B+],                             ; DECREMENT 8
    IFBIT 1,                      FLAG      ; CHECK IF READ
    JMP,                          GETDAT    ; 3RD BYTE IS NEXT?
                                            ; IF SO, THEN READ.
    JSR ACK,                                ; GET ACKNOWLEDGED
                                            ; WHEN 8 BITS ARE
                                            ; SHIFTED.
    IFBIT 0,                      FLAG      ; CHECK IF READ
    JP CEC1,                                ; OR WRITE OPERATION.
    IFBNE                         #04       ; ON READ (HERE)
    JMP LOPA,                               ; IF NOT 2 BYTES YET
    RET                                     ; AFTER EE-ADDRESS AND
                                            ; WORD ADDRESS ARE SHFT.

CEC1:
    IFBNE,                        #06       ; 1ST AND 2ND DATA-
    JMP LOPA,                               ; BYTE (3RD + 4TH)
```

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4

```
                                                          ;NSEC TO PROPERLY
                                                          ;ERASE WRITE.
LD B,                                   #EEDAT2           ; INIT RAMS
LD  [B-],                               #078              ; ANOTHER 2 BYTES
LD  [B-],                               #056              ; OF FIXED DATA
LD  [B-],                               #0E0              ; MIRROR OF #07
LD  [B],                                #025              ; MIRROR OF "A5"
LD B,                                   PORTLD            ; POINT LPORT DAT REG.
               ; TO MODIFY "SDA, SCL"
RBIT 2, [B],                                              ; PREPARE FOR START
JSR STACON,                                               ; CONDITION.
JSR WAIT,                                                 ; AFTER WRITE TO EE
                                                          ; WAIT FOR > THAN 40
                                                          ;MSEC TO PROPERLY
                                                          ; ERASE WRITE.
.FORM

        ;*********************************
        ;****  DO READ FROM EE-PROM  ****
        ;*********************************

        (READ 4 SUCCESSIVE BYTES)
RBIT 0                                  FLAG              ; INDICATE READ
LD B,                                   #EEWRD            ; INIT RAMS
LD  [B-],                               #0A0              ; MIRROR OF #05
LD  [B],                                #025              ; MIRROR OF "A5"

        ;*********************************
        ;** FIRST 2 BYTES SAME AS IF WRITE **
        ;*********************************

                            (IN TERMS OF TRNSMIT)
LD B,                                   #PRTLD            ; PREPARE
RBIT 2 [B]                                                ; FOR
JSR STACON,                                               ; START COND.
                                                          ; AND SHIFT 1ST
                                                          ; 2 BYTES.
SBIT 2,                                 PORTLD            ; PREPARE FOR
NOP,                                                      ; ANOTHER START-
NOP,                                                      ; CONDITION,
SBIT 3,                                 PORTLD            ; SDA HIGH FIRST.
SBIT 1,                                 FLAG              ; INDICATE THAT
                                                          ; 3RD BYTE IS NEXT
LD B,                                   #EEWRD            ; INIT RAMS
LD  [B-],                               #0A0              ; MIRROR OF #05
LD  [B],                                #0A5              ; MIRROR OF "A5"
                                                          ; PERFORM ANOTHER
RBIT 2, [B],                            PORTLD            ; START
JSR STACON
RBIT 1,                                 FLAG
JMP INIT                                                  ;CLOSE THE LOOP WHEN
.FORM                                                     ;FINISHED
```

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```
STP:
    SBIT 3,                 PORTLD      ; ESTABLISH STOP-
    NOP,                                ; CONDITION
    SBIT 2,                 PORTLD
    RET,
    .FORM

        ***********************************
        ; ** GET 8BIT OF DATA FROM EE-PROM **
        ***********************************

GETDAT:
    JSR ACK,                            ; GET ACKNOWLEDGMENT
    LD B,                   #EEREAD     ; POINT FIRST READ RAM
    JP                      GETDT1      ; AND READ IN

GETDAT:
    JSR ACK,                            ; ACKNOWLEDGMENT TO EE-
                                        ; PROM WHEN 8 BITS
                                        ; ARE SHIFTED IN.

GETDAT1:
    LD BITCO,               #008        ; INIT BIT COUNTER
    RBIT 2,                 PORTLC      ; BEFORE READING, PUT
    RBIT 2,                 PORTLD      ; 'SDA' INTO HIGH-Z.

LOPB:
    SBIT 3,                 PORTLD      ; DO CLOCK HIGH
    RBIT 7, [B]                         ; READ IN EEDATA
    IFBIT 2,                PORTLD      ; IN SETS OF 8 BITS
    SBIT 7, [B]
    RBIT 3,                 PORTLD      ; DO CLOCK LOW
    DRSZ BITCO,                         ; CHECK IF 8 BITS
    JP SHFT                             ; ARE SHIFTED
    LD A, [B+],                         ; INCREMENT B
    IFBNE                   #06         ; CHECK IF 4 BYTES
    JMP GETDT,                          ; ARE SHIFTED IN?
    SBIT 2,                 PORTLC      ; PUT L2=0
    JMP STP                             ; WHEN TRUE, DO STOP
                                        ; CONDITION AND
                                        ; RETURN

    .FORM

SHFT:
    LD A, [B],                          ; ROTATE BITS ONE
    RRC A                               ; POSITION RIGHT
    X A, [B]
    JP LOPB

        *************************************
        ; ** SIMPLE ROUTING TO DO 40 MSEC DELAY **
        *************************************
```

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```
LOPD:
    LD 0F2,                          #OFF        ; TO PRODUCE>40MSEC
                                                 ; TIMEOUT
LOPC:
                                                 ; TO PROPERLY PROGRAM
    DRSZ 0F2,                                    ; EEPROM. TIME REQUIRED
    JP LOPC,                                     ; TO ERASE/WRITE
    DRSZ0F1,                                     ; THE EEPART.
    JP LOPD
    RET

ACK1:
    SBIT 2,                          PORTLC      ; INDICATE TO EE-PROM
    JP ACLK,                                     ; (PUT DATA LINE LOW)

ACK:
    RBIT 2,                          PORTLC      ; PUT DATA-LINE HI-Z

ACLK:
                                                 ; AND GET ACKNOWLEDGE
    SBIT 3,                          PORTLD      ; 8 BITS ARE SHIFTED,
    NOP                                          ; DO A DUMMY CLOCK
    NOP
    NOP
    RBIT 3,                          PORTLD      ; (FOR ACKNOWLEDGE)
    SBIT 2,                          PORTLC
    RET
    .END
```

TL/D/11268–13

EEPROMs

Abstract: National's new NM25C04 serial EEPROM can write from 1 to 4 bytes at a time and has a sequential read capability. The command protocol is straight forward and byte-oriented. The result is a serial EEPROM to be taken seriously for any application not using a microcontroller with a dedicated MICROWIRE™ interface

What is SPI?

The Serial Peripheral Interface (SPI) is a general purpose synchronous serial interface originally found on certain Motorola microcontrollers. A virtually identical interface can now be found on certain TI and SGS Thompsen microcontrollers as well. The SPI should not be confused with the SCI (Serial Communications Interface) frequently also found on the same microcontrollers but usually used for asynchronous communications.

Since Many SPI Protocols are Possible, What Convention has been Adopted for the EEPROM?

Unlike the MICROWIRE and Inter-Integrated Circuit (IIC) serial buses, the Serial Peripheral Interface (SPI) does not completely define a data transfer protocol. National's 25Cxx SPI EEPROM interface convention assumes that the Motorola Microcontroller's SPI registers are set with:

Clock Phase Bit = 1
Clock Polarity Bit = 0

These same settings are usable for the SPI interfaces found on other manufacturer's microcontrollers as well. In this data transfer convention, Slave Selects reset the serial logic between transfers. The Slave Selects are asserted low. Data transfer lengths are multiples of 8-bit bytes.

Reads and writes to the EEPROM are initiated by enabling the device by asserting the Slave Select pin low and shifting an opcode and address fields to the EEPROM *(Figure 2)*. This requires 16 bits of data or two full transfers from the 8-bit data register on the microcontrollers SPI. For write operations this is followed by one to four bytes of the data to be written. The write operation is internally self-timed and begins when the Slave Selects become low. For read operations the address is answered by bytes of data on the SO pin starting from the address requested and sequencing upward as many times as is desired, wrapping around at the end of the memory array.

NATIONAL'S NM25C04 EEPROM FEATURES AND OPERATION OVERVIEW

- 512 x 8-bits
- Write protect pin
- No need to pre-erase locations before write
- One to four byte block write—wraps at end of four byte memory blocks
- Unlimited sequential read—wraps at end of memory array
- Four zone software initialized write protection to prevent unintended overwrites to reserved areas
- Internally self-timed write cycles
- Write cycle ready/busy indication via polling internal status register—does not tie up the output bus during write timeout

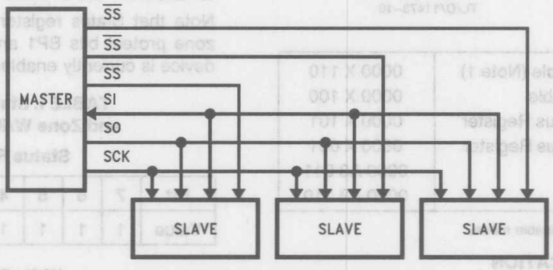
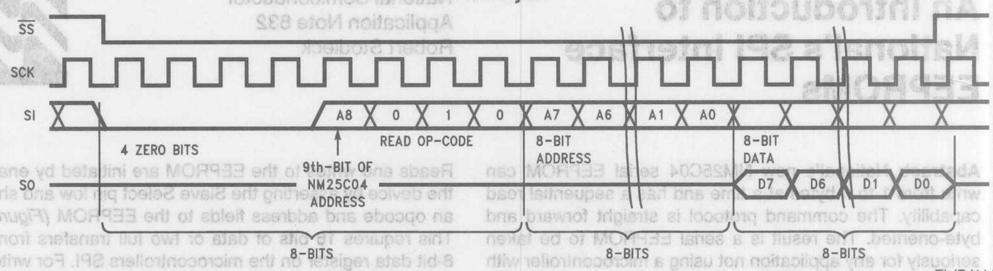


FIGURE 1. The physical Serial Peripheral Interface definition is very similar to National's MICROWIRE. "Slave" Selects, Serial Clock, Slave In (SI), Slave Out (SO). The SPI interface can also be used to access MICROWIRE devices.

Read Cycle



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Write Cycle

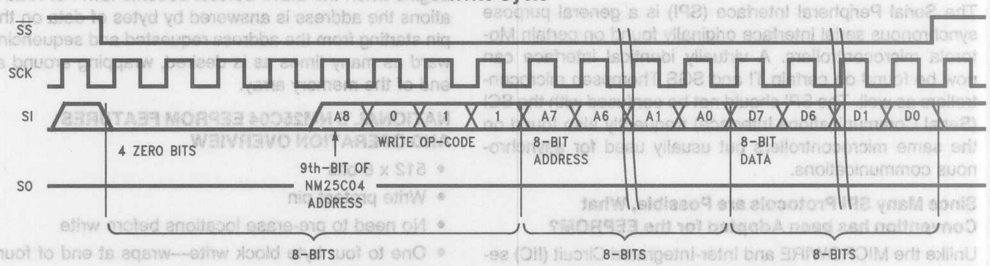

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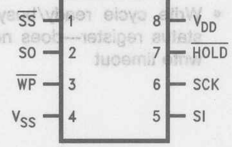
FIGURE 2. National's SPI EEPROM byte-oriented read and write cycle conventions. Note that the read cycle can be extended and data bytes from sequential bytes will be output. Write cycles can actually include 1 to 4 bytes to be written into a 1 to 4 location "block".

- Clock gate pin (hold)
- Slave In (SI)
- Slave Out (SO)
- Slave Select (SS)
- Serial Clock (SCK)
- Serial Transfer Hold (HOLD)
- Write Protect (WP)



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OPCODES

WREN	Write Enable (Note 1)	0000 X 110
WRDI	Write Disable	0000 X 100
RDSR	Read Status Register	0000 X 101
WRSR	Write Status Register	0000 X 001
READ	Read	0000 A8 011
WRITE	Write	0000 A8 010

Note 1: Part powers up in write disable mode.

WRITE COMPLETE INDICATION VIA STATUS REGISTER

All EEPROMs have write cycles that are far longer than normal read cycles. Since writes are always relatively infrequent, it is often possible to simply wait out this time period before proceeding with other operations. However, the read status register opcode provides a method of polling for the end of write indication that does not force the processor to wait before proceeding to another operation. In fact, the only time it is absolutely required that one check the write complete status is prior to another read or write attempt. Unlike most serial EEPROMs this is practical on the NM25C04 by the read status register (RDSR) operation (see Table I). The RDY bit in the status register is low if the EEPROM has completed all write operations and is ready for another read or write.

Note that Status register also provides the status of the zone protect bits BP1 and BP0, and reveals whether the device is currently enabled for writing the WEN bit.

TABLE I. Status Register Format and Zone Write Protection Ranges

Status Register Format

Bit	7	6	5	4	3	2	1	0
Value	1	1	1	1	BP1	BP0	WEN	RDY

Write Protect Ranges

BP1	BP0	Write Protected Range
0	0	None
0	1	180–1FF
1	0	100–1FF
1	1	000–1FF

4

BLOCK WRITE AND SEQUENTIAL READ

One to four bytes can be written within a "block" boundary. The first write "block" is at addresses 0 to 3, the second is at addresses 4 to 7 etc. The block to be written to is loaded in one sequence by simply loading an additional byte after the first byte shown in the *Figure 2* write cycle example. If address "0" were requested and four bytes are sent, the first byte will go to address zero and the second would go to address two etc. If address "3" were requested and two bytes are sent, the first byte will go to address three and the second would wrap around the block boundary and be written to address zero. Block write allows four bytes at a time, thus reducing the average write time. This is sometimes important due to the very long inherent write cycle times of EEPROMs.

Sequential read allows successive bytes to be read out of the EEPROM without having to re-send a read opcode or address for each new byte. This feature allows significant improvements in the average read access time for multibyte data. The entire length of memory can be read in one operation if required. The read sequence will wrap back to location zero if read past the end of memory.

WRITE PROTECT FEATURES

EEPROMs operate on 5V supplies and do not require a separate high-voltage supply to execute write operations. This is a primary feature of EEPROMs but inherent in this capability are some unique problems as well. Since they can be programmed on board and data in memory is non-volatile, accidental overwrite is a constant possibility. Unlike the majority of components on a typical PC board, the non-volatile characteristic assures that the problem will not correct itself after reset or power down. These problems are far less common in serial I/O devices than in parallel EEPROMs but it remains a serious issue. Thus a number of write protect strategies can be supported on the NM25C04.

SOFTWARE WRITE ENABLE/DISABLE

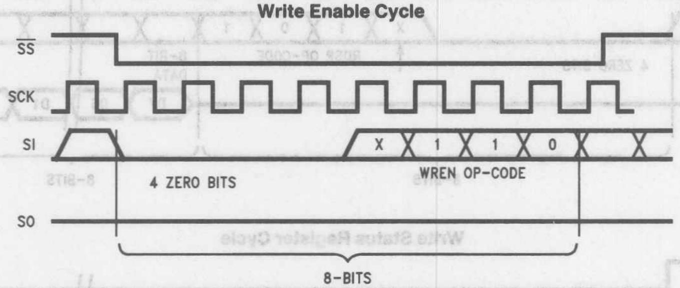
All of National's Serial EEPROMs power up in a write disable state to prevent accidental writes in the noise of the power-up operation. In order to actually write to the device, a write enable instruction must be sent to the EEPROM before a write instruction can be successfully executed. This is the function of the **WREN** (WRite ENable) instruction. The write function can be disabled again with the **WRDI** (WRite DIsable) instruction. The requirement that one execute a write enable instruction before an actual write operation greatly reduces the probability of a random noise induced write over. It can also be used to manage software related problems or to assist in debug.

ZONE WRITE PROTECTION

The NM25C04 has the ability to disable writes via software to certain areas of EEPROM. This is done with the **WRSR** (WRite Status Register) instruction. The write protect ($\overline{WP}$) pin must be high to allow writes to the status register and the **WRSR** instruction must **always** be preceded by a WREN (WRite ENable) instruction. Execution of the WRSR instruction always places the device in the write disable state. Thus the WREN instruction **must** be executed before any further writes to the EEPROM can occur.

The values in two non-volatile bits of the status register control whether the higher ¼, the higher ½, or the entire array is rendered unwritable. This write protection feature is under software control but is non-volatile. Protected areas become read only memory. The **RDSR** (ReaD Status Register) instruction allows the state of the write disable bits and the write status bits to be read. The two non-volatile write protect bits are writable via the **WRSR** (WRite Status Register) instruction. They may be altered repeatedly.

Write Enable Cycle



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Write Disable Cycle

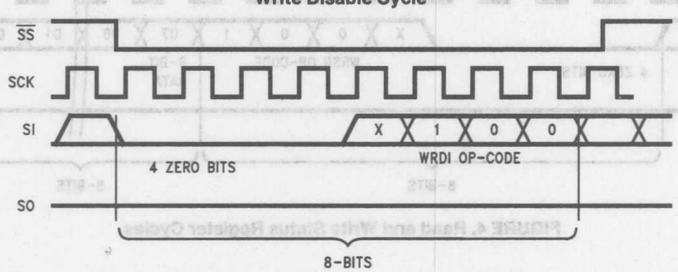

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FIGURE 3. Read and Write Status Register Cycles

WRITE PROTECT PIN

The write protect pin provides a hardware method of preventing writes. The write protect pin must be high to allow normal writes to the EEPROM or to the status register. The uses of this pin are numerous. A manufacturer may use it to prevent a serial number, date of manufacture, security code or similar information from being altered intentionally or unintentionally in the field. Thus the EEPROM may be pre-programmed in a programmer prior to assembly. Once installed in the PC board with the write protect pin tied low, the data in the EEPROM is permanent. Calibration data can be made to be alterable only in the factory or by a field engineer by controlling the write protect pin with a jumper or internal switch.

One of the more subtle problems is the possibility of overwrite in a microcontroller "crash". Microcontrollers are easily upset by V_{CC} transients caused by such things as relay or electric motor operation, intermittent power switch operation or battery replacements, etc. V_{CC} transients can induce glitches on reset, interrupt or clock lines but the result is generally similar, that is, the microcontroller's program counter will be upset. The microcontroller will leave its normal program sequence and begin running at an arbitrary program memory location. One of the possible "landing" sites is the code associated with writing the serial EEPROM. Since microcontroller address spaces are often quite small this is a serious possibility, especially if the transients are a common occurrence. Badly designed reset circuits can aggravate or cause this problem. This type of event can also defeat software based write protect strategies. The write protect pin can be used to safeguard against this type of problem.

WRITE PROTECT PIN APPLICATIONS EXAMPLES

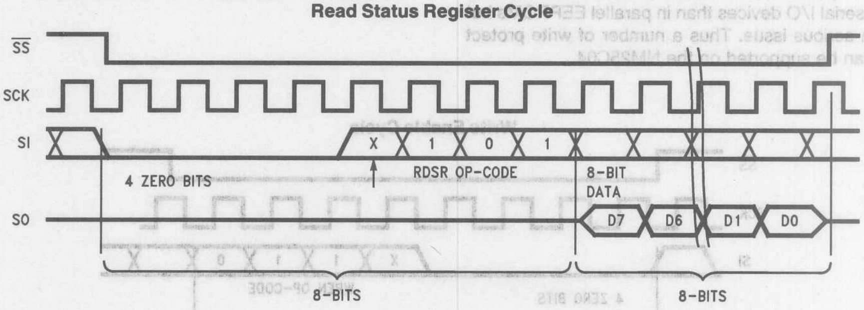
Oven or Refrigerator Temperature Controller *(Figure 5)*

A temperature controller uses an EEPROM to record both set point and calibration information. Use of the EEPROM to record the set temperature prevents loss of the set temperature if the unit is shut off. Calibration data for the temperature sensor is also recorded in EEPROM initially at the factory but may be recalibrated by a technician in the field. In the interests of compactness and economy the microcontroller is located in close proximity to an electromagnetic relay used to control a larger off-board power relay which actually switches power on or off to a heater or refrigeration unit. This is the only output required from this board.

In this design the power relay shares the same power cord as the digital logic board. This is the normal case for refrigerators and ovens. The power line is subject to numerous transients types not the least of which is caused by the routine turn-on and turn-off of the relays, heating elements or cooling systems of the appliance itself, but which also includes lightning, outages, imperfectly inserted cords and etc. Thus it is impossible to guarantee that the on-board microcontroller will run faultlessly throughout its service life. The problem is not that a destructive microcontroller malfunction is particularly probable, the problem is that such an event need only occur once to corrupt the data in the EEPROM and cause problems.

If the microcontroller "crashes" it is a simple matter to unplug the unit to reset the controller. In fact a simple watch dog timer can reset the microcontroller routinely so that such an event will not even be noticed. But it is possible that the calibration data or set point data in the EEPROM will be

Read Status Register Cycle



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Write Status Register Cycle

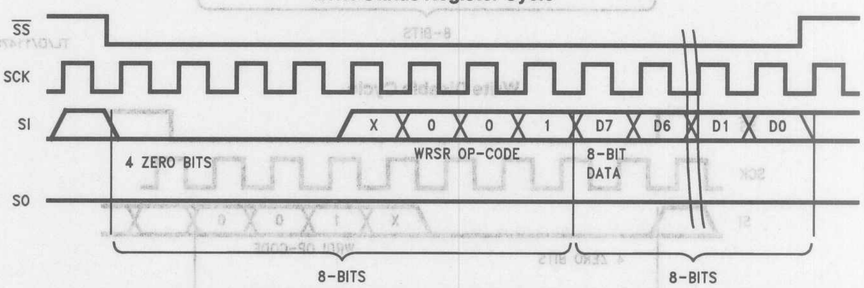

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FIGURE 4. Read and Write Status Register Cycles

overwritten in such a crash. This may be true almost regardless of what software protection schemes are in place. And of course the non-volatile EEPROM will not "forget" the data from the transient event after powerdown or reset.

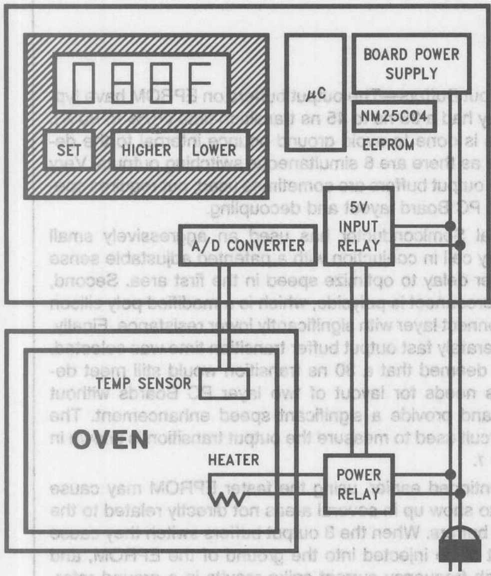

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FIGURE 5. Simple Temperature Controller in an Oven Application

A fix to this problem is to hardwire the Write Protect pin to a switch or push button that must be closed manually any time the values in the EEPROM are to be updated. i.e., when changing the temperature set point or re-calibrating the controller (See Figure 6).

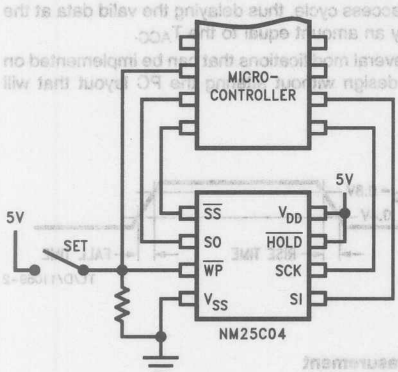

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FIGURE 6. Using National's SPI EEPROM Write Protect Pin and a Mechanical Switch to Safeguard Critical Data

The more obvious approach of simply allowing the microcontroller to read the set switch and handle the write operation to the EEPROM should be avoided. This approach introduces the danger of subjecting the EEPROM to unintended writes from a temporarily wayward microcontroller.

Auto Cassette Deck Security Code Application

Auto Cassette Decks sometimes employ an anti-theft scheme requiring that the owner enter a security code into the unit from a keypad on the front panel before the unit can be used. In practice the actual security code is typically resident in a serial EEPROM. The initial code is entered at the factory and in some cases may be changed by the owner who has to know the original code in order to change the code.

The application problem has many similarities to the temperature controller example. It is important not to corrupt the data in the EEPROM. To do so would deny use of the cassette player to its owner. The power supply to the player is prone to transient events. The motors and control elements on the deck create V_{CC} transients and the car itself creates predictable power supply catastrophes. Cranking the car on a low battery, battery replacement and the inevitable jump start to name a few.

The fix is precisely the same as the temperature controller example. That is a mechanical switch can be used to enable writes, via the Write Protect pin, only at the time when a change is clearly intended by the user.

CLOCK GATING PIN ($\overline{\text{HOLD}}$)

For those applications where the EEPROM may be interfaced to relatively simple logic, a clock gating pin has been provided. Transitions of the $\overline{\text{HOLD}}$ pin must be restricted to times when the clock pin is high to avoid clock glitches. (This is a simple AND gate.)

SUMMARY

National established the standard for serial EEPROM devices with the NM93CXX MICROWIRE family. National offers a variety of devices and interface options. The SPI NM25CXX family devices offer designers new choices for varied applications. The feature set of this new family makes it suitable for any application that does not use a microcontroller with a dedicated IIC or MICROWIRE interface.

Designing with National's High Performance CMOS EPROM

National Semiconductor
Application Note 717
Paul Lubeck

INTRODUCTION

The purpose of this application note is to inform the system designer of possible pitfalls of using high speed EPROM. In older generation EPROM the fastest commonly available data access times were 150 ns and 100 ns, but with the current generation EPROM, data access times of less than 100 ns are common, and this is true of National Semiconductor's family of 1.2 micron (0.9 Leff) EPROM. This family of EPROM is differentiated from other National EPROM by using a part number prefix of NM rather than NMC. For availability of specific part numbers and speeds contact your local National Semiconductor sales office or franchised distributor.

The problems that are encountered are typically seen as noise on the data-out lines, noise on the data-in lines, or possibly noise on the control signals. The cause of the noise must be understood to truly eliminate it.

In EPROM chip design, there are several ways to decrease the overall data access time. The major areas are:

1. Memory Cell—Designers are always looking for ways to decrease the size of the memory cell as this significantly affects the total die size. Typically as the memory cell becomes smaller, the cell current becomes less, and as the cell current becomes lower, the delay at the sense amplifier has to be increased to assure correct data is being read. On the other side of the issue, overall smaller die sizes and smaller geometries bring higher speed, therefore the actual speed improvement realized depends on the design.
2. Interconnect Technology—By decreasing the resistance of the poly-silicon interconnects lines in the EPROM, the device can be significantly faster. This is one of the few speed enhancements that doesn't carry a significant penalty in some other area.
3. Output Buffers—The output buffers on EPROM have typically had a 35 ns to 45 ns transition time (10% to 90%). This is done to avoid ground bounce internal to the device as there are 8 simultaneous switching outputs. Very fast output buffers are sometimes used, but requires specific PC Board layout and decoupling.

National Semiconductor has used an aggressively small memory cell in conjuction with a patented adjustable sense amplifier delay to optimize speed in the first area. Second, the interconnect is polycide, which is a modified poly silicon interconnect layer with significantly lower resistance. Finally, a moderately fast output buffer transition time was selected. It was deemed that a 30 ns transition would still meet designers needs for layout of two layer PC Boards without noise and provide a significant speed enhancement. The test circuit used to measure the output transition is shown in *Figure 1.*

As mentioned earlier, using the faster EPROM may cause noise to show up in several areas not directly related to the output buffers. When the 8 output buffers switch they cause current to be injected into the ground of the EPROM, and this high frequency current spike results in a ground reference that is not the same at all points within the EPROM. As a result of this "ground bounce" the reference for the inputs into the EPROM is temporarily altered. There is sufficient margin built into the EPROM to account for this internal noise and still meet the specification, although if the input signals are marginal or the ground to the EPROM is highly inductive the inputs are likely to detect a transition. A transition on the address inputs will cause the EPROM to begin a new data access cycle, thus delaying the valid data at the Q outputs by an amount equal to the T_{ACC}.

There are several modifications that can be implemented on an existing design without altering the PC layout that will

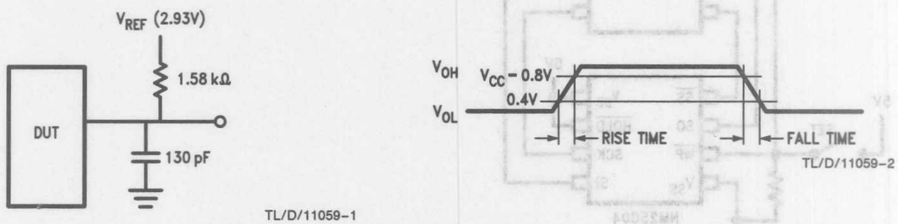

FIGURE 1. Output Transition Time Measurement

overcome the problem, although the best solution is to use these modifications in the circuit design as well as follow some specific PC layout rules. The non-layout modifications are as follows:

1. Improve the input high voltage levels to the EPROM. The goal of this modification is to provide as much V_{IH} margin as possible so that more ground bounce can be tolerated. This can be accomplished in several ways. Many systems use a resistor from the signal line to V_{CC} to avoid oscillation while the line is in the high impedance mode (or in the case of a OC output the resistor is mandatory). If the minimum V_{IH} observed is at or near the specified 2.0V V_{IH} of the EPROM (it should be at 2.4V minimum for reasonable margin and system to system variation) the pull-up resistor value should be decreased. Most output drivers (1.2 mA) can guarantee a good V_{IL} with a 4.7 kΩ pull-up resistor, or in the case of an output driver capable of 800 μA a 7 kΩ resistor is a reasonable minimum. It may not be necessary to use such a low value resistor. A minimum value resistor can be selected simply by applying ohm's law as follows:

$$\frac{\text{Max } V_{CC} - V_{IL} \text{ of EPROM}}{\text{Max } I_{OL} \text{ of driver} - \text{Max } I_{IL} \text{ of total loads on driver}} = R$$

Max V_{CC} is maximum voltage of the voltage supply to the resistor.

V_{IL} of EPROM is the maximum input low voltage of the EPROM. In this case it is 0.8V. It is good to allow margin so using 0.45V is conservative.

Max I_{OL} of driver is the maximum output low current the driver is capable of at the V_{IL} level assumed above.

Max I_{IL} of total loads on driver is the sum of all currents at the node excluding the current of the resistor.

Using this method a pull-up resistor value can be selected that will aid in providing the best V_{IH} while guaranteeing a V_{IL} with good margin. Since the ground bounce problem is normally a problem that affects the Input High Threshold, the V_{IH} should be given the most margin.

2. A second method of improving V_{IH} to the EPROM and thus making the EPROM more immune to ground bounce is to use latches or drivers that have a better V_{OH}. Many CMOS devices will drive a V_{OH} near V_{CC} making them an excellent choice for this application.

3. Improving the ground connection (making it less inductive) can have significant impact. If the EPROM has a ground connection that is capacitive rather than inductive and is closely coupled to the drivers (in respect to signal and ground), steps 1 and 2 above may not be necessary. To accomplish a low inductive/high capacitive ground supply, each device should have a ceramic capacitor in the range 0.1 μF to 0.47 μF, or similar. In addition there should be a charge storage capacitor electrically close. This should be similar to an aluminum electrolytic in the range of 4.7 μF to 15 μF. *Figure 2* shows a satisfactory 2-layer PC board layout using latches on all address lines. Typically only eight of the address lines will require latches and the other address lines will be directly driven from the micro, this is only to demonstrate a sound layout including capacitors and power connections.

Many systems use dedicated layers in the PC board for V_{CC} and ground. In these systems there is little to be concerned about due to the excellent characteristics of this approach. Equally satisfactory results can also be obtained with routed V_{CC} and ground, but close attention must be given to the result.

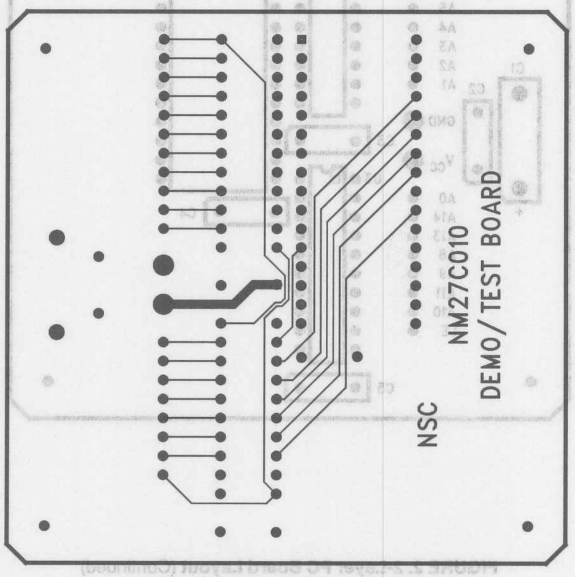

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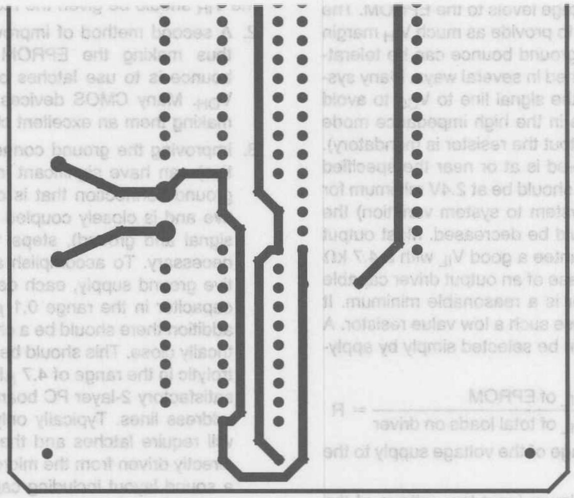
FIGURE 2. 2-Layer PC Board Layout



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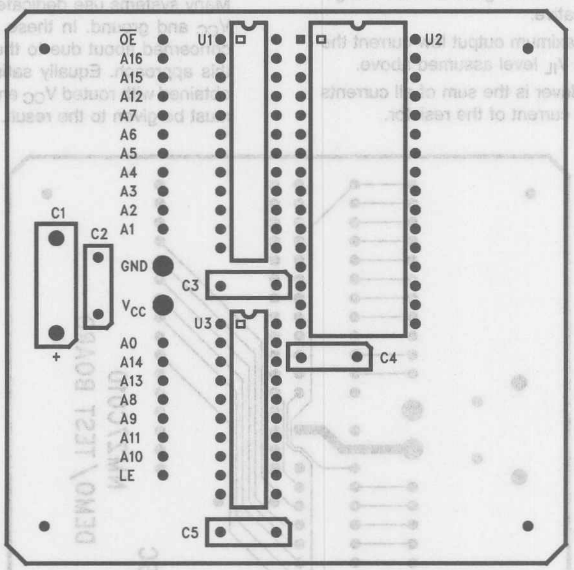

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U1 = DM74ACT

U2 = NM27C010N90

U3 = DM74ACT373N

C1 = 4.7 μF capacitor

C2–C5 = 0.47 μF capacitor

FIGURE 2. 2-Layer PC Board Layout (Continued)

Improves Performance

INTRODUCTION

EPROMs are widely used for non-volatile code/data storage in a variety of systems ranging from computers to instrumentation. A number of applications like laser printer engines and analytical instruments (e.g. spectrometers) rely heavily on look-up tables for their operation. The performance in all such applications can be improved by using high-speed EPROMs and data buffers, which demand a premium price.

National Semiconductor has introduced a new family of EPROMs, called *Processor Oriented EPROMs* (POP), which will improve the performance without requiring faster speed EPROMs. One of the members of POP Family is *Immediate Access EPROMs*. These devices improve the interface to 32-bit popular microprocessors like ’030 and X386.

The POPs improve the interface by addessing two areas: guaranteed data hold time at the end of EPROM access cycle and faster data bus disable time. In this application note we will show how the use of *Immediate Access EPROMs* help in the system performance improvement. Two cases are studied—the first is a 68030-based system and the second is a X386-based system. For each case the design with the standard EPROM and the POP is discussed. It will be shown that to get the same performance as with 120 ns 27P512 (POP), 80 ns (for ’030 design) and 70 ns (for X386 design) 27C512 (standard) EPROMs are required. The general guidelines apply to any standard microprocessor and some microcontrollers.

TARGET APPLICATIONS

- High Performance Computers
- Instrumentation—Look-Up Table Based
- Digital Switch (PBX)
- Laser Printer Engines
- Automotive Controllers

A: 68030-EPROM INTERFACE

Figure 1 shows the block diagram of EPROM interface to 68030-25.

For 68030 CLK input is the specified processor frequency clock and all the timing is specified with respect to CLK. For 25 MHz 68030 CLK period is 40 ns.

The 68030 supports two types of read and write operations—asynchronous and synchronous. Lower performance systems may utilize asynchronous interface, where 8- or 16-bit EPROM data bus is used and multiple transfers are required to fetch a 32-bit operand. Higher performance systems use 32-bit EPROM data bus and do a synchronous data transfer. The fastest synchronous read operation requires two clock cycles for completion as shown in *Figure 2*.

The cycle begins with valid address and control signals on 68030 output pins. The buffered address is applied to the EPROM. The control logic decodes the address and enables the EPROM. After the EPROM access time the data is available for reading to the processor. The control logic issues $\overline{STERM}$ signal to the 68030 to indicate the cycle is over. Due to longer access time for EPROMs, one will have to introduce wait states before $\overline{STERM}$ is returned. Table I defines the relevant AC specifications for the read operation for the 68030. With the basic timing explained let us see what the interface looks like in detail.

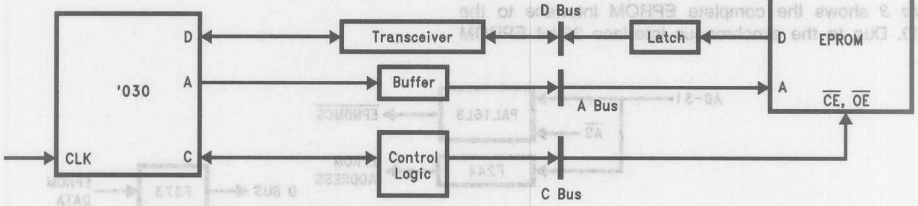

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FIGURE 1. 68030-EPROM Interface Block Diagram

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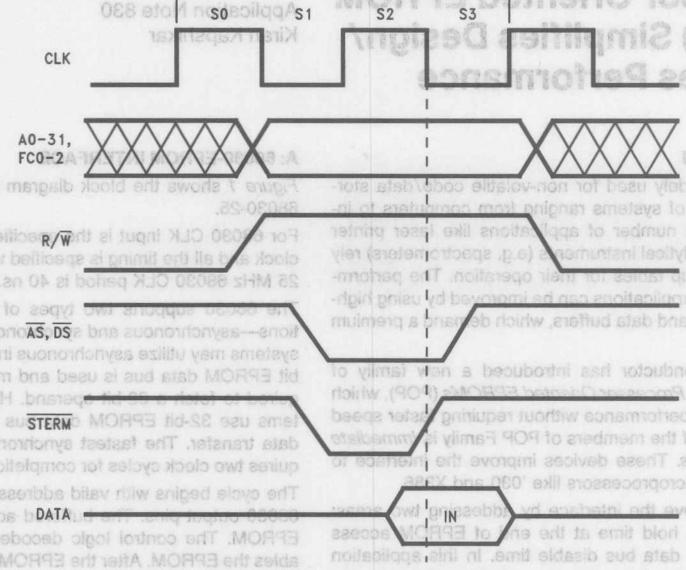

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FIGURE 2. The Fastest Synchronous Read Cycle (68030)

TABLE I. AC Specifications for 68030 Read Operation (Synchronous)

		Min	Max
CLK Period	(t1)	40 ns	80 ns
A0–A31, R/$\overline{\text{W}}$ Valid after Rising Edge of CLK	(t6, t18)	0 ns	20 ns
$\overline{\text{AS}}$, $\overline{\text{DS}}$ Valid after Falling Edge of CLK	(t9)	3 ns	18 ns
D0, D31 Setup before Falling Edge of CLK	(t27)	2 ns	
D0, D31 Hold after Falling Edge of CLK	(t30)	8 ns	

DESIGN WITH STANDARD EPROM

Figure 3 shows the complete EPROM interface to the 68030. Due to the synchronous interface 32-bit EPROM data bus (four 27C512s) is used. The 68030 design requires the use of address strobe ($\overline{\text{AS}}$) signal to qualify the chip selects. The decoder PAL 16L8-7 (7.5 ns delay) uses the address and $\overline{\text{AS}}$ to generate $\overline{\text{EPROMCS}}$. F244 is used to buffer the processor address.

The LATCHENABLE signal latches the EPROM data in F373, so that 68030 data hold time requirements can be met. The output enable signals applied to the EPROM and the F373 are used to enable and disable the data bus. The control PALs use CLK and $\overline{\text{CLK}}$ (inverted CLK) to generate the various control signals. $\overline{\text{EPROMSTERM}}$ indicates the end of EPROM read cycle. The memory controller uses this signal to issue $\overline{\text{STERM}}$ to the processor.

Figure 4 shows the timing diagram for 27C512 read cycle. For a (4 + ½) cycle EPROM access (the '030 reads the data on the falling edge of CLK), 120 ns 27C512s are required as shown in Equation 1.

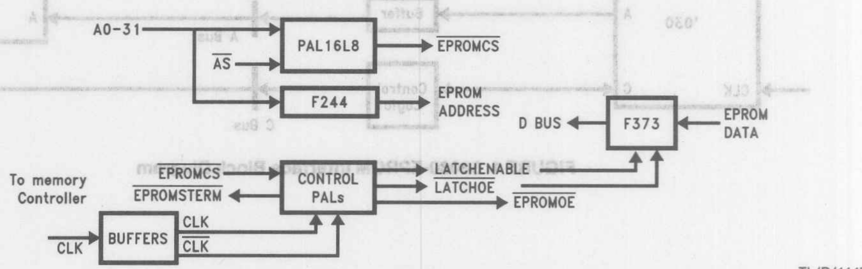

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FIGURE 3. Complete EPROM Interface to 68030

For (n + ½) clock cycle accss the EPROM timing equation is,

t_2	$+ t_9$	$+ \text{Max}\{t_{PAL}, t_{PD}244\}$	$+ t_{ACC}$
½ CLK period	$\overline{\text{CLK}}$ to $\overline{\text{AS}}$ delay	Max {PAL delay, 244 delay}	EPROM access time
$+ t_{PD}$ 373	$+ t_{PD}$ (transceiver)	$+ t_{27}$	$\leq (n + ½) * (t_{CLK})$
latch delay	transceiver delay	data setup time to 68030	

Substituting the values from the 68030 datasheet,

For a 4.5 clock cycle access

$$20 + 18 + 7.5 + t_{ACC} + 5 + 5 + 2 \leq 4.5 * (40) \quad (1)$$

$t_{ACC} \leq 123$ ns

For a 3.5 clock cycle access

$$20 + 18 + 7.5 + t_{ACC} + 5 + 5 + 2 \leq 3.5 * (40) \quad (2)$$

$t_{ACC} \leq 83$ ns

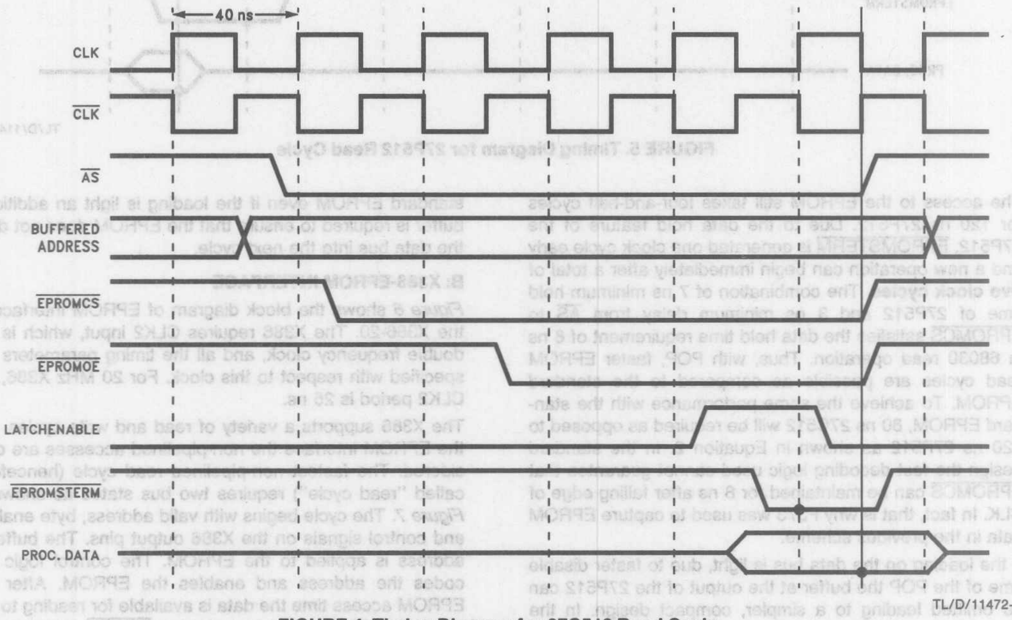

FIGURE 4. Timing Diagram for 27C512 Read Cycle

About 3 ns margin takes care of delays due to trace lengths, clock skews and loading effects. $\overline{\text{EPROMSTERM}}$ is generated during the fifth cycle, to be sampled on the rising edge of CLK in the sixth cycle so that a new operation can begin after a total of **six clock cycles.**

DESIGN WITH POP (27P512—120 ns)

The 68030 Interface to POP looks very much the same as the Standard EPROM interface. Because the Immediate Access EPROM has a minimum of 7 ns hold time, F373 latch is no longer required. A buffer is introduced in place of the F373, assuming a large load on the data bus. $\overline{\text{EPROMSTERM}}$ can be generated one cycle early as compared to the standard EPROM Design. The complete timing diagram is shown in *Figure 5*.

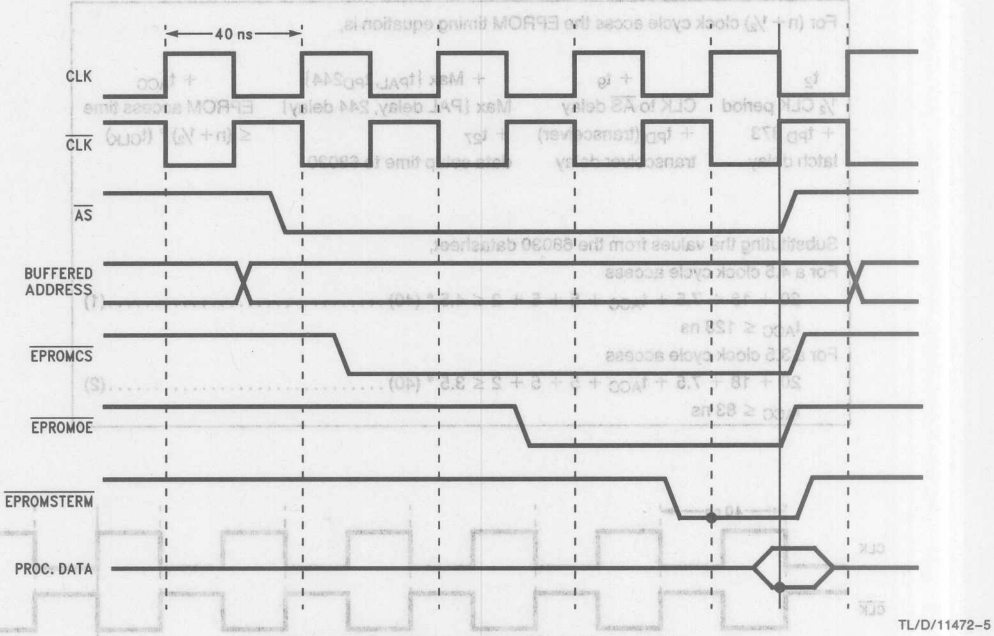

FIGURE 5. Timing Diagram for 27P512 Read Cycle

The access to the EPROM still takes four-and-half cycles for 120 ns 27P512. Due to the data hold feature of the 27P512, $\overline{\text{EPROMSTERM}}$ is generated one clock cycle early and a new operation can begin immediately after a total of **five clock cycles**. The combination of 7 ns minimum hold time of 27P512 and 3 ns minimum delay from $\overline{\text{AS}}$ to $\overline{\text{EPROMCS}}$ satisfies the data hold time requirement of 8 ns in 68030 read operation. Thus, with POP, faster EPROM read cycles are possible as compared to the standard EPROM. To achieve the same pertormance with the standard EPROM, 80 ns 27C512 will be required as opposed to 120 ns 27P512 as shown in Equation 2. In the standard design the fast decoding logic used cannot guarantee that $\overline{\text{EPROMCS}}$ can be maintained for 8 ns after falling edge of CLK. In fact, that is why F373 was used to capture EPROM data in the previous scheme.

If the loading on the data bus is light, due to faster disable time of the POP the buffer at the output of the 27P512 can be omitted leading to a simpler, compact design. In the standard EPROM even if the loading is light an additional buffer is required to ensure that the EPROM does not drive the data bus into the next cycle.

B: X386-EPROM INTERFACE

Figure 6 shows the block diagram of EPROM interface to the X386-20. The X386 requires CLK2 input, which is the double frequency clock, and all the timing parameters are specified with respect to this clock. For 20 MHz X386, the CLK2 period is 25 ns.

The X386 supports a variety of read and write cycles. For the EPROM interface the non-pipelined accesses are considered. The fastest non-pipelined read cycle (henceforth called "read cycle") requires two bus states as shown in *Figure 7.* The cycle begins with valid address, byte enables and control signals on the X386 output pins. The buffered address is applied to the EPROM. The control logic decodes the address and enables the EPROM. After the EPROM access time the data is available for reading to the processor. The control logic issues $\overline{\text{READY}}$ signal to the processor and the cycle is over.

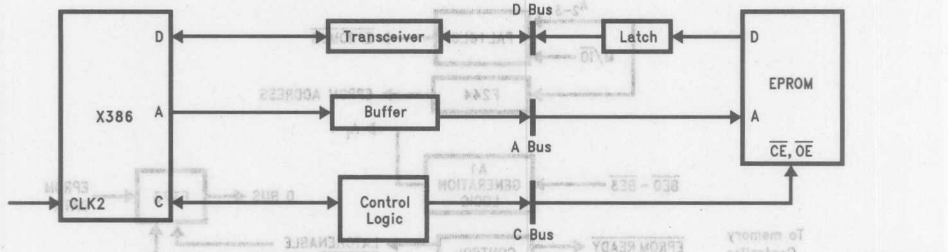

FIGURE 6. X386—EPROM Interface Block Diagram

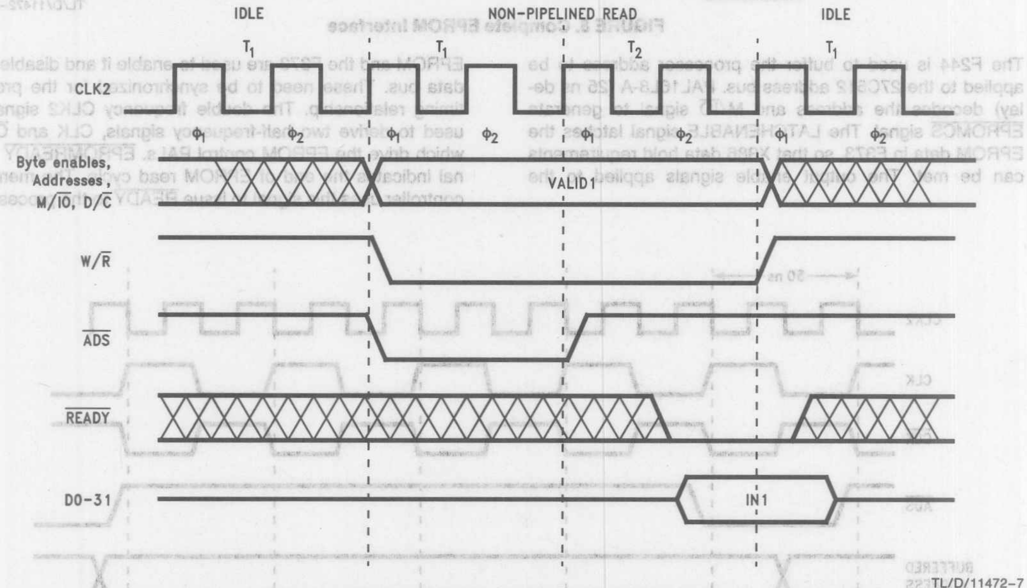

FIGURE 7. The Fastest Non-Piplined Read Cycle

Due to longer access times for EPROM, one will have to introduce wait states before $\overline{\text{READY}}$ is returned. Table II defines the relevant AC specifications for the read operation. With the basic timing explained let us see what the interface looks like in detail.

TABLE II. AC Specification for X386 Read Operation

	Min	Max
CLK2 Period (t1)	25 ns	125 ns
A2–A31, Valid after Rising Edge of CLK2 (Phase 1) (t6)	4 ns	30 ns
W/$\overline{\text{R}}$, M/$\overline{\text{IO}}$ Valid after Rising Edge of CLK2 (Phase 1) (t10)	6 ns	28 ns
D0, D31 Setup before Rising Edge of CLK2 (Phase 1) (t21)	11 ns	
D0, D31, Hold after Rising Edge of CLK2 (Phase 1) (t22)	6 ns	

DESIGN WITH STANDARD EPROM (27C512)

The X386 data bus is 32-bit wide whereas, 27C512 has a 8-bit data bus. A variety of options are possible for interfacing these two different width data buses. The X386 has $\overline{\text{BS16}}$ input, which informs the processor whether the current cycle is a 16-bit cycle or not. By using this input—we can design 16-bit EPROM interface, that uses two 27C512s in parallel. In this case, we need to generate A1, from the byte enables ($\overline{\text{BE0}}$–$\overline{\text{BE3}}$). The A1 generation logic is not shown, but can be derived easily. The interface is shown in *Figure 8*.

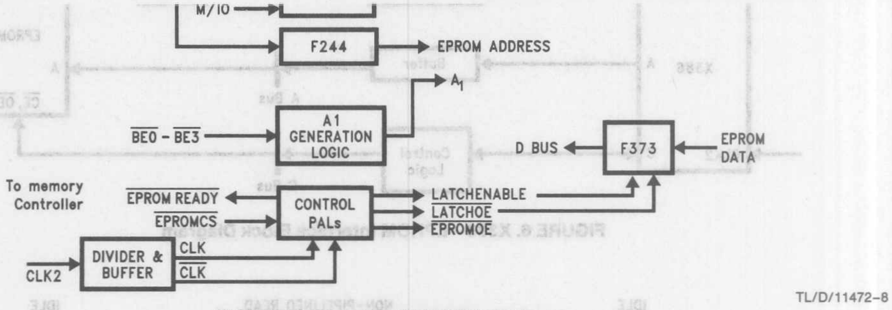

FIGURE 8. Complete EPROM Interface

The F244 is used to buffer the processor address to be applied to the 27C512 address bus. PAL16L8-A (25 ns delay) decodes the address and M/$\overline{IO}$ signal to generate $\overline{EPROMCS}$ signal. The LATCHENABLE signal latches the EPROM data in F373, so that X386 data hold requirements can be met. The output enable signals applied to the EPROM and the F373 are used to enable it and disable the data bus. These need to be synchronized for the proper timing relationship. The double frequency CLK2 signal is used to derive two half-frequency signals, CLK and $\overline{CLK}$, which drive the EPROM control PALs. $\overline{EPROMREADY}$ signal indicates the end of EPROM read cycle. The memory controller uses this signal to issue $\overline{READY}$ to the processor.

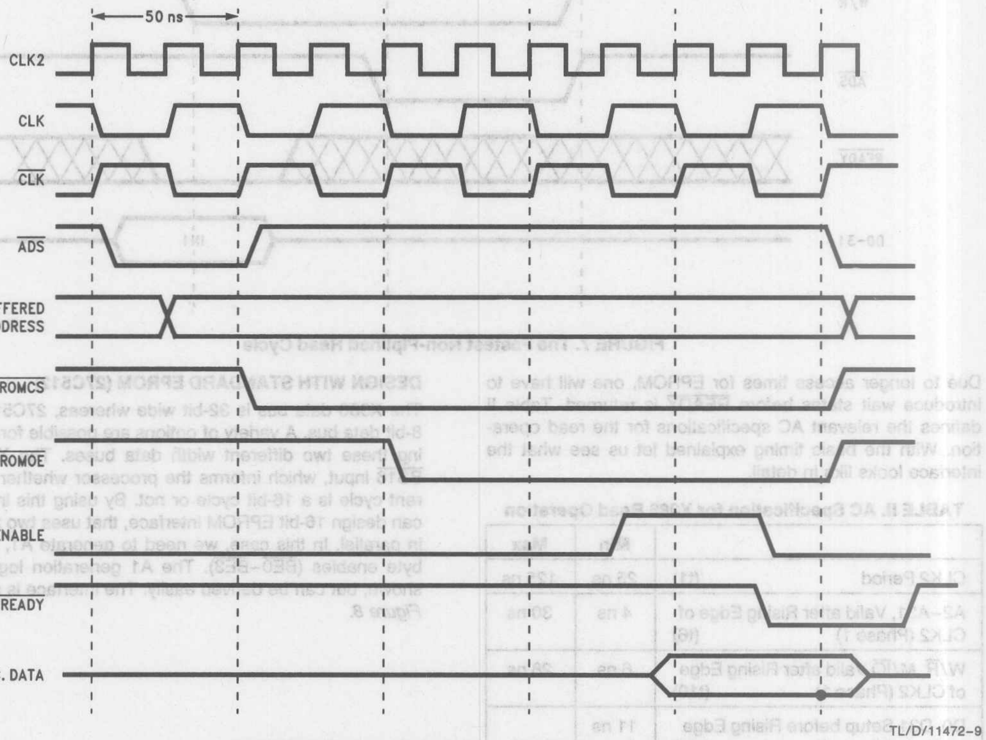

FIGURE 9. Timing Diagram for 27C512 Read Cycle

Figure 9 shows the timing diagram for the 27C512 Read Cycle. For a 4-cycle EPROM access, 120 ns 27C512 are required as shown in Equation 3 below.

About 4 ns margin takes care of delays due to trace length, clock skews and loading effects. $\overline{\text{EPROMREADY}}$ is generated in the fifth cycle, so that, a new operation can begin after a total of **five cycles.**

DESIGN WITH POP (27P512)—120 ns

The interface to the POP looks very much as the standard EPROM interface. The address decoder, A1 generation logic and the address buffer are unchanged. Because the Immediate Access EPROM has a minimum of 7 ns data hold time, the F373 latch is no longer required. A buffer is introduced in place of the F373, assuming a large load on the data bus. $\overline{\text{EPROMREADY}}$ can be generated one clock cycle earlier as compared to the standard EPROM design cycle. The complete timing diagram is shown in *Figure 10.*

The access to the EPROM still takes four cycles, for 120 ns 27P512. Due to data hold feature of the 27P512 $\overline{\text{EPROM READY}}$ is generated one clock cycle early and a new operation can begin immediately after a total of **four cycle.** 7 ns minimum data hold time of the 27P512 satisfies the data hold time requirement of 6 ns in the X386 read operation. Thus, due to hold time feature of Immediate Access EPROM, faster EPROM read cycles are possible as compared to the standard EPROM. To achieve the same performance as 120 ns POP, 70 ns standard EPROM are required as shown in Equation 4.

For n clock cycle access the EPROM timing equation is,

t_6	$+ \text{Max}\{t_{PAL}, t_{PD}(\text{buffer})\}$	$+ t_{ACC}$	$+ t_{PD}$ (latch)
CLK2 to address valid	Max {PAL delay, buffer delay}	EPROM access time	buffer delay
$+ t_{PD}$ (transceiver)	$+ t_{21}$	$\leq (n)\,(2)\,t_{CLK2}$	
transceiver delay	data setup time to X386		

Substituting the values from the datasheet,

For a 4-cycle access

$$30 + 25 + t_{ACC} + 5 + 5 + 11 \leq 4 * (50) \qquad (3)$$

$$t_{ACC} \leq 124 \text{ ns}$$

For a 3-cycle access

$$30 + 25 + t_{ACC} + 5 + 5 + 11 \leq 3 * (50) \qquad (4)$$

$$t_{ACC} \leq 74 \text{ ns}$$

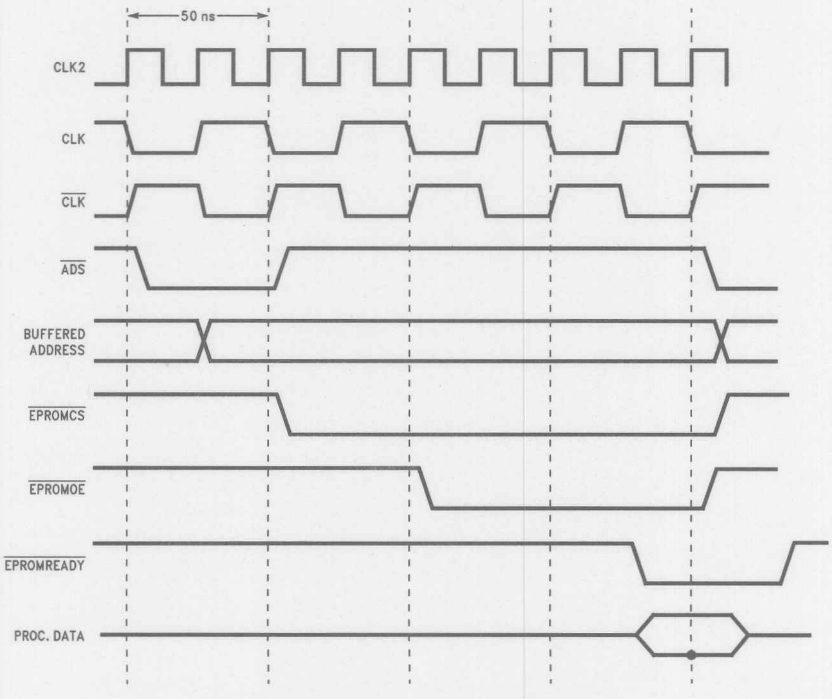

FIGURE 10. Timing Diagram for 27P512 Read Cycle

In the Immediate Access EPROM design the data buffer at the output of 27P512 can be omitted depending on the application. Due to the fast disable time of the 27P512 (25 ns as opposed to 50 ns in the 27C512), if the loading on the data bus is light the 27P512 outputs can directly drive the data bus. In such a case, even simpler and compact design is achieved.

CONCLUSION

National's POP family of devices are ideal for the popular processor based design (e.g. '030 and X386), which demand performance from the non-volatile storage devices without paying significant cost penalty. For the same access time the number of wait states is reduced leading to a maximum of 20% performance improvement. Standard faster access EPROMs can be designed in, but with extra components and added complexity of design. Depending on the loading conditions the external buffer at the POP output can be omitted without causing data bus contention. The reduced component count leads to compact PCB real estate which reduces design and manufacturing costs.

The performance improvement is achieved though two features offered by the POP devices. The data hold feature guarantees data at the EPROM output pins at the end of access cycle. The fast data float feature assures that EPROM will release the data bus much faster compared to the standard EPROMs. As shown in this application note EPROM memory subsystem can be easily designed with POP with improved performace and reduced component count.

Benefits of Low Voltage EPROMs in Cellular Applications

National Semiconductor
Application Note 826
Madhusudhan Rayabhari

INTRODUCTION

Cellular phones are rapidly moving towards the "Portable Phone" concept from their origin as vehicular mobile telephone units. The Portable phone provides the user with utmost mobility. Reduced equipment size and power consumption form the key to the design of such portable phones. The introduction of Low Voltage EPROMs by National Semiconductor addresses these requirements. The power drain on the battery in the standby and talk modes determines the duration for which the battery charge lasts. This application note discusses the critical nature of this factor and shows how the new Low Voltage EPROMs from National go a long way in satisfying the needs of cellular designers. Batteries last up to 25% longer on a single charge in designs which employ the new Low Voltage EPROMs from National.

CELLULAR CONCEPTS

The circuitry of a cellular phone consists of two sections—the Radio Section and the Digital Section. The radio section deals with the transmission and reception of voice and signaling information at the appropriate radio frequencies. The digital section is concerned with the generation and interpretation of signaling information, display functions and with manipulation of voice and users inputs. *Figure 1* gives the block diagram of a typical cellular telephone. The Radio Section *(Figure 1a)* consists of the modulator, demodulator, duplexer and the power amplifier for transmission of signals at the specified level. The frequency synthesizer is controlled by the digital section and is capable of generating the required frequencies for transmission and reception on any of the channels allocated for cellular telephony usage.

The control and digital section *(Figure 1b)* consists of a microcontroller, EPROM, RAM, E²PROM, encoder and decoder for the setup channel (to be explained later) and an analog section consisting of tone-generators, handset interfaces, etc. The density of the EPROM used in typical cellular telephones is 512 kbit–1 Mbit. The entire microcontroller code is stored in this EPROM. The E²PROM is used for storing frequently dialed numbers, information on radio frequencies and certain numbers related to system identification.

SIGNALING AND CALL PROCESSING

Two types of radio channels are used in Cellular Telephony—Setup Channels and Voice Channels. Setup channels transmit and receive messages consisting of binary data only. They are used only for initiating and setting up voice calls. These channels are for common use of cellular phones which are in the process of setting up a call. Voice channels are used for voice communication and for short bursts of data required for control purposes during the call or at call termination. These bursts are interleaved with voice.

When first powered up, the cellular phone enters what is called the idle state. In this state, it scans the entire group of setup frequencies to determine the strongest carrier signal and begins to monitor that channel for incoming calls. Usually, the strongest signal belongs to the base station of the cell in which the cellular phone is operating. At periodic intervals, the setup channels are scanned for the strongest signal to determine whether the movement of the cellular phone has made the use of the setup channel of another cell more appropriate.

The important point to note here is that for such an activity (i.e., monitoring the setup channel for incoming calls) the receive portion of the radio circuitry and the digital control section which includes the microcontroller, RAM, EPROM, etc., are constantly powered on. What this actually means is that the logic circuitry is always on, whether or not a voice call is in progress, and thus represents a constant drain on the battery. It is important, therefore, that this circuitry draw minimal current in view of extending battery life. The power drain of a cellular phone is a critical factor in the selection as all of them radiate the same amount of power which is determined by the relevant standard (i.e., EIA IS19B). Typical figures on power consumption for presently available cellular phones are 55 mA–60 mA in standby (Idle) mode and 550 mA–575 mA in the talk mode. The calculations for power saving that follow are based on these representative figures and a design based on a standard 5V microcontroller operating at 2 MHz–3 MHz and using a battery of 700 mAH rating.

A typical cellular phone uses an E²PROM for storing frequently dialed numbers and electronic identification information. A separate analog IC featuring 4 analog switches (typically a CD4066) is used for switching voice, touch-tone and binary signaling on to the radio channel. An important design feature in this application note is the use of the versatile NM95C12. This device integrates, on a space saving 14-pin SO/DIP, a 1024-bit E²PROM and 4 programmable switches which can be used in a variety of modes. In this application, the switches are used in the analog mode where they are used for connecting the touch-tone, binary and voice signals onto the transmit channel. This device replaces the use of separate ICs for the E²PROM and analog switches. On a vehicle mounted unit, they can also be used to select between the handset and speakerphone modes. It has a serial interface to the microcontroller—MICROWIRE/PLUS™. This leads to lesser interconnect wiring on the board, giving further savings in board space.

POWER SAVING

Power consumption is reduced in two ways—by operating at a lower voltage or by using devices that consume lesser power. The NM27LV010 from National fits both categories. It is capable of operating at 3V and it consumes vastly reduced power. While standard EPROMs consume up to 100 mW (20 mA typical @ 5V and 3 MHz) National's NM27LV010 consumes about 24 mW (6 mA–8 mA typical @ 3V), thus reducing power drawn by the EPROM by 75%. Substituting these values in typical power consumption figures of a cellular phone (Box-1) shows that **the standby time of the cellular phone is extended from a typical 12 hour value to up to 15 hours**. The cellular phone consumes a very large amount of current in talk mode. Using National's Low Voltage EPROMs would extend the talk time

adequate for the cellular application. Another significant point of interest to the designer is the operating frequency. The power consumption varies widely with the operating frequency. *Figure 2* depicts the relationship between the operating frequency and the typical active current for the NM27LV010. The designer may consider operating the system at an appropriately reduced frequency to achieve further savings in power.

SUMMARY

Using the low voltage EPROMs from National in cellular applications leads to savings in power and space. An overall the components for the digital section available from National. National has also announced an entire family of Low Voltage Logic Devices for designing systems for 3V operation. A large number of National's components come with a highly optimized serial interface—MICROWIRE/PLUS. This interface is used for device control and reduces the interconnect wiring associated with usual parallel buses leading to savings in board space. National also produces most of the analog and digital components of the cellular radio systems, giving a single source solution to the Cellular Designer's needs.

TABLE I

Functional Block	Component	Function	Features
EPROM	NM27LV512	Code Storage	Low Voltage Operation, Low Power Consumption
E^2PROM	NM95C12	Non Volatile Storage for Number, Frequencies, etc.	MICROWIRE/PLUS operation, 4 Analog switches for summing signals, selection between handset and speakerphone operations on vehicle mounted mobile phones. Replaces a separate IC for analog switching.
Display	MM58201	LCD Driver	Low Power, Serial Interface

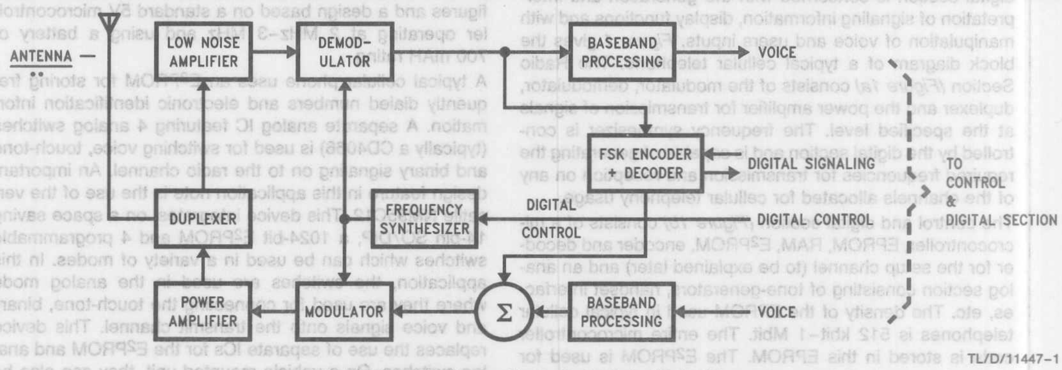

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FIGURE 1a. Radio Section of a Cellular Telephone

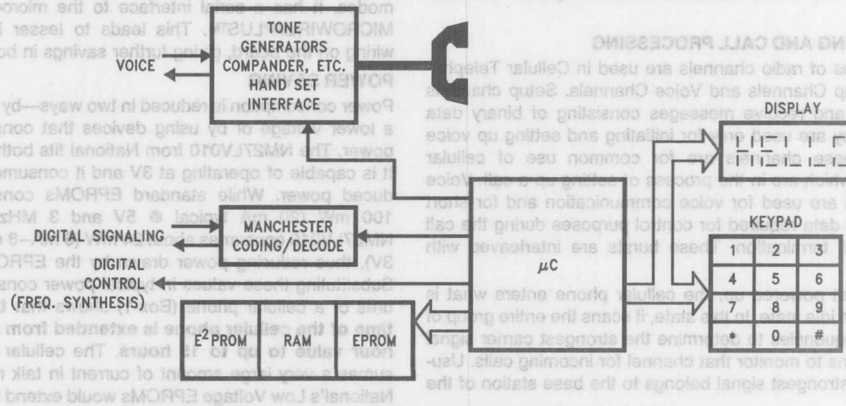

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FIGURE 1b. Control and Digital Section of a Cellular Telephone

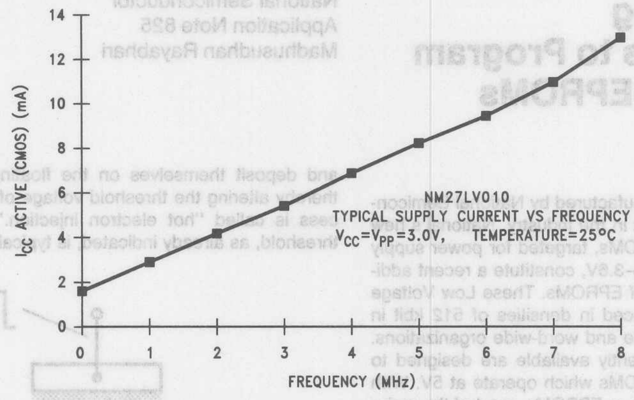

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FIGURE 2. Plot of Power Supply vs Operating Frequency

Standard EPROM Solution	
Typical Cellular Phone Current Drain (in Standby Mode)	55 mA
Typical EPROM Current @ 3 MHz and 5V	20 mA
LV EPROM Solution	
Typical Current (LV EPROM)	8 mA
Logic ICs (for Interface)	4 mA
Total Current → 12 mA @ 3V	
Total Power → 12 * 3 = 36 mW	
Using a DC-DC Converter which is 80% efficient	
Current @ 5V	= 36/(0.8 * 5) = 9 mA
Current Savings → 20 mA − 9 mA = 11 mA	
Current drain using LV EPROM → 55 mA − 11 mA = 44 mA	
Extension of Standby Time (Using a 700 mAH Battery)	
(700/44) − (700/55) = 3.18 Hours	
Extension of Standby Time	
(Percentage) = 3/12 → 25%	

Note: All above calculations assume a 3 MHz Operating Frequency

BOX-1. Power Savings Calculation

Using Existing Programmers to Program Low Voltage EPROMs

National Semiconductor
Application Note 825
Madhusudhan Rayabhari

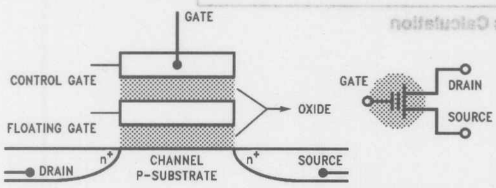
INTRODUCTION

The range of EPROMs manufactured by National Semiconductor is one of the largest in the industry. National's new family of Low Voltage EPROMs, targeted for power supply voltages in the range of 3V–3.6V, constitute a recent addition to the growing family of EPROMs. These Low Voltage EPROMs are being introduced in densities of 512 kbit in byte-wide and 1 Mbit in byte and word-wide organizations. EPROM programmers currently available are designed to program the standard EPROMs which operate at 5V. With the introduction of Low Voltage EPROMs, most of the major manufacturers of EPROM programmers have begun the process of upgrading their hardware and software to accommodate the Low Voltage EPROMs. This issue of programmer updates is common to all manufacturers of Low Voltage EPROMs across the industry.

National's Low Voltage EPROMs use exactly the same programming algorithm as the standard 5V parts and are fully capable of programming on existing programmers, which program the standard 5V EPROMs, with no adverse effects whatsoever on their reliability and endurance. This note seeks to alleviate any concern the EPROM user may have on programming the Low Voltage EPROMs on programmers which program 5V parts and shows that these programmers are guaranteed to correctly program National's Low Voltage EPROMs. Beginning with a brief and simplified overview of the internal structure of EPROM, the note describes the process of programming and programming verify and shows that National's Low Voltage EPROMs program correctly on existing programmers.

EPROM OVERVIEW

The basic storage element in the EPROM is a MOS transistor which has an additional "floating" gate built in between the control gate and the channel. This element is usually referred to as the cell *(Figure 1)*.



TL/D/11434-1

FIGURE 1. EPROM Cell and Its Schematic

An important parameter of the cell is its threshold voltage—the control gate voltage at which the cell begins to conduct. The threshold voltage of an erased cell is well below the V_{CC} value. When the control gate is driven to V_{CC}, the erased cell conducts and this is a logic "1". Programming elevates the threshold of the cell by 5V–10V. This results in the programmed cell not conducting under normal operating voltages, and is permanently off. This is a logic "0". A fully erased EPROM reads all "1"s. Programming consists of applying elevated voltages to the gate and the drain of the cell. This causes electrons to penetrate the intervening oxide and deposit themselves on the floating gate *(Figure 2)*, thereby altering the threshold voltage of the cell. This process is called "hot electron injection." The shift in the threshold, as already indicated, is typically 5V–10V.

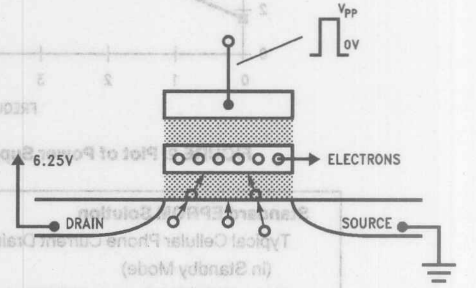


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FIGURE 2. Programming an EPROM Cell

Erasure consists of shining ultra violet light on the die through the quartz window provided. This light provides the electrons trapped on the gate with sufficient energy to return to the channel and on to the control gate, and thereby returns the cell to the unprogrammed state. This is illustrated in *Figure 3*.

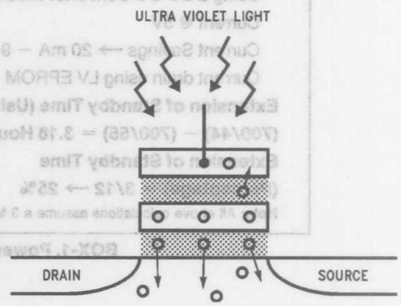

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FIGURE 3. UV Light Erasure of Cell

The number of electrons that get liberated depends on the intensity of the light and the duration of exposure. As already noted, then new Low Voltage EPROMs from National use exactly the same programming algorithm as the standard 5V parts.

PROGRAMMING

The programming algorithm specified by most manufacturers consists of programming data into the EPROM at the specified elevated voltage into all the locations that need to be programmed followed by a verify under normal read conditions. Programming the desired cell requires that an elevated voltage be applied to the bit line. The internal logic applies a high voltage pulse of 13V to the control gate in response to the external PGM pulse. This is illustrated in *Figure 4*.

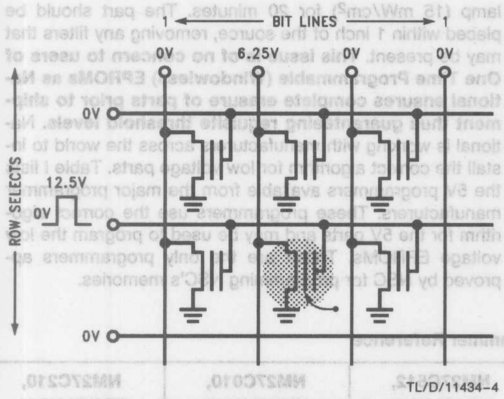

FIGURE 4. Programming a Cell in the Array

The verify is a "read" on the location to check if the cell has the right programmed state and margin. Internally a check is made to see if the cell conducts current of a magnitude greater than half the current of an unprogrammed reference cell. This reference value is called the sense threshold. *Figure 5* depicts the relationship between the applied gate voltage and the current the cell conducts. The amount of current a cell conducts depends on the threshold voltage of the cell and the magnitude of the voltages applied on the control gate and the drain.

PROGRAMMING VERIFY

An accurate verify must read the EPROMs at both V_{CC}(min) and V_{CC}(max). For the Low Voltage EPROMs the values are 3.0V and 3.6V respectively. Most of the current programmers perform verify at the voltage levels specified for a standard 5V part. As a result of incomplete erasure, the lowered cell threshold voltage which might be adequate for 5V levels may not be so for low voltage operation. What this actually means is that the higher level of voltages (5V as against 3.0V–3.6V) may cause the cell to conduct current in excess of the sense threshold. When the voltages are lowered to the correct values, the cell current might not exceed the sense threshold. This is illustrated in *Figure 5.* When the partially erased cell is verified at 5V levels, the current magnitude exceeds the internal sense threshold. However, it would not qualify when verified at voltage levels 3.0V–3.6V. Thus, a part which verifies correctly at 5V might not when operated at 3V. The inability to verify at V_{CC} levels 3.0V–3.6V is a limitation of current programmers and most programmer vendors are in the process of coming up with updates on their products which program and verify the low voltage parts correctly.

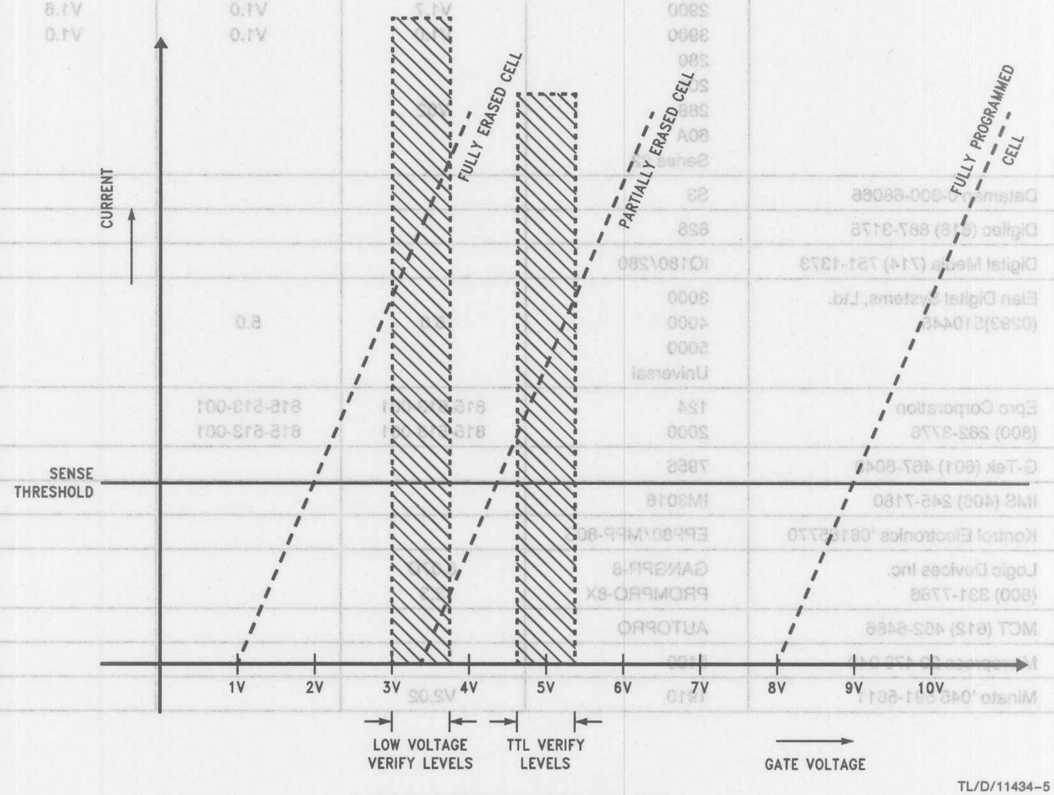

FIGURE 5. EPROM Cell Characteristics

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PROGRAMMING LOW VOLTAGE EPROMs

National's Low Voltage EPROMs are also capable of functioning at the standard supply voltage (V_{CC}) of 5V. Furthermore, National's proprietary manufacturing process using the split-gate SVG technology guarantees that the threshold of factory shipped parts are well below the 3V level and hence may be directly programmed on existing programmers (which verify at 5V levels). The parts thus programmed are guaranteed to work at the 3V levels. National guarantees that the Low Voltage parts erased with an integrated UV light dosage of 15 W-sec/cm^2 will program (with verify at 5V levels) and work reliably at 3V levels. This dosage of UV light is obtained by exposing the part to a typical UV lamp (15 mW/cm^2) for 20 minutes. The part should be placed within 1 inch of the source, removing any filters that may be present. **This issue is of no concern to users of One Time Programmable (Windowless) EPROMs as National ensures complete erasure of parts prior to shipment thus guaranteeing requisite threshold levels.** National is working with manufacturers across the world to install the correct algorithm for low voltage parts. Table I lists the 5V programmers available from the major programmer manufacturers. These programmers use the correct algorithm for the 5V parts and may be used to program the low voltage EPROMs. These are the only programmers approved by NSC for programming NSC's memories.

TABLE I. EPROM Programmer Reference

Manufacturer	Programmer Model	NM27C512, NM27LV512	NM27C010, NM27LV010	NM27C210, NM27LV210
Data I/O (800) 255-2102	UniPak2	V13		
	UniPak 2B	V13	V15	
	212 Mod EPROM	V1.1	V1.1	
	S1000	V11	V11	V20
	Unisite 40	V2.2		
	120/121A	V14.1		
	GangPak			
	2900	V1.7	V1.0	V1.6
	3900	V1.0	V1.0	V1.0
	280			
	201			
	288	V02		
	60A			
	Series 22			
Dataman 0-300-68066	S3			
Digilec (818) 887-3175	828			
Digital Media (714) 751-1373	IQ180/280			
Elan Digital Systems, Ltd. (0293)510448	3000			
	4000	5.0	5.0	
	5000			
	Universal			
Epro Corporation (800) 262-3776	124	815-513-001	815-513-001	
	2000	815-513-001	815-513-001	
G-Tek (601) 467-8048	7956			
IMS (408) 245-7180	IM3016			
Kontrol Electronics '08165770	EPP80/MPP-80S			
Logic Devices Inc. (800) 331-7766	GANGPR-8	8.07D		
	PROMPRO-8X	3.3		
MCT (612) 462-6486	AUTOPRO			
Micropross 20 479 040	5100			
Minato '045 591-5611	1910	V2.02		

TABLE I. EPROM Programmer Reference (Continued)

Manufacturer	Programmer Model	NM27C512, NM27LV512	NM27C010, NM27LV010	NM27C210, NM27LV210
OAE (800) 828-0080	OMN164			
Southern Computer (404) 252-3340	512B			
Stack Ltd. 44-869-240404	C289			
Advantest	R4945 RA951 UP-UPROG	A02 D00	A02 D00	
HI-LO System	All-03	V3.0	V3.0	
BP Microsystems	ER-1140	V1.76	V1.76	
Stag Microsystems (408) 988-1118	39M101	4.0	4.0	
	40M100			
	40M101	7.0		
	40N101	3.0	3.0	
	41M100			
	41M101			
	42M100			
	42M101			
	ZM2000			
	ZM2500			
	ZM2800			
	ZM3000	5.0	5.0	
	PP40	04-01	04-01	

National's Low Current EPROMs

Designing line powered telephones for ISDN is now possible with the introduction of Low Current EPROMs by National Semiconductor. The stringent power budget of 380 mW imposed by the CCITT is now within the reach of the telecom designer by use of the Low Current EPROMs from the Power Miser family introduced by National Semiconductor. A large portion of the residential telecom lines do not require to carry data. Telephony is, and will continue to be the predominant residential telecommunication service. An ISDN terminal equipment with voice-only capability is sufficient to meet the telecom needs of such customers. Until now, design of line powered ISDN telephones presented a formidable task to the designer. This was due to the amount of power the phones were permitted to draw from the ISDN line. **The advent of Low Current EPROMs makes it possible now to design ISDN telephones which are wholly powered by the ISDN line.**

THE STANDARDS

The standards for ISDN are specified by the CCITT and adapted for American use by the American National Standards Institute (ANSI). The standard (T1.605-1991) specifies the power consumption of such equipment. Power consumed is defined in terms of Power Consumption Units (PCUs). Under normal operating conditions a PCU is equivalent to 100 mW (NPCU). Under power failure i.e., restricted conditions it equals 95 mW (RPCU). Fractional units are not permitted and are rounded off to the next integer value. Under restricted conditions only 4 RPCUs are permitted. Hence, the figure of 380 mW. A line powered ISDN telephone must, therefore, be able to provide the entire set of features while consuming only 380 mW of power.

THE DESIGN

Figure 1 gives the block diagram of a line powered ISDN telephone. The following paragraphs describe the key features and elements of the design. The basic functions that need to be incorporated in the design are

- Protocol Control for signaling on the "D" Channel
- Circuit Switched channel for Voice Calls
- Monitoring Functions to power down equipment when not in use
- Keypad and display for user interaction

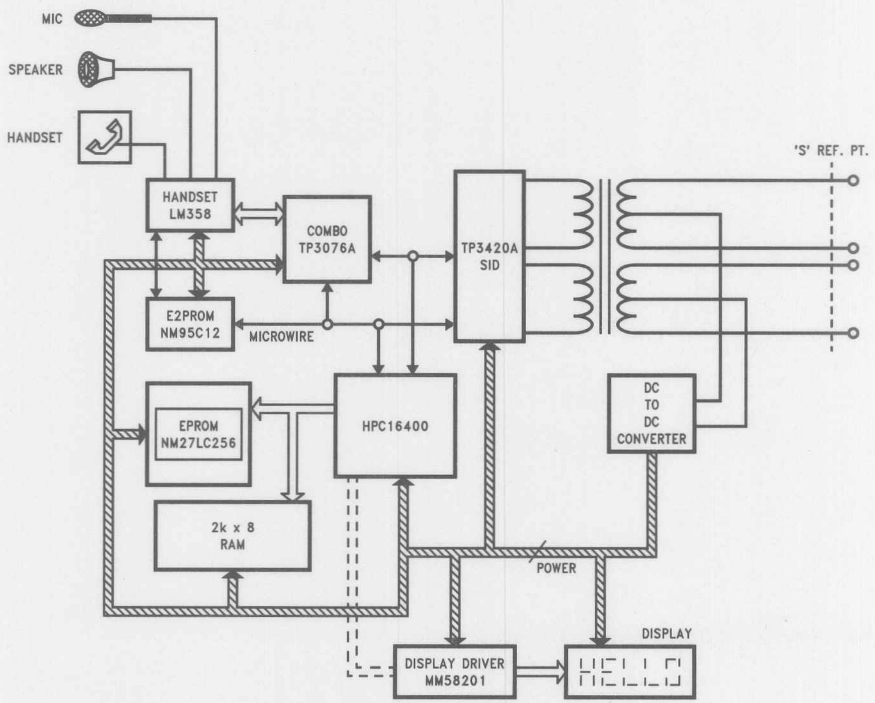

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FIGURE 1. Block Diagram of ISDN Phone

MEMORY

As always, the EPROM is one of the critical components in a microcontroller/microprocessor based design. Important parameters of this building block include density, access time and power consumption. For a design based on 2 MHz processor speed, an access time of 250 ns or better is adequate. A Memory Density of 256 Kbits is typically adequate for ISDN telephony phone applications. The use of the Low Current NM27LC256 from National reduces the EPROM power consumption by over 60%, making line powered ISDN phones possible. As against a power consumption of up to 100 mW in case of standard part the NM27LC256 consumes only 40 mW. This massive reduction of power makes it possible to design an ISDN phone using only the power delivered by the line while implementing a full set of features.

TABLE I

Functional Block	Component	Power
Microcontroller	HPC16400	10 mA
Line Interface (SID)	TP3420A	26 mA
Display Driver	MM58201	0.3 mA
Display	Any 7-Seg 24 Digit	0.5 mA
Codec/Combo	TP3076A	22 mA
Handset Interface	LM358	2 mA
Total Power ——		**60.8 mA**

TABLE II

Functional Block	Component	Power	Stdby Power
EPROM	27LC256	4.5 mA	100 μA
EEPROM	NM95C12	4 mA	800 μA
RAM	2k x 8	5 mA	50 μA
Total Power (Worst Case)		**5 mA**	**900 μA**

Table I lists the components which are constantly on when the phone is in use. These components include the Microcontroller, Line Interface, Display, Display Driver and the Codec. These components form the basic building blocks of the telephone. Table II lists the components in the Memory Section of the telephone. The RAM is required for storing the incoming and outgoing signaling information, which is actually in the form of data packets. For this application a RAM density of 2 Kbytes is adequate. The RAM is also used for the stack operations of the microcontroller. It is important to note that the operation of EPROM and RAM is mutually exclusive. When either of them is accessed, the other is in the standby mode. It is possible, via the microcontroller serial port, to put the codec in the standby mode. This feature is used when activating the E^2PROM to reduce the instantaneous power consumption. This causes no operational problems as typically E^2PROM accesses are made for abbreviated dialing facility, single key dialing, etc. All this occurs in mutual exclusion to voice communication (conversation).

The E^2PROM used in this application is the versatile NM95C12 from National. This device features a 1024-bit E^2PROM array, a set of 8 switches which can be programmed to operate in a variety of modes. In this application, the switches are used to direct analog voice signals at the codec either to the handset or to the speaker phone. This feature obviates the use of analog switches, leading to savings in space and power.

BOX 1

Total Power Available:	380 mW
Available Power with a DC-DC Converter of 88% Efficiency (used in this design):	$380 \times 0.88 = 334.4$ mW
This gives a current of 66.88 mA @ 5V	

Box 1 gives the power budget for the telephone system. A high efficiency DC-DC Converter (88% efficiency) was used in this application. It can be easily seen that the use of National's Low Current NM27LC256 makes it possible to meet the requirements imposed by the budget. This would not be the case had standard EPROMs been used. It is possible to design the entire software with the use of the 256 bytes of on-chip RAM on the microcontroller, eliminating the external RAM. Read/Write memory is required for storing incoming packets of information, formation of outgoing packets and stack for microcontroller operation. The packets are typically less than 16 bytes in size as only supervisory and un-numbered frames of LAPD are involved in signaling (no user information). Memory of 128 bytes or greater can be made available for the stack. This would permit the designer to use a standard DC-DC Converter with efficiencies in the range of 80%–85%.

MICROCONTROLLER AND LINE INTERFACES

An ideal choice for the microcontroller is the HPC16400 from National. This device incorporates a 16-bit core, a selectable 8/16-bit external bus interface, 256 bytes of RAM and most importantly a Protocol Controller for the "D" channel. A key design issue in this case is the power consumption. The HPC16400 consumes a maximum of 10 mA at 5V when operating at 2 MHz—a speed adequate for telephone applications. The National TP3420A SID provides the entire physical interface and the physical layer protocol management for the "S" Reference Point—the interface definition for attachment of subscriber equipment to the ISDN line. The TP3076A from National is an integrated PCM codec and filter designed specifically for ISDN applications. This gives A/μ law selectability and programmable gain. The

LM358 Operational Amplifier from National operates from a single 5V supply and consumes only a worst case maximum current of 2 mA. The LM358 features dual Operational Amplifiers. One channel may be used for the Handset microphone interface and the other for the Speakerphone microphone.

National also produces a variety of display drivers for LCD applications. Of particular interest in this application is the MM58201 LCD display driver which drives up to 192 segments. It draws minimal power (0.3 mA) and is well suited for the ISDN application where different messages (alphanumeric) are displayed for user interaction (Calling Party Number Indication, Reverse Charging request Indication, etc.). It interfaces via a serial port to the Microcontroller.

SUMMARY

The introduction of Low Current EPROMs by National makes it possible now to design ISDN telephones which are wholly powered by the line. The entire set of components required to build an ISDN phone are available from National thus giving a single-point solution to the ISDN designer.

Using National's NMC87C257 256K EPROM with On-Chip Latches

National Semiconductor
Application Note 731
Sean Pitonak

INTRODUCTION

The standard EPROM available from most manufacturers limits the on-chip circuitry to just the minimum needed to operate the EPROM and the minimum of user interface handles. Users of standard EPROMs are forced to include latches in their design to interface with most microcontrollers and microprocessors.

Probably one of the most desirable user-interface features is the ability to directly interface the EPROM to a host device that has a multiplexed address and data port. This type of interface is present on many microcontrollers and microprocessors such as the HPC, 80C51 and many of the Intel and Motorola microcontrollers. National is now manufacturing an EPROM that can directly interface with a host device—the NMC87C257.

NATIONAL'S NMC87C257 SOLUTION

The NMC87C257 is pin-compatible with the standard 27C256 (1 Megabit EPROM, organized as 128K x 8 bits), shown in *Figure 1*. In fact, the NMC87C257 can be directly substituted into the many existing 27C256 sockets when used in the unlatched mode. The internal latches are transparent and the Address Latch Enable (ALE) is on a shared pin with V_{PP}. By tying V_{PP} to V_{CC}, the NMC87C257 behaves exactly like the 27C256. The NMC87C257 is available in both quartz-windowed Ceramic DIP and Plastic LCC packages as is the 27C256.

National's latched EPROM is useful because the same ALE used for the 74F373 latch can be tied to the ALE of the NMC87C257, eliminating the need for the 74F373 latch. As shown in *Figure 2*, it is as simple as removing the two octal latches and routing the appropriate bus and control line to the EPROM.

SUMMARY

The NMC87C257 allows the user the combination of familiar functionality, pinout and programmability (due to its compatibility with existing 27C256 EPROMs) and the advantages of saved board space, cost of the octal latches and their insertion and system power consumption. The NMC87C257 gives the system designer the needed flexibility of interfacing directly with microcontrollers and microprocessors that have multiplexed address and data ports.

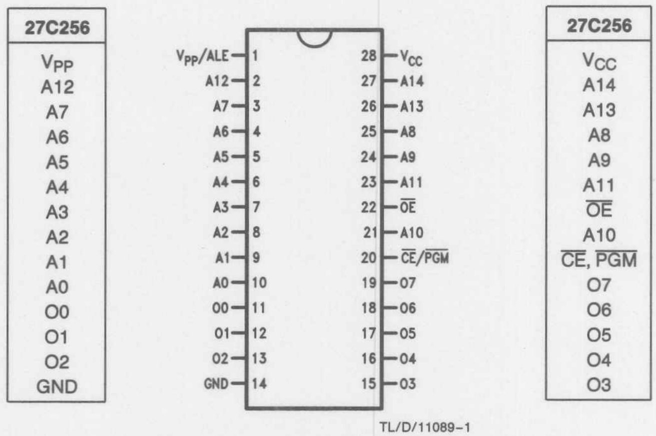

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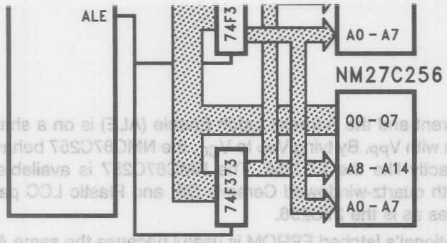
FIGURE 1. Socket Compatible 27C256 EPROM Pin Configuration is Shown in the Block Adjacent to the NMC87C257 Pins.



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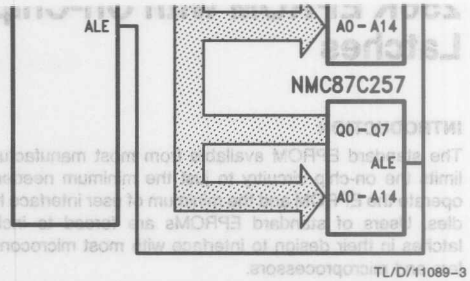

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FIGURE 2. A common HPC Microcontroller application using two NM27C256 EPROMs and two 74F373 external latches (left) and the same application using only two NMC87C257 EPROMs with on-chip latches (right).

Stand Alone Control of MICROWIRE™ Peripherals Using the NMC87C257

National Semiconductor
Application Note 791
Charlie Mitchell

INTENT

This note describes the implementation and use of a standard memory element in the realization of state machine control for the purpose of generating serial data. The applications shown here employ serial data streams to control and program peripheral devices which would otherwise require CPU support for use.

The benefit to the user of the demonstrated techniques is the low cost, low effort, implementation of tasks normally allocated to more sophisticated and more engineering intensive methods. These solutions expand the range of systems and applications in which a variety of National Semiconductor's MICROWIRE devices may be used.

MICROWIRE

The MICROWIRE standard is an interface technique first developed at National in the 1970's in an effort to reduce the component pin count (and hence package size and cost) required for the interfacing of microcontrollers to peripheral components. Over the ensuing years a wide variety of devices employing this interface technique have been introduced to the market. They include display drivers, analog to digital converters, phase lock loop frequency synthesizers, memories and complex analog devices. A full list of all but the most recent devices using the MICROWIRE interface can be found in the *Master Selection Guide*.

A MICROWIRE connection is a straight forward serial hookup consisting of data and clock. Generally, input and output data are presented on separate lines. The clock to data relationship resembles that of a TTL or CMOS 7400 series shift register with the positive edge of the clock performing the active transfer of data into and out of the device. Care must be taken to examine the data sheet for a device under consideration as there may be deviations from this general description. A more complete description of this interface method is available in National Semiconductor Application Note 452 by Abdul Aleaf.

STATE SEQUENCERS

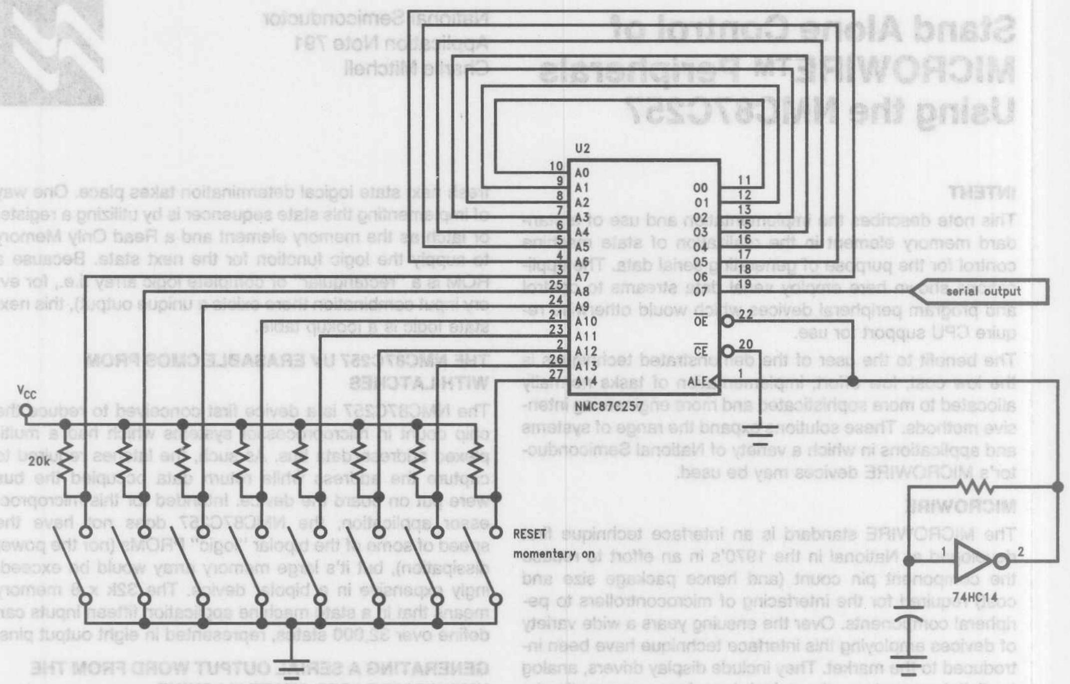
State machines or sequencers in their simplest form consist of a current state memory element and a next state determination network. Upon a clock edge the next state information is converted and held as a new current state while a fresh next state logical determination takes place. One way of implementing this state sequencer is by utilizing a register or latch as the memory element and a Read Only Memory to supply the logic function for the next state. Because a ROM is a "rectangular" or complete logic array (i.e., for every input combination there exists a unique output), this next state logic is a lookup table.

THE NMC87C257 UV ERASABLE CMOS PROM WITH LATCHES

The NMC87C257 is a device first conceived to reduce the chip count in microprocessor systems which had a multiplexed address/data bus. As such, the latches required to capture the address while return data occupied the bus were put on board the device. Intended for this microprocessor application, the NMC87C257 does not have the speed of some of the bipolar "logic" PROMs (nor the power dissipation), but it's large memory array would be exceedingly expensive in a bipolar device. The 32k x 8 memory means that in a state machine application fifteen inputs can define over 32,000 states, represented in eight output pins.

GENERATING A SERIAL OUTPUT WORD FROM THE NMC87C257 BASED STATE MACHINE

Figure 1 depicts a state machine capable of generating 128 different 128-bit serial data streams. DIP switches 0–7 select the specific data stream program. Seven bits of output data are fed back to inputs to define the next state in the serial data sequence. Bit 08 is the serial data output. A CMOS oscillator generates the clock. It is important to note that the clock drives both the ALE (Address Latch Enable) and $\overline{OE}$ (Output Enable) inputs. ALE is the signal which activates the "open" state of the input latch, as such, unlike an edge triggered register, the outputs follow the inputs until its (ALE's) fall. To avoid a high speed feedback phenomenon while the latches are open it is necessary to break the feedback loop and "freeze" the data at the desired output/input state. This is accomplished by disabling the TRI-STATE® outputs. As long as the outputs are loaded only by the high impedance inputs of the CMOS device, the next state information will be transferred into the latches. Resistive or bipolar logic loads should not be attached to lines operating in this manner.



Note: Refer to AN 140 for R & C values.

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FIGURE 1. State Machine for Serial Word Generation

TABLE I. PROM Addresses and Data

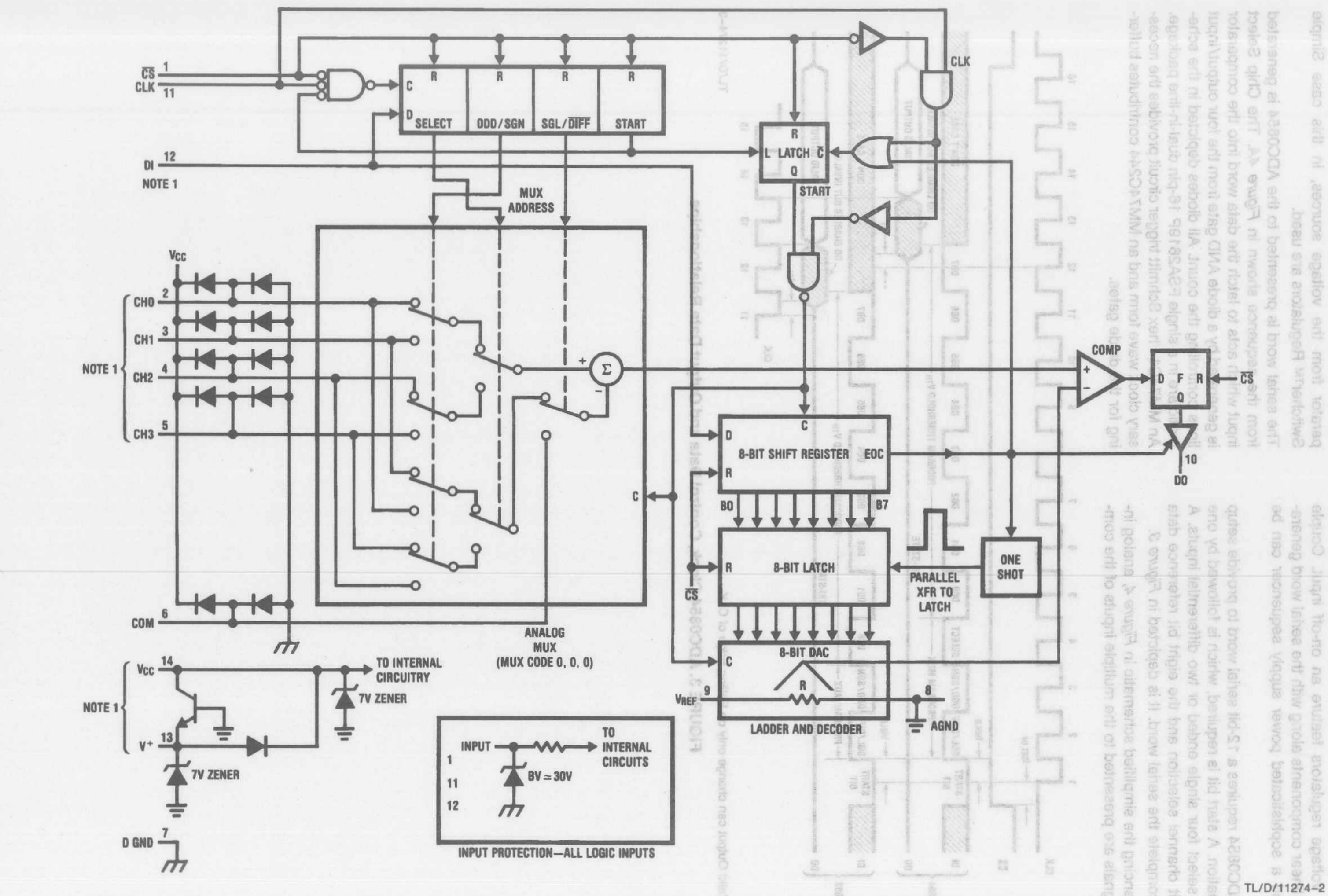
Address	Data (7 Bits)	Serial Output	Comments
nn 7F	00	0	Startup Address Generates 1st Word
nn 00	01	1	
nn 01	02	1	
nn 02	B4	0	
nn B4	03	1	
•			
•			
•			
nn 7E	7E	0	Loop to Self - Stop

Table I shows an example of the PROM code which generates the serial output. The address includes a leading byte "nn" which will determine which of the bit streams will be selected. Notice that the 7-bit data is in fact the next state information reflected in the next address.

APPLICATIONS FOR A SERIAL WORD GENERATOR USING THE NMC87C257

A Power Supply Sequencer

The ADC0854 is a comparator circuit with a MICROWIRE controlled four input multiplexer and a settable 8-bit reference divider which drives the second compare input. A block diagram is depicted in *Figure 2*.

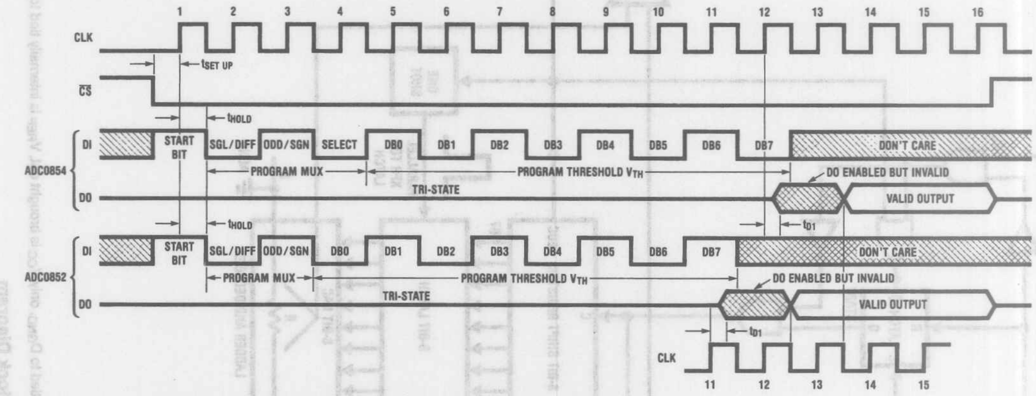


Note 1: For ADC0852; D1 is input directly to the D input of ODD/SIGN, select: is forced to a "1", A_{GND} and COM are internally tied to D_{GND}, only V_{CC} is brought out, V_{REF} is internally tied to V_{CC}, only CH2 and CH3 are brought out.

FIGURE 2. ADC0854 Detailed Block Diagram

The ADC0854 requires a 12-bit serial word to provide setup information. A start bit is required, which is followed by one bit to select four single ended or two differential inputs. A two bit channel selection and the eight bit reference data byte complete the serial word. It is depicted in *Figure 3*.

Referencing the simplified schematic in *Figure 4,* analog input signals are presented to the multiple inputs of the com- from the sequence shown in *Figure 4A.* The Chip Select input which acts to latch the data word into the comparator is generated by a diode AND gate from the four output/input lines controlling the count. All diodes depicted in the schematic are in a single FSA2619P 16-pin dual-in-line package. An MM74C14 hex Schmitt trigger circuit provides the necessary clock wave form and an MM74C244 contributes buffering for the diode gates.



Note: Valid Output can change only on Falling Edge of CLK.

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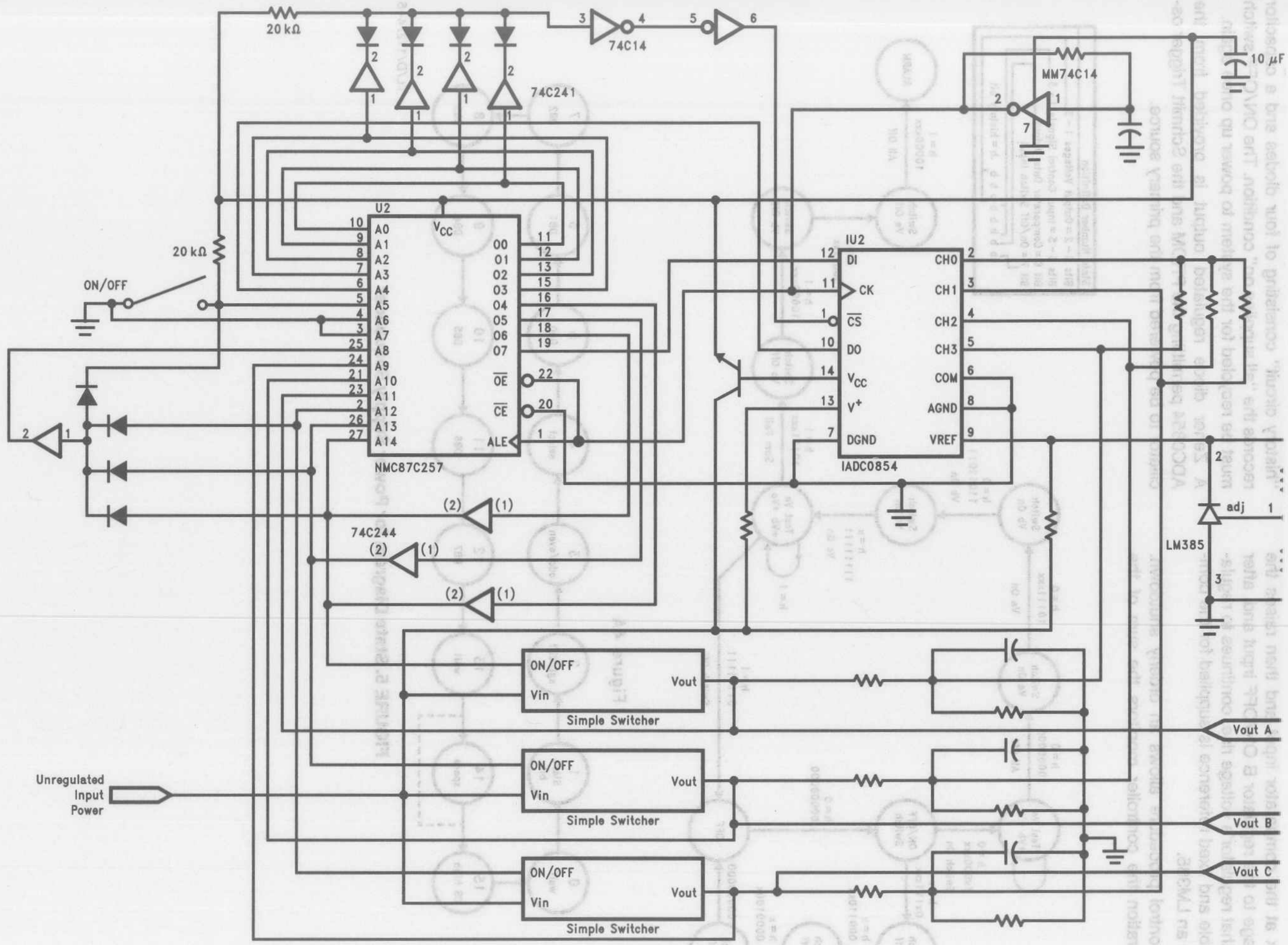
FIGURE 3. ADC0854 Clock, Control Data and Output Data Relationships



Note: Refer to AN 140 for R & C values.

Note: As resistive and capacitive values in this circuit will vary with application, consult the datasheets of the associated devices for component selection.

FIGURE 4. Partial Schematic of Power Supply Sequencer

Each regulator output is sequentially selected by the PROM generated MICROWIRE and tested for compliance to a voltage level also set via the MICROWIRE. When Voltage A reaches its terminal value, the sequencer delays for a defined period while voltage settles as determined here by the RC network at the comparator input and then raises the control voltage to the regulator B ON/OFF input and, after monitoring that regulator's voltage rise, continues to regulator C. A stable and fixed reference is supplied for the comparisons by an LM385.

A similar control procedure allows an orderly shutdown. During operation the controller monitors the sum of the three supply voltages. A drop from the proper sum will commence the controlled shutdown. These procedures are delineated by the state diagram in *Figure 5b.* In order to differentiate the state defining the condition of the voltages when powering up and the state produced when shutting down a "history circuit" consisting of four diodes and a capacitor records the "all supplies on" condition. The ON/OFF switch must be recycled for the system to power up once again.

A Zener diode regulated output is provided from the ADC0854 permitting the PROM and the Schmitt Trigger oscillator to be powered from the primary source.

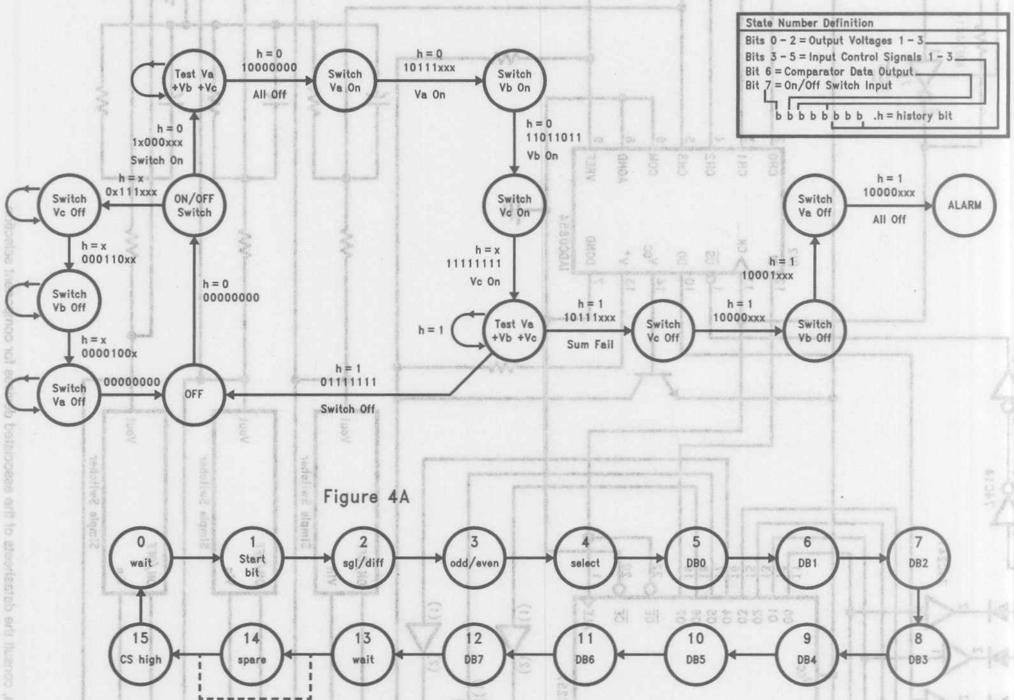


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FIGURE 5. State Diagram for Power Supply Sequencer

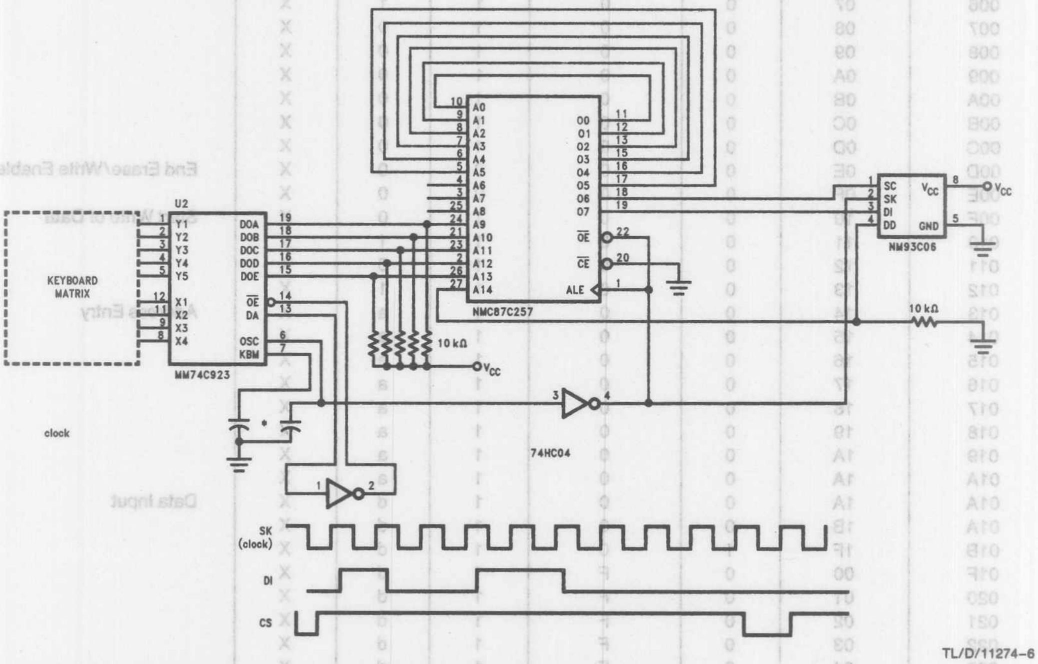
PRODUCTION LINE PROGRAMMING OF MICROWIRE EEPROMS

EEPROMs are frequently programmed prior to board insertion on the production line. This programming may reflect the revision level of the system software and the engineering change level of the printed circuit board.

In this case an NM93C06 256-bit device has been selected. In a production line situation it is desirable to write a segment of memory with the parameters described above.

In order to perform this task the memory must receive a series of MICROWIRE commands. Each of the commands is itself a state ordered sequence. The command sequences first enable the write capability, write 16 bits of information to the specified address and then turn off the write enable. Table II lists the inputs and outputs of the NMC87C257 for a sequence to write a sixteen bit word.

The logic diagram in *Figure 6* depicts a circuit which includes keypad entry capability such that an operator can select up to 20 different such commands.



*Consult MM74C923 datasheet for component values appropriate to the specific application.

FIGURE 6. Logic Diagram for EEPROM Programmer

TABLE II. PROM Listing for EEPROM Programming

Address (Hex)	00–04 (Hex)	EN	74HC173 (Hex)	CS	DI	DO	Comments
000	01	0	0	0	0	X	
001	02	0	0	1	0	X	Start Erase/Write Enable
002	03	0	0	1	1	X	Start Bit
003	04	0	0	1	0	X	Opcode
004	05	0	0	1	0	X	
005	06	0	0	1	1	X	
006	07	0	0	1	1	X	
007	08	0	0	1	0	X	
008	09	0	0	1	0	X	
009	0A	0	0	1	0	X	
00A	0B	0	0	1	0	X	
00B	0C	0	0	1	0	X	
00C	0D	0	0	1	0	X	
00D	0E	0	0	0	0	X	End Erase/Write Enable
00E	0F	0	0	0	0	X	
00F	10	0	0	1	0	X	Start Write of Data
010	11	0	0	1	1	X	
011	12	0	0	1	0	X	
012	13	0	0	1	1	X	
013	14	0	0	1	a	X	Address Entry
014	15	0	0	1	a	X	
015	16	0	0	1	a	X	
016	17	0	0	1	a	X	
017	18	0	0	1	a	X	
018	19	0	0	1	a	X	
019	1A	0	0	1	a	X	
01A	1A	0	0	1	a	X	
01A	1A	0	0	1	d	X	Data Input
01A	1B	0	0	1	d	X	
01B	1F	1	0	1	d	X	
01F	00	0	F	1	d	X	
020	01	0	F	1	d	X	
021	02	0	F	1	d	X	
022	03	0	F	1	d	X	
023	04	0	F	1	d	X	
024	05	0	F	1	d	X	
025	06	0	F	1	d	X	
026	07	0	F	1	d	X	
027	08	0	F	1	d	X	
028	09	0	F	1	d	X	
029	0A	0	F	1	d	X	
02A	0B	0	F	1	d	X	
02B	0C	0	F	1	d	0	End of Cycle
02C	0D	0	F	0	0	0	Wait for Data Out to
02D	0E	0	F	1	0	0	Go High
02E	0F	0	F	1	1	1	
02F	10	0	F	0	0	X	
030	11	0	F	1	0	X	Start of Erase/Write
031	12	0	F	1	1	X	Disable Cycle
032	13	0	F	1	0	X	
033	14	0	F	1	0	X	
034	15	0	F	1	0	X	
035	16	0	F	1	0	X	
036	17	0	F	1	0	X	
037	18	0	F	0	0	X	End of EWDS Command
038	19	0	F	0	0	X	

FILTER PARAMETER CONTROL

The LMC835 provides the complete resistor and switch set to implement a stereo 7 band equalizer or a mono 14 band system. While control of this device is usually provided from a microcontroller there are instances where that expense and effort are not necessary to achieve a complex filtering function.

To program the LMC835 one of fourteen frequency bands must be selected and the gain for that band entered. This band gain setting requires a minimum of 18 states. All fourteen bands must be preset and various control states must be implemented. Because of the large number of states involved in setting each of the fourteen bands a wider word is needed than can be implemented in a single PROM. There are several methods of dealing with this, however the most straight forward (for purposes of illustration) is to employ two PROMs.

The MICROWIRE interface used with the LMC835 differs slightly from those implemented above in that it uses a strobe to transfer data from the internal shift register to the latch for the addressed switch matrix. This permits the reprogramming of individual bands without the necessity of rewriting the entire machine state.

A complete logic diagram for the word generator is shown in *Figure 7*. The schematics for the implementation of the linear portions of the circuit can be obtained by referencing the LMC835 datasheet. A template for the PROM listing is also shown in *Figure 8*.

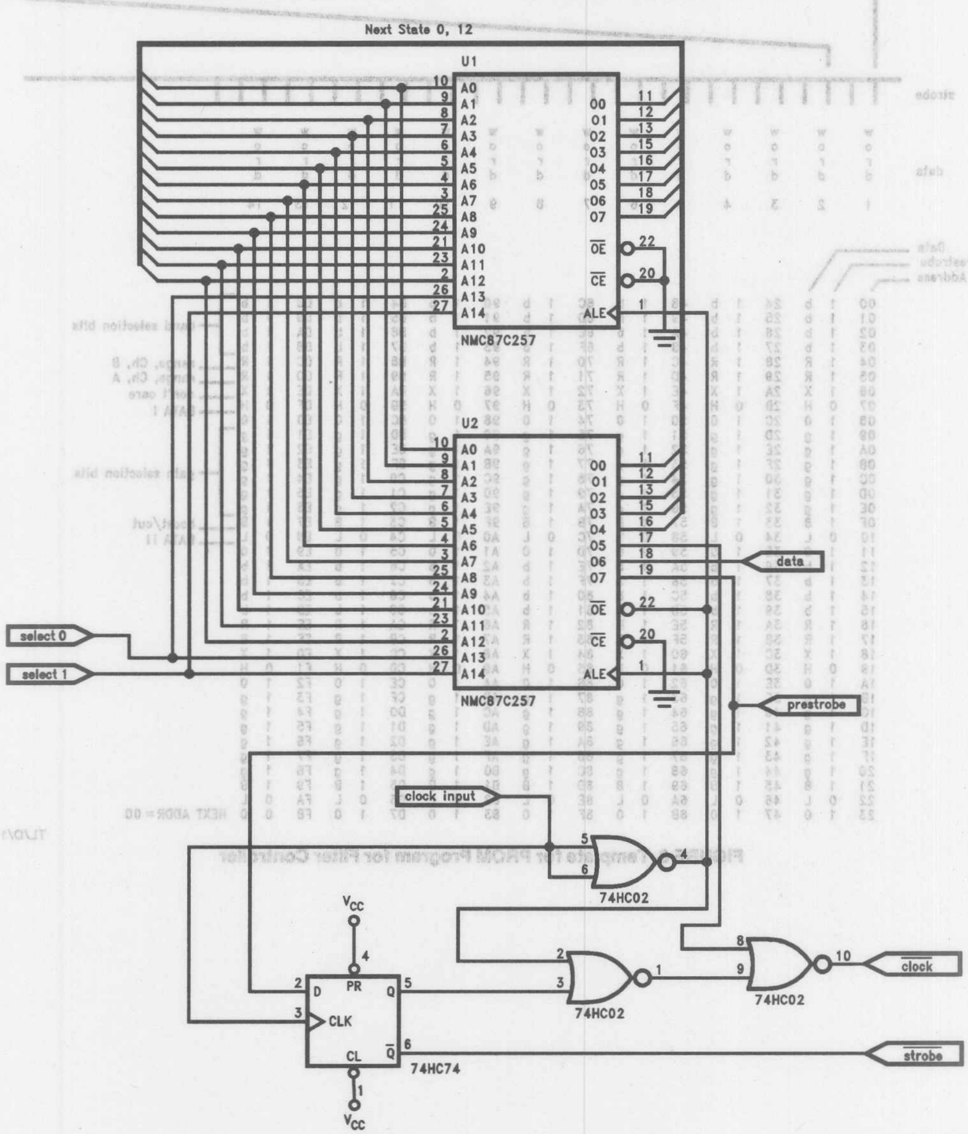


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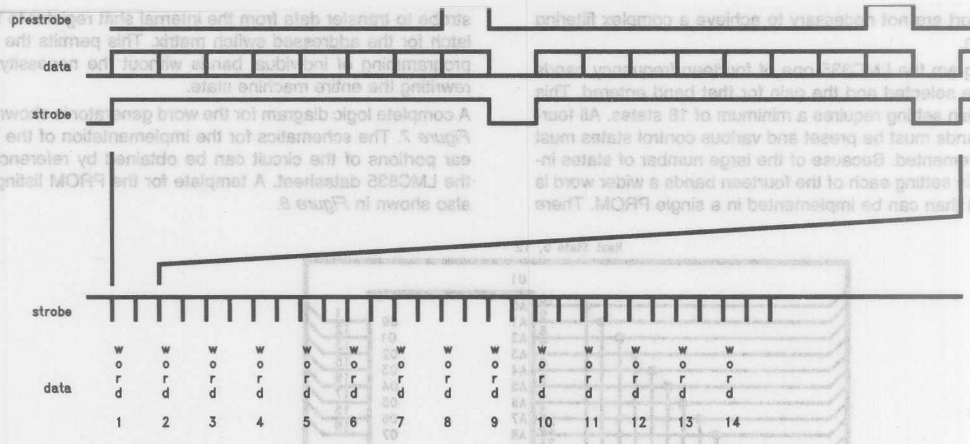
FIGURE 7. Logic Diagram for Equalizer Controller



Address	Prestrobe	Data	Address	Prestrobe	Data	Address	Prestrobe	Data	Address	Prestrobe	Data	Address	Prestrobe	Data	Address	Prestrobe	Data	Address	Prestrobe	Data	
00	1	b	24	1	b	48	1	b	6C	1	b	90	1	b	B4	1	b	D8	1	b	
01	1	b	25	1	b	49	1	b	6D	1	b	91	1	b	B5	1	b	D9	1	b	
02	1	b	26	1	b	4A	1	b	6E	1	b	92	1	b	B6	1	b	DA	1	b	band selection bits
03	1	b	27	1	b	4B	1	b	6F	1	b	93	1	b	B7	1	b	DB	1	b	
04	1	R	28	1	R	4C	1	R	70	1	R	94	1	R	B8	1	R	DC	1	R	range, Ch, B
05	1	R	29	1	R	4D	1	R	71	1	R	95	1	R	B9	1	R	DD	1	R	range, Ch, A
06	1	X	2A	1	X	4E	1	X	72	1	X	96	1	X	BA	1	X	DE	1	X	don't care
07	0	H	2B	0	H	4F	0	H	73	0	H	97	0	H	BB	0	H	DF	0	H	DATA I
08	1	0	2C	1	0	50	1	0	74	1	0	98	1	0	BC	1	0	E0	1	0	
09	1	g	2D	1	g	51	1	g	75	1	g	99	1	g	BD	1	g	E1	1	g	
0A	1	g	2E	1	g	52	1	g	76	1	g	9A	1	g	BE	1	g	E2	1	g	
0B	1	g	2F	1	g	53	1	g	77	1	g	9B	1	g	BF	1	g	E3	1	g	
0C	1	g	30	1	g	54	1	g	78	1	g	9C	1	g	C0	1	g	E4	1	g	gain selection bits
0D	1	g	31	1	g	55	1	g	79	1	g	9D	1	g	C1	1	g	E5	1	g	
0E	1	g	32	1	g	56	1	g	7A	1	g	9E	1	g	C2	1	g	E6	1	g	
0F	1	B	33	1	B	57	1	B	7B	1	B	9F	1	B	C3	1	B	E7	1	B	boost/cut
10	0	L	34	0	L	58	0	L	7C	0	L	A0	0	L	C4	0	L	E8	0	L	DATA II
11	1	0	35	1	0	59	1	0	7D	1	0	A1	1	0	C5	1	0	E9	1	0	
12	1	b	36	1	b	5A	1	b	7E	1	b	A2	1	b	C6	1	b	EA	1	b	
13	1	b	37	1	b	5B	1	b	7F	1	b	A3	1	b	C7	1	b	EB	1	b	
14	1	b	38	1	b	5C	1	b	80	1	b	A4	1	b	C8	1	b	EC	1	b	
15	1	b	39	1	b	5D	1	b	81	1	b	A5	1	b	C9	1	b	ED	1	b	
16	1	R	3A	1	R	5E	1	R	82	1	R	A6	1	R	CA	1	R	EE	1	R	
17	1	R	3B	1	R	5F	1	R	83	1	R	A7	1	R	CB	1	R	EF	1	R	
18	1	X	3C	1	X	60	1	X	84	1	X	A8	1	X	CC	1	X	F0	1	X	
19	0	H	3D	0	H	61	0	H	85	0	H	A9	0	H	CD	0	H	F1	0	H	
1A	1	0	3E	1	0	62	1	0	86	1	0	AA	1	0	CE	1	0	F2	1	0	
1B	1	g	3F	1	g	63	1	g	87	1	g	AB	1	g	CF	1	g	F3	1	g	
1C	1	g	40	1	g	64	1	g	88	1	g	AC	1	g	D0	1	g	F4	1	g	
1D	1	g	41	1	g	65	1	g	89	1	g	AD	1	g	D1	1	g	F5	1	g	
1E	1	g	42	1	g	66	1	g	8A	1	g	AE	1	g	D2	1	g	F6	1	g	
1F	1	g	43	1	g	67	1	g	8B	1	g	AF	1	g	D3	1	g	F7	1	g	
20	1	g	44	1	g	68	1	g	8C	1	g	B0	1	g	D4	1	g	F8	1	g	
21	1	B	45	1	B	69	1	B	8D	1	B	B1	1	B	D5	1	B	F9	1	B	
22	0	L	46	0	L	6A	0	L	8E	0	L	B2	0	L	D6	0	L	FA	0	L	
23	1	0	47	1	0	6B	1	0	8F	1	0	B3	1	0	D7	1	0	FB	0	0	NEXT ADDR = 00

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FIGURE 8. Template for PROM Program for Filter Controller

SUMMARY

The use of the NMC87C257 CMOS PROM with latches has been shown to be an effective element in the implementation of several MICROWIRE interfaces. This use allows the designer to implement systems with devices necessitating a MICROWIRE interface without the use of a microcontroller or microprocessor.

In constructing or adapting any of the circuits described in this note the reader is advised to obtain copies of the National Semiconductor data sheets for the components included and to review their operation for applicability to their system requirements.

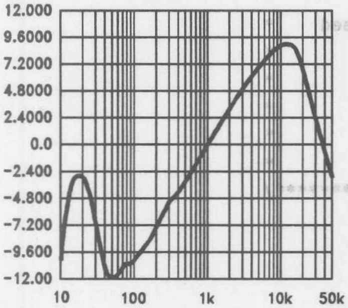

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FIGURE A1. A Ramp Transfer Characteristic. Refer to Table A1 for program inputs.

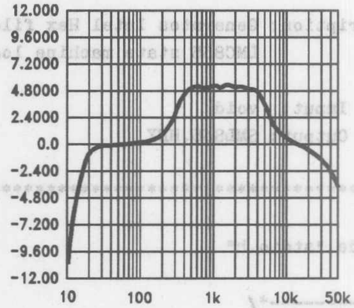

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FIGURE A2. Vocal Presence Filter. Refer to Table A2 for program inputs.

TABLE A1. Program Inputs for Ramp Transfer Characteristic

Frequency (Hz)	Level (dB)
40	−7
63	−6
100	−5
160	−4
250	−3
400	−2
630	−1
1k	0
1.6k	+1
2.5k	+2
4k	+3
6.3k	+4
10k	+5
16k	+6

TABLE A2. Program Inputs for Vocal Presence Filter

Frequency (Hz)	Level (dB)
40	0 Subsonic Filter
63	0
100	0
160	0
250	0
400	+3
630	+3
1k	+3
1.6k	+3
2.5k	+3
4k	+3
6.3k	0 Supersonic Filter
10k	0
16k	0

Figures A1 and *A2* are gain vs. frequency plots of specimen filters realized using the logic of *Figure 7* and PROM code generated with SM835.c.

```
/*************************************************************
*                                                            *
* File: SM835.C                                              *
* Author: Bob Moses, Rane Corporation, Mukilteo, WA          *
* Revision: 18 June 1991                                     *
* Compiler: Borland TurboC                                   *
*                                                            *
* Description: Generates Intel Hex file for NMC87C257 based  *
*              LMC835 state machine loader.                  *
*                                                            *
* File Input:  void                                          *
* File Output: SML835.HEX                                    *
*                                                            *
*************************************************************/

#include "stdio.h"

/*------------*/
/* Data Types */
/*------------*/

struct LMC835_RECORD
{
    int chAbands[7];   /* gains for chan A bands */
    int chArng;        /* chan A range */
    int chBbands[7];   /* gains for chan B bands */
    int chBrng;        /* chan B range */
};

/*--------------------*/
/* Function Prototypes*/
/*--------------------*/

void say_howdy(void);
void get_parameters(struct LMC835_RECORD *eq);
void compile_state_mach(struct LMC835_RECORD *eq, unsigned int states[]);
void output_data(unsigned int states[]);
void wr_ihex_data_rec(FILE *outfile, unsigned int addr, unsigned char recsize,
                      unsigned char data[]);

/*--------------*/
/* Main Program */
/*--------------*/

main()
{
    /* declare one LMC835 equalizer */
    struct LMC835_RECORD eql;
```

```
    say_howdy();
    get_parameters(&eql);
    compile_state_mach(&eql,states);
    output_data(states);
}

/*------------*/
/* Functions  */
/*------------*/

void say_howdy(void)
{
    clrscr();
    fprintf(stdout,"\nSM835 - NMC87C257 LM835 State Machine Loader.");
    fprintf(stdout,"\n\nThis Program accepts parameters for an LMC835-based");
    fprintf(stdout,"\nequalizer and generates an Intel Hex file ( SML835.HEX )");
    fprintf(stdout,"\nfor the NMC87C257 State Machine Loader. This file can be");
    fprintf(stdout,"\nloaded into most EPROM programmers and split-programmed");
    fprintf(stdout,"\n(even and odd bytes) into two EPROMs.");
    fprintf(stdout,"\n\nThe LMC835 graphic equalizer consists of two channels");
    fprintf(stdout,"\n(chan A & chan B), each channel has 7 bands. The range of");
    fprintf(stdout,"\neach band is selectable for ± 12 dB in 1 dB steps, or");
    fprintf(stdout,"\n± 6 dB in 1/2 dB steps.\n");
}

void get_parameters(struct LMC835_RECORD *eq)
{
    unsigned int i,currng;
    int tempint;
    char chan;
    float tempfloat;

    /* get range for chan A */
    fprintf(stdout,"\nPlease enter range of chan A (0 = ±12dB, 1 = ±6dB): ");
    fscanf(stdin,"%d",&tempint);
    eq->chArng = tempint&0x0001;

    /* get range for chan B */
    fprintf(stdout,"Please enter range of chan B (0 = ±12dB, 1 = ±6dB): ");
    fscanf(stdin,"%d",&tempint);
    eq->chBrng = tempint&0x0001;
```

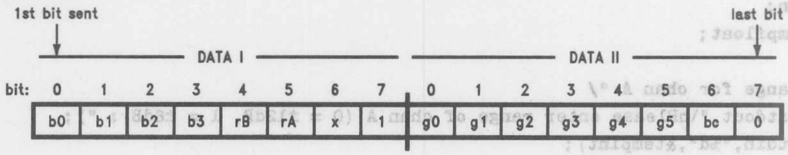
4

```
        /* if start of chan B, modify chan flag and chan range variables */
        if(i == 7)
        {
            chan = 'B';
            currng = 12-6*(eq->chBrng);
        }
        /* get a band value */
        fprintf(stdout,"Gain of chan %c band #%d? ",chan,(i%7)+1);
        fscanf(stdin,"%g",&tempfloat);

        /* scale for range */
        if(currng == 6) tempint = (int)(tempfloat*2.0);
        else tempint = (int)tempfloat;

        /* check limits */
        if((tempint > 12) || (tempint < -12))
        {
            fprintf(stderr,"...err! value must be between -%d and +%d\n",currng,currng);
            continue;
        }
        /* save band */
        if(chan == 'A') eq->chAbands[i] = tempint;
        else eq->chBbands[i-7] = tempint;
        i++; /* band counter */
    }
}
void compile_state_mach(struct LMC835_RECORD *eq, unsigned int states[])
{
```

LMC835 CONTROL CODES



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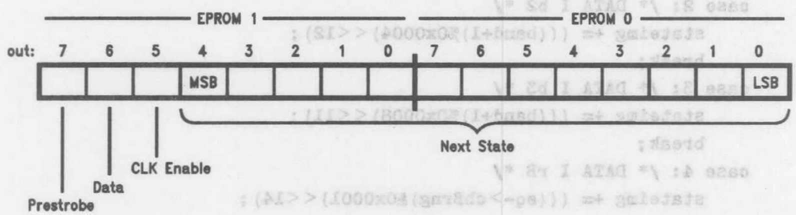
```
/*

   State Machine:
   --------------

   --- State ------------------------------- Outputs -------------------
   Current   Next  |          Data               Prestrobe    CLK Enable
   -------   ----  | ------------------------    ---------    ----------
      0        1   | Chan A, band 1, DATA I b0       0            0
      1        2   | Chan A, band 1, DATA I b1       0            0
      2        3   | Chan A, band 1, DATA I b2       0            0
      3        4   | Chan A, band 1, DATA I b3       0            0
      4        5   | Chan A, band 1, DATA I rB       0            0
      5        6   | Chan A, band 1, DATA I rA       0            0
      6        7   | Chan A, band 1, DATA I x        0            0
      7        8   | Chan A, band 1, DATA I 1        1            0
      8        9   | rest for strobe                 0            0
      9        9   | Chan A, band 1, DATA II g0      0            0
     10       11   | Chan A, band 1, DATA II g1      0            0
     11       12   | Chan A, band 1, DATA II g2      0            0
     12       13   | Chan A, band 1, DATA II g3      0            0
     13       14   | Chan A, band 1, DATA II g4      0            0
     14       15   | Chan A, band 1, DATA II g5      0            0
     15       16   | Chan A, band 1, DATA II bc      0            0
     16       17   | Chan A, band 1, DATA II 0       1            0
     17       18   | rest for strobe                 0            0
     18       19   | Chan A, band 2, DATA I b0       0            0
      :        :   :           :                     :            :
     34       35   | Chan A, band 2, DATA II 0       1            0
     35       36   | rest for strobe                 0            0
      :        :   :           :                     :            :
    124      125   | Chan A, band 7, DATA II 0       1            0
    125      126   | rest for strobe                 0            0
    126      127   | Chan B, band 1, DATA I b0       0            0
      :        :   :           :                     :            :
    250      251   | Chan B, band 7, DATA II 0       1            0
    251      252   | rest for strobe                 0            0
    252      252   |           0                     0            1
   ---------------------------------------------------------------------
```

TL/D/11274-13

```
  NMC87C257 pin connections:
  --------------------------
```



TL/D/11274-12

```
/*
```


4

```
    unsigned int band,substate,stateimg,curstate;
    unsigned char LMC835GainCodeTable[] = [0x2F,0x2D,0x29,0x01,0x16,0x2A,
                                           0x12,0x02,0x04,0x08,0x10,0x20,
                                           0x00,
                                           0x20,0x10,0x08,0x04,0x02,0x12,
                                           0x2A,0x16,0x01,0x29,0x2D,0x2F};

    /*---------*/
    /* chan A */
    /*---------*/

    for(band = 0,curstate = 0;band < 7;band++)
    {
        for(substate = 0;substate < 18;substate++)
        {
            /* next state = current state +1 */
            stateimg = (curstate+1)&0x1FFF;

            /* CLK Enable */
            stateimg &= 0xDFFF;

            /* Prestrobe */
            if((substate == 7)||(substate == 16)) stateimg += 0x8000;

            /* Data */
            switch(substate)
            {
                case 0: /* DATA I b0 */
                    stateimg += (((band+1)&0x0001)<<14);
                    break;
                case 1: /* DATA I b1 */
                    stateimg += (((band+1)&0x0002)<<13);
                    break;
                case 2: /* DATA I b2 */
                    stateimg += (((band+1)%0x0004)<<12);
                    break;
                case 3: /* DATA I b3 */
                    stateimg += (((band+1)%0x0008)<<11);
                    break;
                case 4: /* DATA I rB */
                    stateimg += (((eq->chBrng)&0x0001)<<14);
                    break;
                case 5: /* DATA I rA */
                    stateimg += (((eq->chArng)&0x0001)<<14);
                    break;
                case 6: /* DATA I don't care */
                    break;
                case 7: /* DATA I 1 */
                    stateimg += 0x4000;
                    break;
*/
```

4

```
                case 8: /* rest for strobe */
                    break;
                case 9: /* DATA II g0 */
                    stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0001)<<14);
                    break;
                case 10: /* DATA II g1 */
                    stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0002)<<13);
                    break;
                case 11: /* DATA II g0 */
                    stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0004)<<12);
                    break;
                case 12: /* DATA II g3 */
                    stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0008)<<11);
                    break;
                case 13: /* DATA II g4 */
                    stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0010)<<10);
                    break;
                case 14: /* DATA II g5 */
                    stateimg += ((LMC835GainCodeTable[eq->chAbands[band]+12]&0x0020)<<9);
                    break;
                case 15: /* DATA II bc ( 0 = cut, 1 = boost) */
                    if(eq->chAbands[band] < 0) stateimg &= 0xBFFF;
                    else stateimg += 0x4000;
                    break;
                case 16: /* DATA II 0 */
                    stateimg &= 0xBFFF;
                    break;
                case 17: /* rest for strobe */
                    break;
            } /* switch... */

            /* write this state to states array */
            states[curstate++] = stateimg;

        } /* for(substate... */
    } /* for(band... */

    /*--------*/
    /* chan B */
    /*--------*/

    for(band = 7;band < 14;band++)
    {
        for(substate = 0;substate < 18;substate++)
        {
            /* next state = current state +1 */
            stateimg = (curstate+1)&0x1FFF;

            /* CLK Enable */
            stateimg &= 0xDFFF;
```

4

```
/* Data */
switch(substate)
{
    case 0: /* DATA I b0 */
        stateimg += (((band+1)&0x0001)<<14);
        break;
    case 1: /* DATA I b1 */
        stateimg += (((band+1)&0x0002)<<13);
        break;
    case 2: /* DATA I b2 */
        stateimg += (((band+1)&0x0004)<<12);
        break;
    case 3: /* DATA I b3 */
        stateimg += (((band+1)&0x0008)<<11);
        break;
    case 4: /* DATA I rB */
        stateimg += (((eq->chBrng)&0x0001)<<14);
        break;
    case 5: /* DATA I rA */
        stateimg += (((eq->chArng)&0x0001)<<14);
        break;
    case 6: /* DATA I don't care */
        break;
    case 7: /* DATA I 1 */
        stateimg += 0x4000;
        break;
    case 8: /* rest for strobe */
        break;
    case 9: /* DATA II g0 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0001)<<14);
        break;
    case 10: /* DATA II g1 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0002)<<13);
        break;
    case 11: /* DATA II g2 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0004)<<12);
        break;
    case 12: /* DATA II g3 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0008)<<11);
        break;
    case 13: /* DATA II g4 */
        stateimg += ((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0010)<<10);
        break;
```

```
            case 14: /* DATA II g5 */
stateimg +=((LMC835GainCodeTable[eq->chBbands[band-7]+12]&0x0020)<<9);
                break;
            case 15: /* DATA II bc ( 0 = cut, 1 = boost) */
                if(eq->chBbands[band-7] < 0) stateimg &= 0xBFFF;
                else stateimg += 0x4000;
                break;
            case 16: /* DATA II 0 */
                stateimg &= 0xBFFF;
                break;
            case 17: /* rest for strobe */
                break;
        } /* switch... */

        /* write this state to states array */
        states[curstate++] = stateimg;

      } /* for(substate... */
    } /* for(band... */

    /* final state: "jump 0" with clock disabled */
    states[252] = 252+0x2000;
}

void output_data(unsigned int states[])
{
    unsigned int i,addr,bitmask;
    unsigned char csum,data[16];
    FILE *outfile;

    /* open output file */
    if((outfile = fopen("sml835.hex","w")) == NULL )
    {
        fprintf(stderr,"can't open file SML835.HEX");
        exit(0);
    }

    /* write states to stdout */
    /*--------------------------*/
    for(i = 0;i < 253;i++)
{
        if(i == 252) fprintf(stdout,"\n\nFinal state...");
        else if (!(i&18)) fprintf(stdout,"\n\nBand %d...",(i/18)+1);
        fprintf(stdout,"\nState %d: ",i);

        /* write each state as a binary image  */
        for(bitmask = 0;bitmask < 16;bitmask++)
        {
            if((states[i]<<bitmask)&0x8000) fprintf(stdout,"1");
            else fprintf(stdout,"0");
        }
    }
```

4

```
    /* write states to Intel Hex file */
    /*---------------------------------*/
    fprintf(stdout,"\n\nWriting Intex Hex file: SML835.HEX...\n");

    /* write first 252 states */
    for(addr = 0;addr < 252;addr += 8)
    {
        /* copy 8 states (16 bytes) to temp data buffer */
        for(i = 0;i < 16;i += 2)
        {
            data[i] = (char)(states[addr+(i/2)]&0x00FF);
            data[i+1] = (char)((states[addr+(i/2)]>>8)*0x00FF);
        }

        /* write data to Intex Hex record */
        wr_ihex_data_rec(outfile,addr*2,16,data);
    }

    /* write last state */
    data[0] = (char)(states[252]&0x00FF);
    data[1] = (char)((states[252]>>8)&0x00FF);
    wr_ihex_data_rec(outfile,252*2,2,data);

    /* EOF record */
    fprintf(outfile,"\n:00000001FF");

    /* close file */
    fclose(outfile);
}

void wr_ihex_data_rec(FILE *outfile, unsigned int addr, unsigned char recsize, unsigned char
data[])
{
    unsigned int i;
    unsigned char csum;

    /* record mark, record length, record address, and record type fields */
    fprintf(outfile,"\n:%2.2X%4.4X00",recsize,addr);
    csum = recsize + (char))addr&0x00FF) + (char)((addr>>8)&0x00FF);

    /* data field */
    for(i = 0;i < recsize;i++)
    {
        fprintf(outfile,"%2.2X",data[i]);
        csum += data[i];
    }

    /* checksum field */
    csum &= 0x00FF;
    csum *= -1;
    fprintf(outfile,"%2.2X",csum);
}
```

BIBLIOGRAPHY

NMC87C257 — CMOS PROM with Address Latches

ADC0854 — Multiplexed Comparator with 8-bit Reference Divider

FSA2619 — Monolithic Diode Array

MM74C14 — Hex CMOS Schmitt Trigger

NM93C06 — 256-bit Electrically Erasable Programmable Memory

MM74C923 — 20 Key Encoder

LMC35 — Digital Controlled Graphic Equalizer

AN-452 — MICROWIRE Serial Interface

AN-140 — CMOS Schmift Trigger

Appendix

ACKNOWLEDGEMENTS

The author would like to express his gratitude to the engineering staff at Rane Corporation in Mukilteo, Washington for providing expert assistance and breadboarding of the LMC835 application and to Bob Moses for contributing a C program (see Appendix) to generate the ROM map.

Section 5
Quality and Reliability

Section 5 Contents

National Semiconductor

Non-Volatile Memory Reliability Information

The reliability performance of National Semiconductor's Non-Volatile Memories is assured through the use of conservative design rules, stringent product qualification criteria, and monthly ongoing reliability audits. When manufactured on our well defined and SPC controlled wafer fabrication and assembly processes, the result is memory products which provide outstanding reliability.

QUALIFICATION

All new products, redesigned products, process changes, and package/assembly changes are subjected to a rigorous regime of stress testing prior to release for sale. All National EPROM, EEPROM, and FLASH memories are subjected to stress testing which includes: High Temperature Operating Life Test, Temperature Cycling, High Temperature Storage, ESD, and Latch-Up Characterization. Plastic packages, additionally, receive Temperature Humidity Bias and Autoclave testing. Three lots from three distinct wafer fabrication and assembly lots are used.

In addition to these customary demonstrations of robustness, other tests unique to memory devices are employed. The ability to program, retain program, and erase are fundamental attributes of any EPROM, EEPROM or FLASH memory. These characteristics are tested at multiple thousands of program-and-erase cycles. Data retention is assessed through the use of a 250°C static bake (150°C for plastic packages). The evaluation devices typically are programmed to a checkerboard pattern.

National's qualification requirements are detailed in Table I.

RELIABILITY AUDIT

Each month, samples of representative device families and package styles are drawn from actual production lots and submitted to Operating Life, Temperature Humidity Bias, Temperature Cycling and Autoclave Tests. This ongoing assessment of the outgoing reliability characteristics provides certainty that there is no change in the product going to customers.

Ongoing Reliability Audit criteria are found in Table II.

PRE-CONDITIONING

It has been well established that plastic surface mount IC package reliability can be compromised by the stresses of the various SMD solder attachment techniques. The package cracking is a result of the rapid egress of absorbed package moisture during IR, Vapor Phase, or other SMD soldering methods. This harsh assembly environment represents actual practice in manufacturing, but also presents a dilema to the Component Reliability Engineer. Environmental stress tests conducted to assess reliability attributes and device life could yield misleading data if the potential effects of the rigors of SMD assembly are not, in some way, considered. Recognizing these facts, National has implemented a regime of preconditioning devices, prior to subjecting parts to on-going Reliability audits. Since many customers' circuit boards include both through-hole and SMD devices, this regime has been expanded to include plastic DIPs.

The following defines the preconditioning used on audit samples prior to temperature-humidity-bias (THBT) tests and autoclave (ACLV).

Surface Mount Package

- 30 temp cycles, −65°C to +150°C
- Bake, 8 hrs @ 125°C
- Moisture soak
- 3 Simulated IR or VPS reflow cycles
- Flux immersion and clean

Through-Hole

- 30 temp cycles, −65°C to +150°C
- Moisture soak
- Flux immersion and clean

TABLE I. Qualification Criteria

Test	Conditions	Duration	Sample Size	Accept Number
Operating Life (Dynamic Burn-In)	V_{CC}: 5.5V Temperature: 150°C	1,000 Hours	100 x 3	0
Temperature/Humidity/Bias	V_{CC}: 5.5V Temperature: 85°C Humidity: 85% RH	1,000 Hours	100 x 3	0
Temperature Cycle (Unbiased)	−65°C ⟷ +150°C	1,000 Cycles	100 x 3	0
Autoclave (Unbiased)	Temperature: 121°C Pressure: 15 PSIG RH = 100%	500 Hours	100 x 3	0
High Temperature Storage Life	Temperature: 150°C (Plastic) 250°C (Ceramic)	1,000 Hours	100 x 3	0
Electrostatic Discharge (ESD)	Human Body Model Voltage: 2,000V		25 x 3	0

Note 1: Three distinctly different lots are used.

TABLE II. Periodic Audit Criteria

Test	Conditions	Duration	Sample Size	Accept Number
Operating Life (Dynamic Burn-In)	V_{CC}: 5.5V Temperature: 150°C	1,000 Hours	100 x 3	0
Temperature/ Humidity/Bias	V_{CC}: 5.5V Temperature: 85°C Humidity: 85% RH	1,000 Hours	100 x 3	0
Temperature Cycle (Unbiased)	−65°C ←→ +150°C	1,000 Cycles	100 x 3	0
Autoclave (Unbiased)	Temperature: 121°C Pressure: 15 PSIG	500 Hours	100 x 3	0

Reliability Testing

Reliability-"The characteristic of an item expressed by the probability that it will perform its required function under the stated conditions for a stated period of time."

Any statement about reliability, directly or indirectly, includes some measure of time. The prime interest is in what an item's *future* state will be, rather than its current condition. As such, reliability testing attempts to predict the future. To accomplish this, accelerated stress test techniques are utilized to "speed up the clock". These stress tests typically employ temperature, voltage, mechanical shock and humidity to accelerate the natural aging process of integrated circuits. The stress tests most commonly used at National, for Qualification and Reliability Audit, are discussed in the following paragraphs.

OPL—OPERATING LIFE TEST

High temperature operating life test is the most commonly used and generally accepted accelerated life test in the semiconductor industry. The role of high temperature in accelerating chemical and physical failure mechanisms has long been known and established. In this test, sample devices are exercised under bias while being subjected to elevated temperatures (most frequently 125°C or 150°C) for extended periods of time. The voltage and temperature stresses of this test can actively promote such failure mechanisms as oxide breakdown, electro-migration, surface or bulk leakage, ionic contamination or channeling that may indicate design or manufacturing deficiencies.

THBT—TEMPERATURE-HUMIDITY-BIAS TEST

Temperature-Humidity-Bias testing at 85°C, 85% Relative Humidity is the industry standard environmental stress test whose role is to accelerate electro-chemical failures of plastic packaged devices through the application of moisture, temperature, and bias. Unlike hermetic cavity packages, moisture can permeate the plastic encapsulant and reach the die. The applied bias is used to create potential electrolytic cells which accelerate corrosion of die metallization (the primary failure mechanism) and increase ionic mobility. This test is usually continued for 1000 hours.

HE—HOT ELECTRON TEST

This test, similar to OPL but at low temperature (−40°C), is performed to assess whether devices are sensitive to hot electron injection. Non-Volatile Memories depend on the presence or absence of stored charge on a floating gate as the logic storage element. Any unintentional injection (or loss) of charge is not desirable and could change the logic state. With this test, worst case conditions of low temperature and accelerating field (voltage) are used to accelerate any possible hot electron effects. Hot electron effects are a function of channel length, oxide thicknesses, junction depth, channel doping level and passivation materials, therefore, it is more often used as a device design or process qualification test.

TMCL—TEMPERATURE CYCLE TEST

In this test, devices are cycled between hot and cold air chambers to determine the resistance of devices to exposure at temperature extremes. The rapid change in temperature extremes from −65°C to +150°C provides mechanical stresses far greater than those expected during a typical device's lifetime of operation within data sheet conditions.

ACLV—AUTOCLAVE TEST

Autoclave is a highly accelerated environmental test which assesses the mechanical integrity of the plastic encapsulation system and the resultant effects of galvanic corrosion. Here, pressure, temperature, and humidity are employed in stressing the plastic encapsulated devices. The stress conditions of 121°C, 100% R.H. at 15 PSIG, are applied for durations of up to 500 hours.

BAKE—HIGH TEMPERATURE BAKE

High temperature storage at 150°C or 250°C, unbiased, is performed to measure the ability of National's non-volatile memories to retain data after having been programmed.

ESD TEST

Establishes the device's susceptibility to Electro-Static Discharge damage. This destructive test is done using the Human Body Model, per MIL STD 883, Method 3015.

LATCH-UP TEST

This test attempts to induce latch-up in device input/outputs. Voltage/currents are forced on I/O pins in an effort to trigger an SCR-like high current latched condition. This test procedure is per JEDEC Standard No. 17.

Section 6

Physical Dimensions

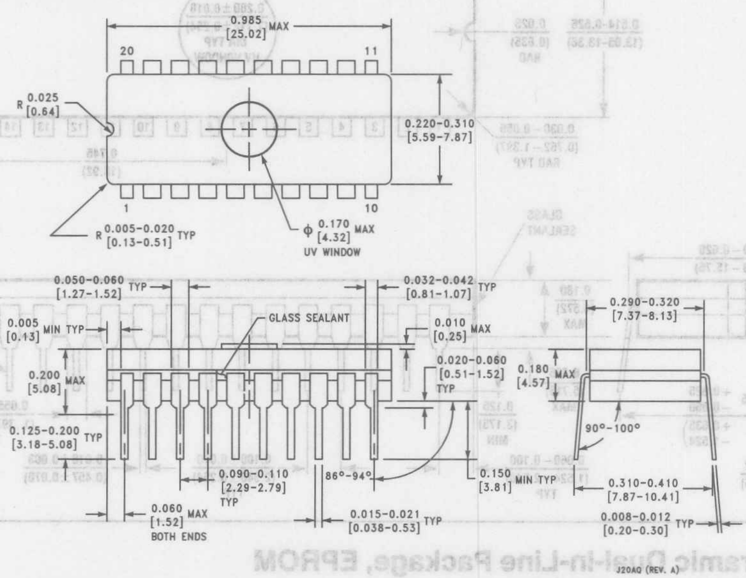
Section 6 Contents

6

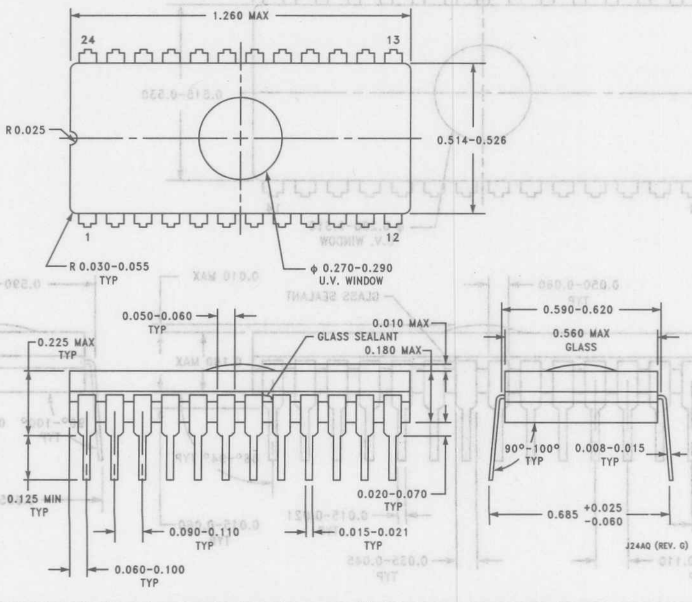
National Semiconductor

All dimensions are in inches (millimeters)

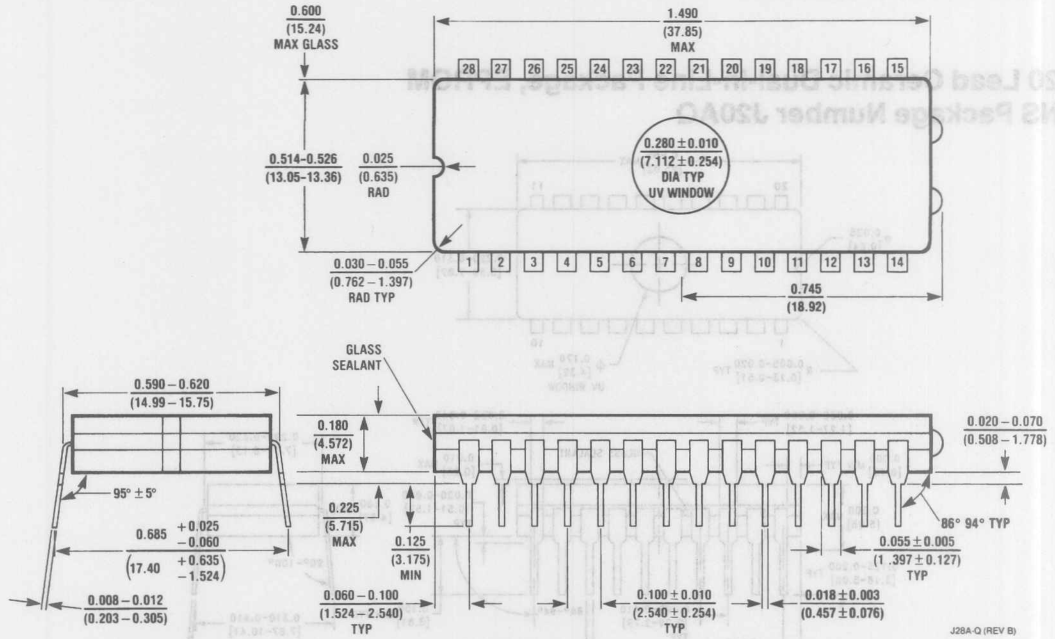
20 Lead Ceramic Dual-in-Line Package, EPROM
NS Package Number J20AQ



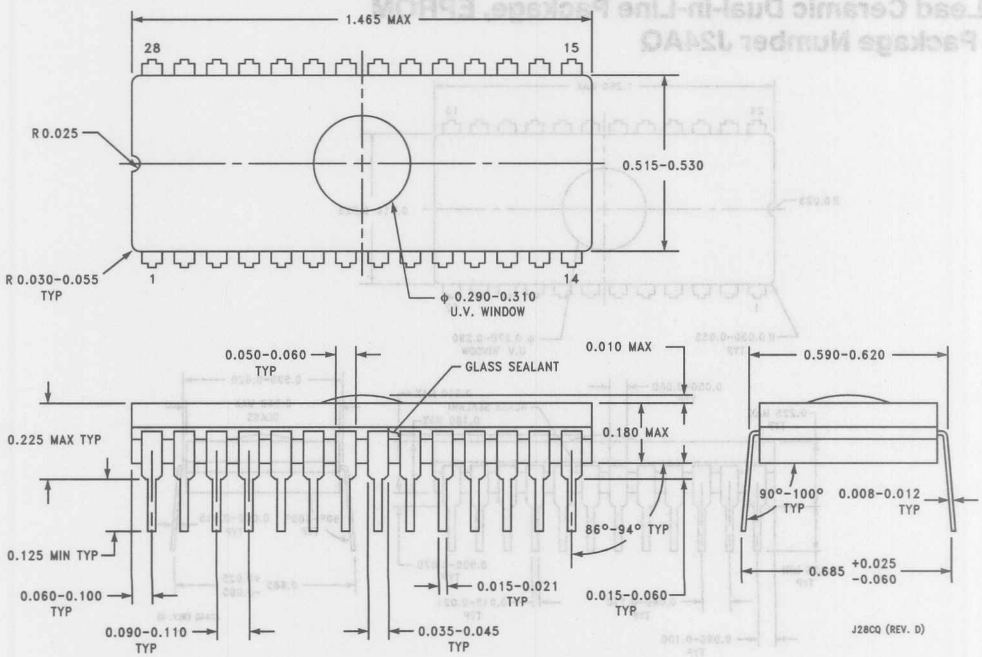
24 Lead Ceramic Dual-in-Line Package, EPROM
NS Package Number J24AQ



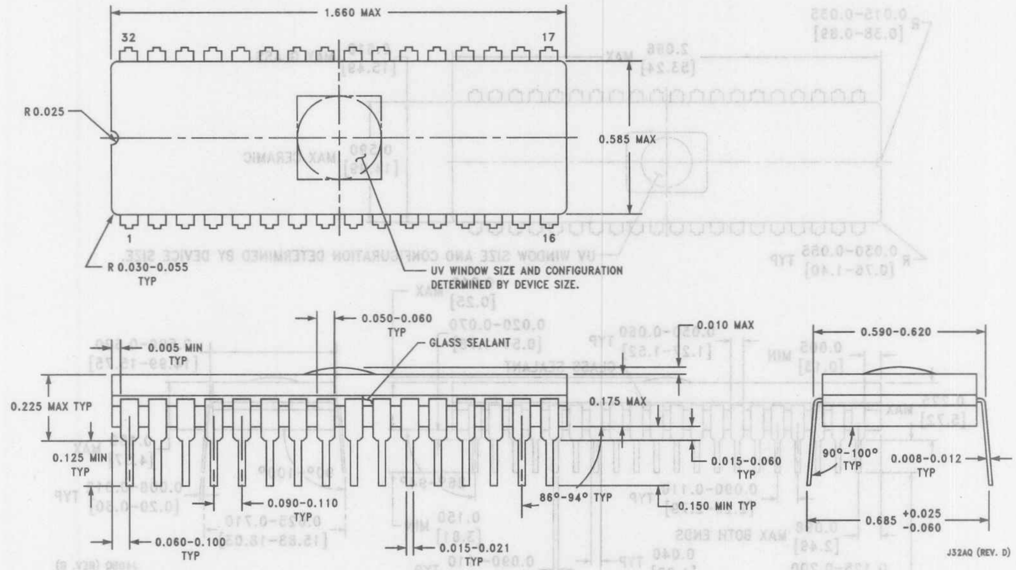
28 Lead Ceramic Dual-in-Line Package, EPROM
NS Package Number J28AQ



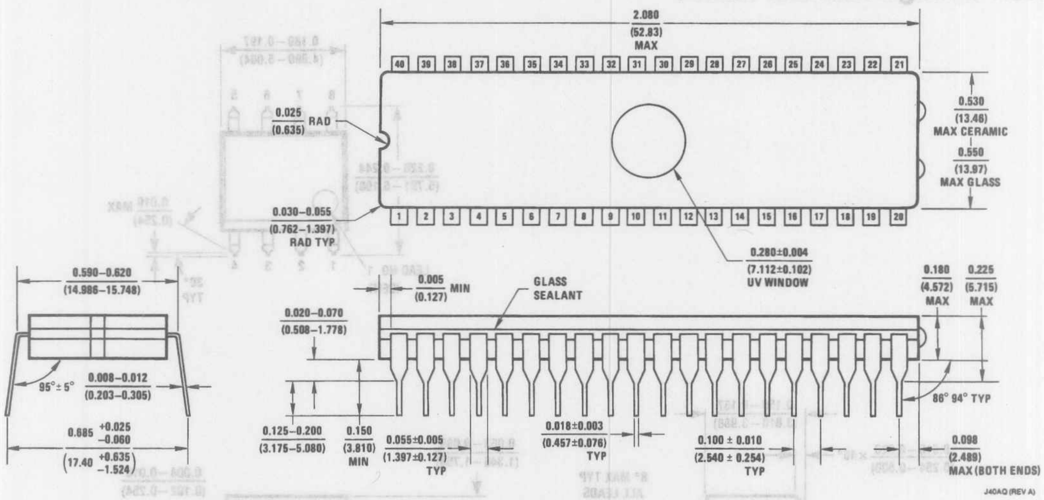
28 Lead Ceramic Dual-in-Line Package, EPROM
NS Package Number J28CQ

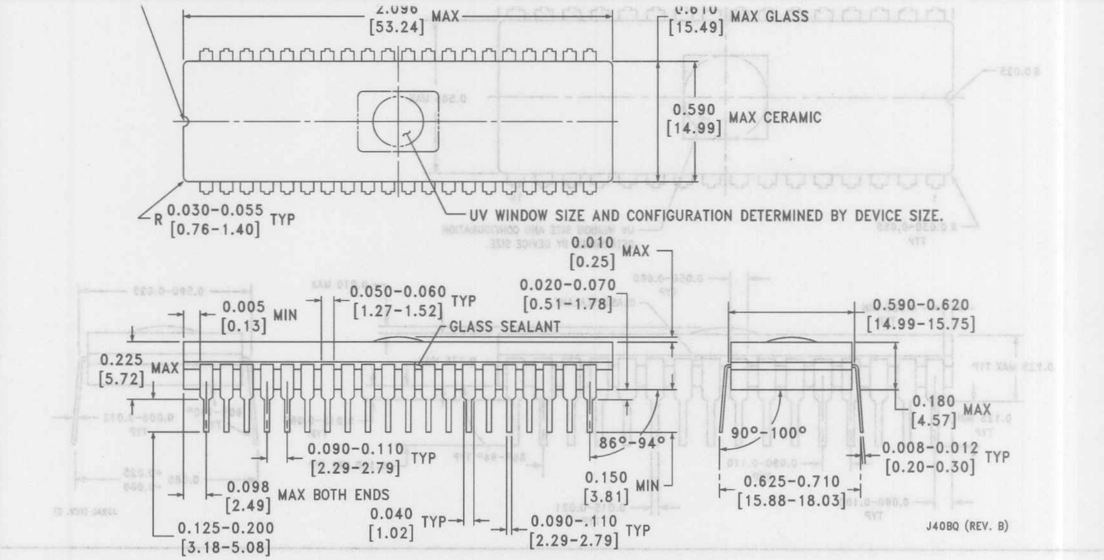


32 Lead Ceramic Dual-in-Line Package, EPROM
NS Package Number J32AQ

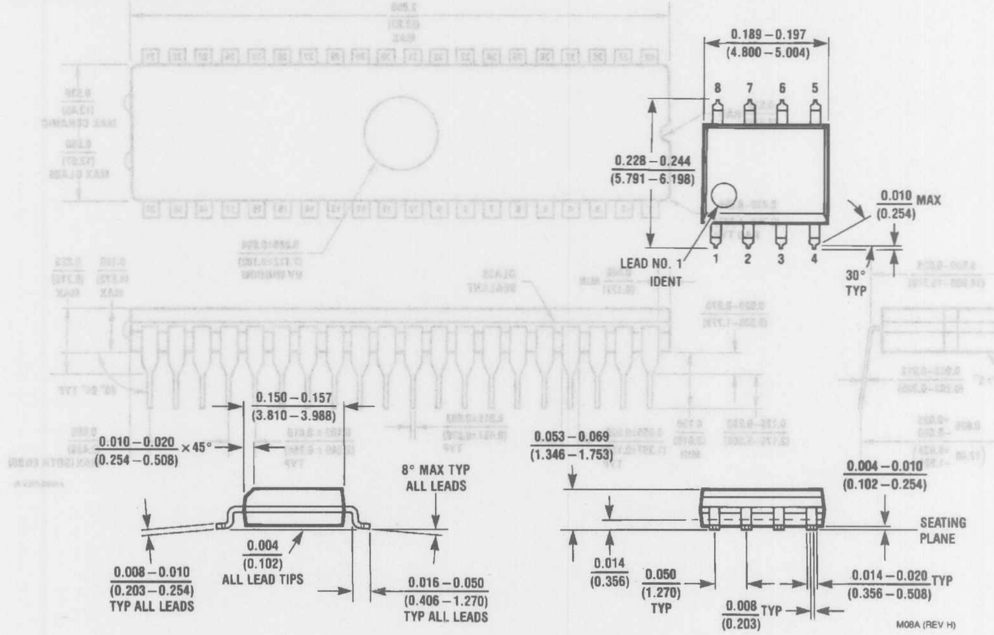


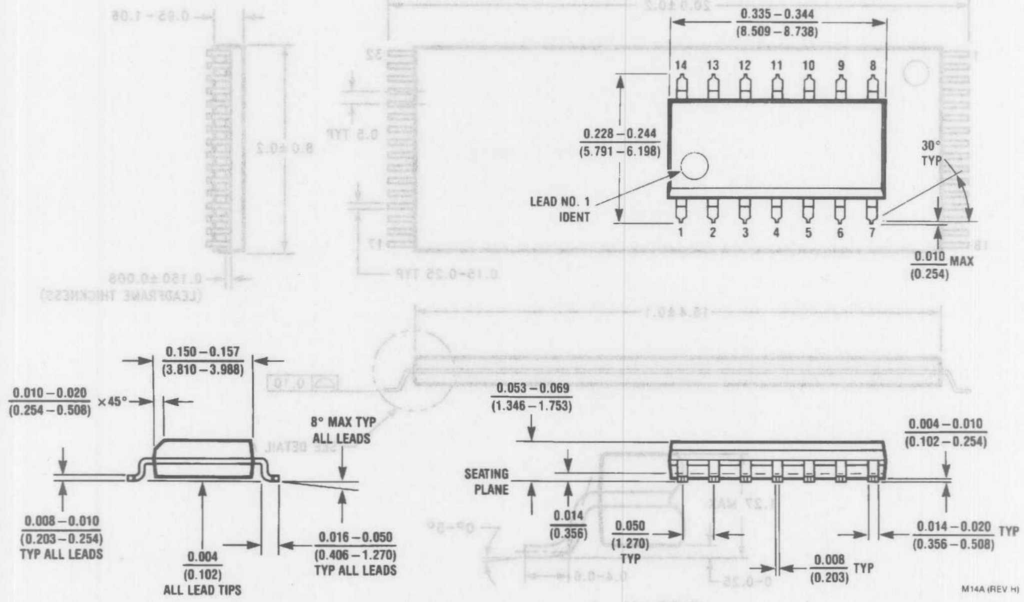
40 Lead Ceramic Dual-in-Line Package, EPROM
NS Package Number J40AQ



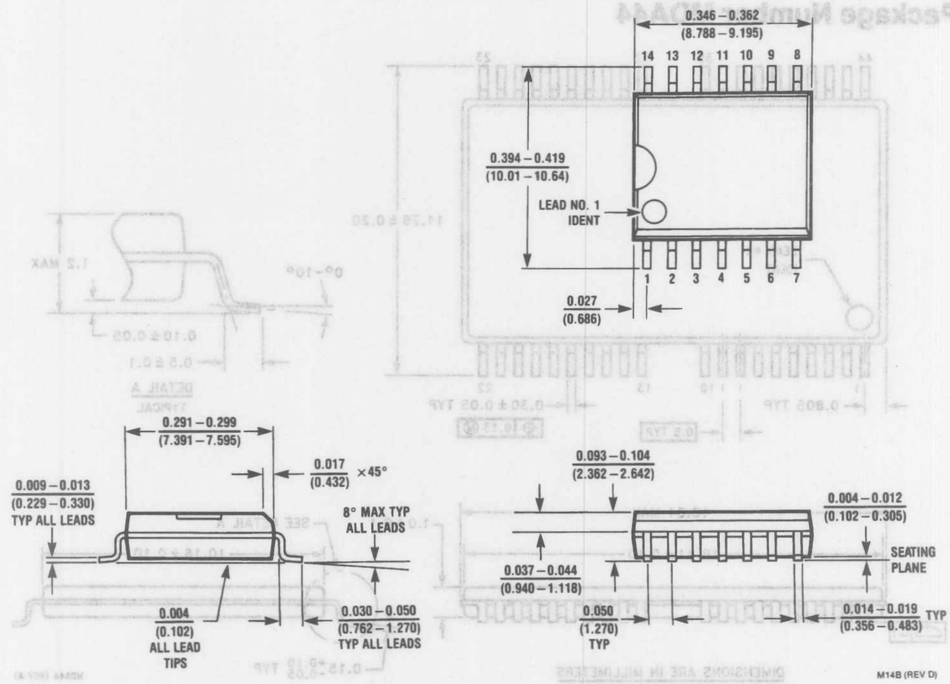


8 Lead (0.150″ Wide) Molded Small Outline Package, JEDEC
NS Package Number M08A

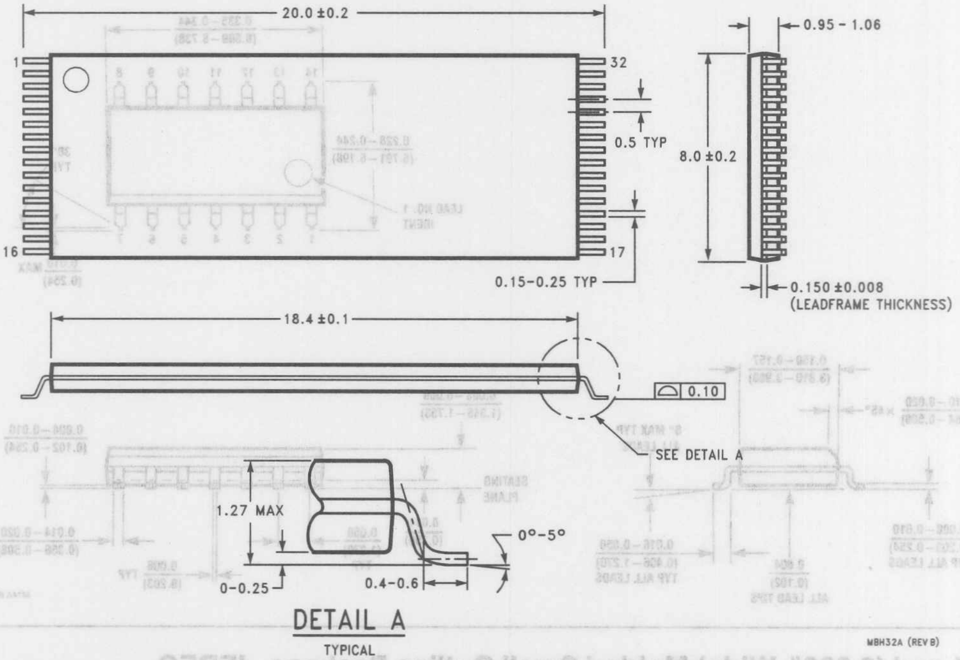




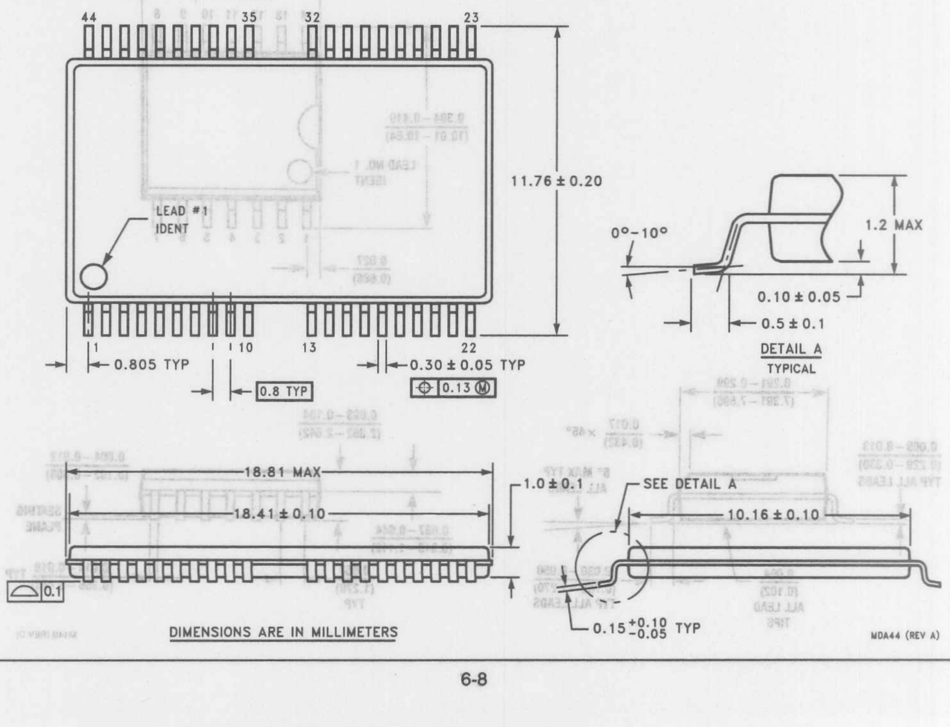
14 Lead (0.300″ Wide) Molded Small Outline Package, JEDEC
NS Package Number M14B



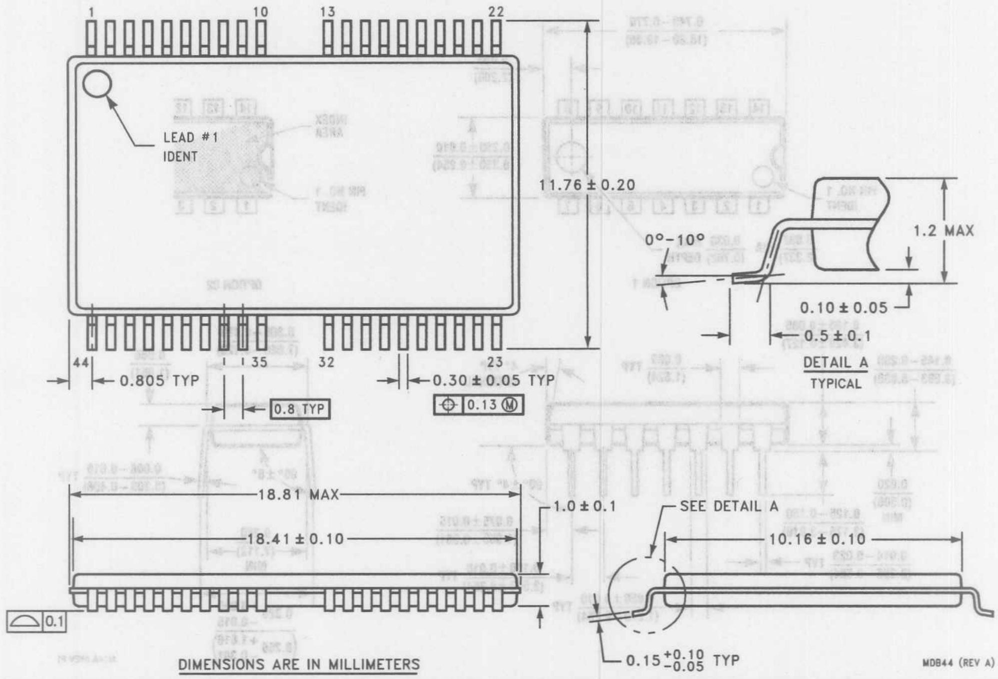
32 Lead Molded Thin Small Outline Package, EIAJ, Type I
NS Package Number MBH32A



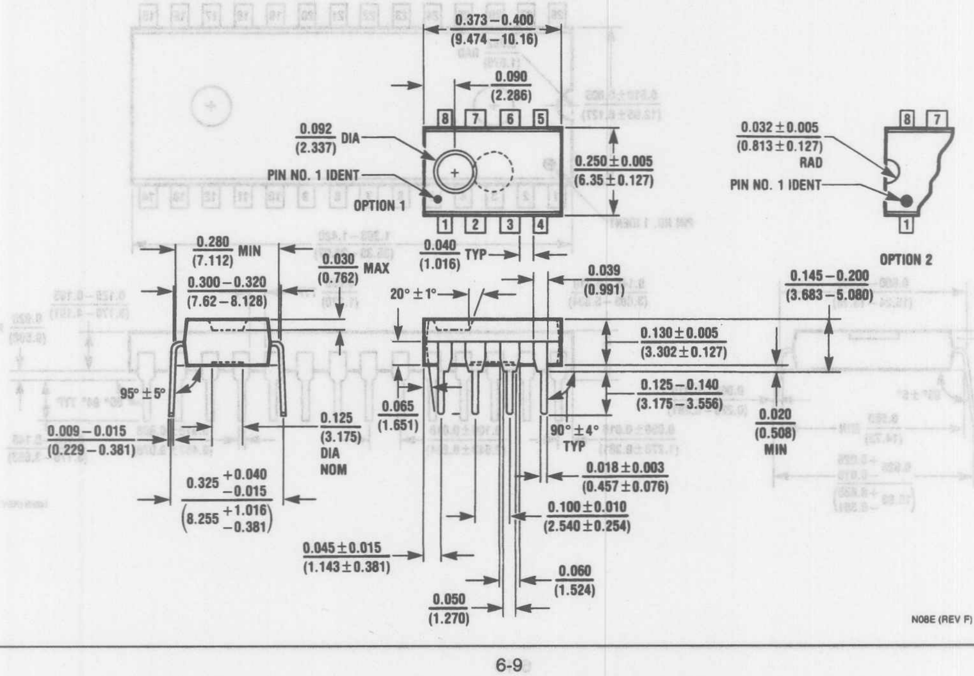
44 Lead Thin Small Outline Package, EIAJ, Type II
NS Package Number MDA44



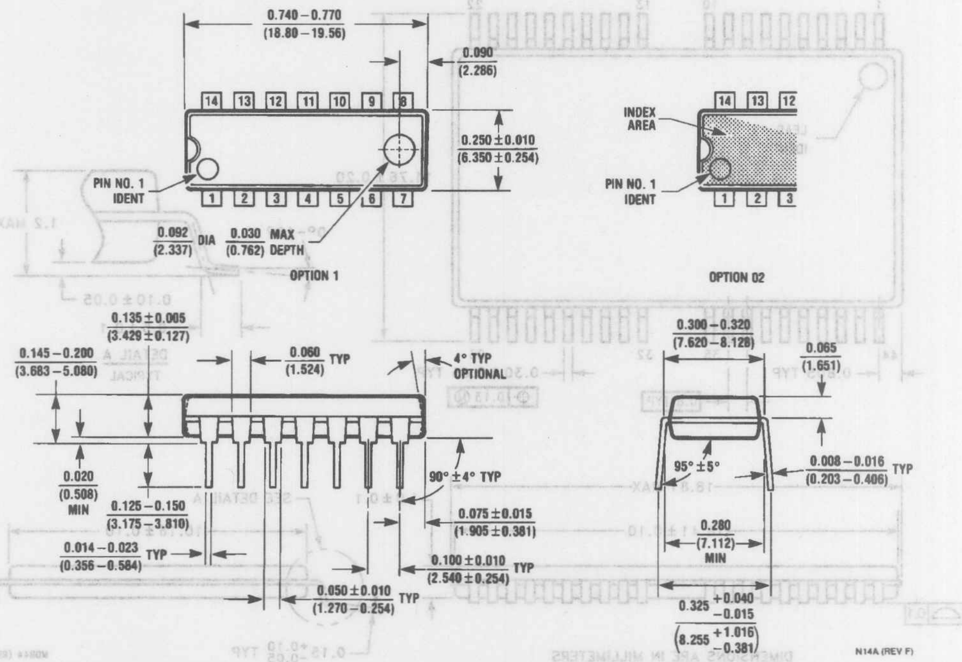
44 Lead Thin Small Outline Package, EIAJ, Type II
NS Package Number MDB44



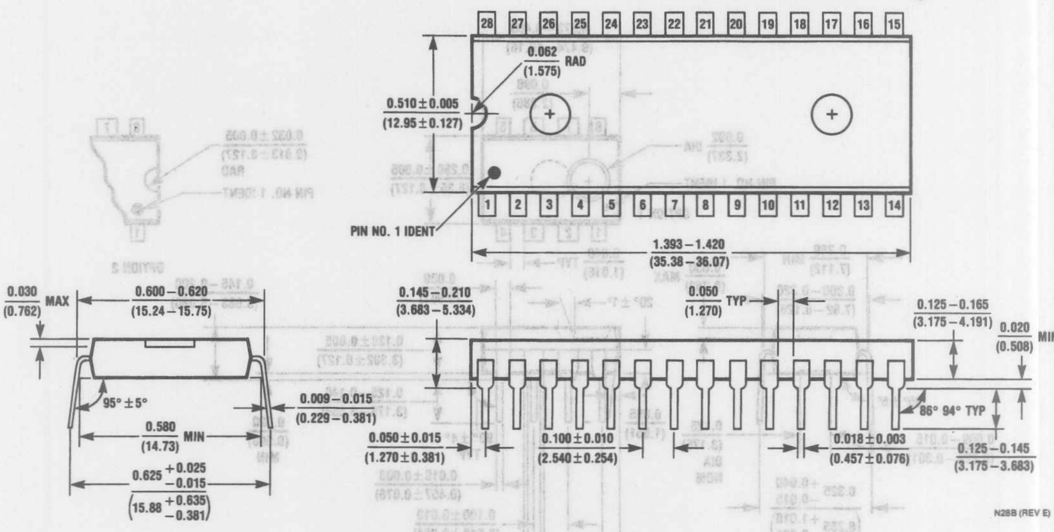
8 Lead (0.300″ Wide) Molded Dual-in-Line Package
NS Package Number N08E



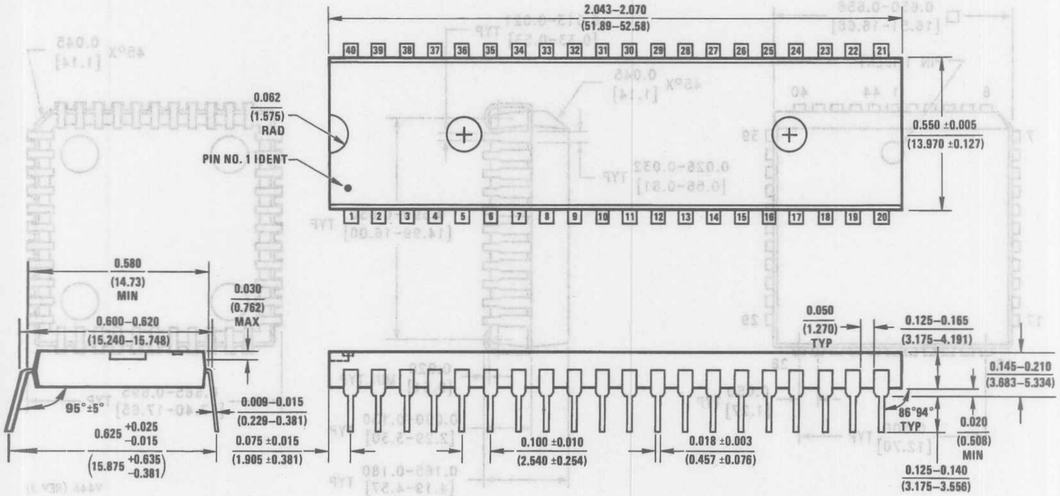
14 Lead (0.300″ Wide) Molded Dual-in-Line Package
NS Package Number N14A



28 Lead (0.600″ Wide) Molded Dual-in-Line Package
NS Package Number N28B

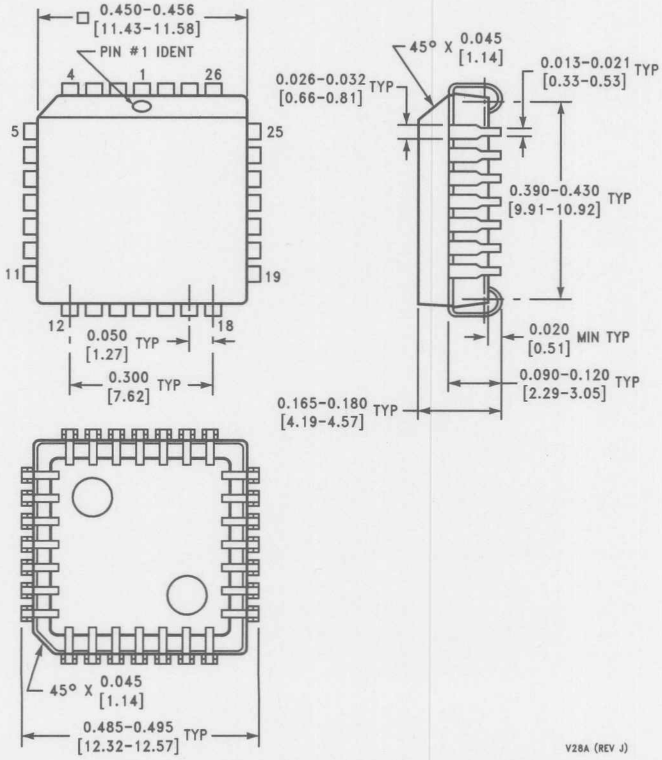


40 Lead (0.600″ Wide) Molded Dual-in-Line Package
NS Package Number N40A

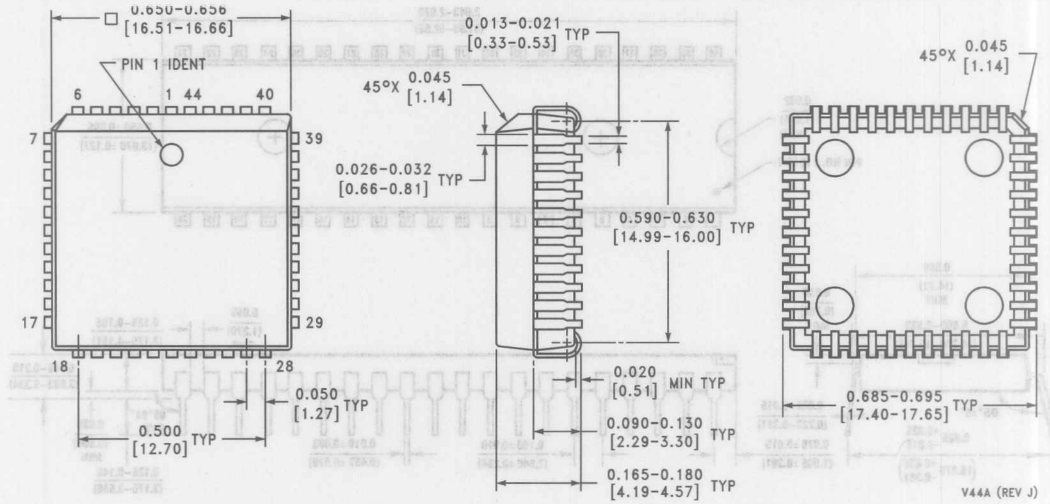


N40A (REV E)

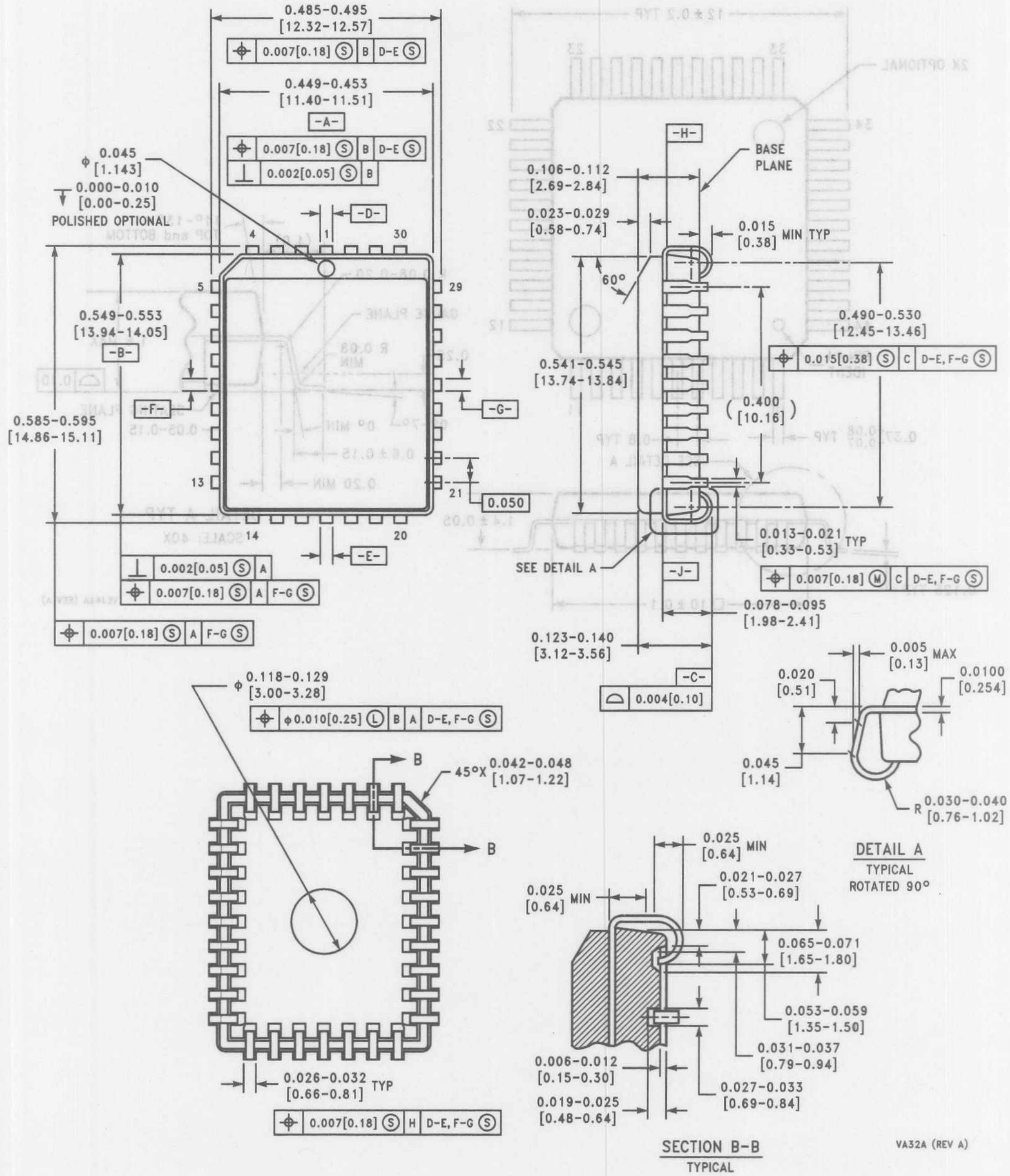
28 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V28A



V28A (REV J)


0.650-0.656
[16.51-16.66]
PIN 1 IDENT
6
1
44
40
7
39
17
29
18
28
0.050
[1.27]
TYP
0.500
[12.70]
TYP
0.013-0.021
[0.33-0.53]
TYP
45°X
0.045
[1.14]
0.026-0.032
[0.66-0.81]
TYP
0.590-0.630
[14.99-16.00]
TYP
0.020
[0.51]
MIN TYP
0.090-0.130
[2.29-3.30]
TYP
0.165-0.180
[4.19-4.57]
TYP
45°X
0.045
[1.14]
0.685-0.695
[17.40-17.65]
TYP
V44A (REV J)

32 Lead Molded Plastic Leaded Chip Carrier
NS Package Number VA32A



44 Lead (10mm x 10mm) Molded Plastic Quad Flat Package, JEDEC
NS Package Number VEJ44A